# 1D Filter Module - Lattice Radiant Software

# User Guide

FPGA-IPUG-02099-1.1

June 2020

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# Acronyms in This Document

A list of acronyms used in this document.

| Acronym | Definition |
|---|---|
| FPGA | Field Programmable Gate Array |
| RTL | Register Transfer Level |
| IP | Intellectual Property |
| MSB | Most Significant Bit |
| LSB | Least Significant Bit |

# 1. Introduction

The 1D Filter Module has three modes: 1D Symmetry, 1D Asymmetry Serial, and 1D Asymmetry Parallel, which support configurable number of taps each with its own coefficient.

## 1.1. Quick Facts

Table 1.1 shows a summary of the 1D Filter Module.

**Table 1.1. 1D Filter Module Quick Facts**

| | | |
|---|---|---|
| **IP Requirements** | Supported FPGA Families | CrossLink™-NX, Certus™-NX |
| **Resource Utilization** | Targeted Devices | LIFCL-40, LIFCL-17, LFD2NX-40 |
| **Design Tool Support** | Lattice Implementation | Lattice Radiant® Software 2.1 |
| | Synthesis | Lattice Synthesis Engine (LSE) |
| | | Synopsys® Synplify Pro® for Lattice |
| | Simulation | For the list of supported simulators, see the Lattice Radiant Software 2.1 User Guide. |

## 1.2. Features

The key features of 1D Filter Module include:

- Supports the following modes:
  - 1D Symmetry
  - 1D Asymmetry Serial
  - 1D Asymmetry Parallel
- Configurable number of taps
- Supports both Positive and Negative Symmetry for 1D Symmetry Mode only
- Configurable Reset Mode
- Configurable data width and sign representation for Data A and B
- Configurable Bus Ordering

## 1.3. Conventions

### 1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

### 1.3.2. Signal Names

Signal names that end with:

- _*n* are active low
- _*i* are input signals
- _*o* are output signals

### 1.3.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

# 2. Functional Description

The 1D Filter Module filters the input data according to the following general equation:

$$result = \sum_{n=0}^{NUM\_OF\_TAPS} (A_n * B_n)$$

The following sections provides information on the 1D Filter Module modes:

- 1D Asymmetry Serial
- 1D Asymmetry Parallel
- 1D Symmetry

## 2.1. 1D Asymmetry Serial mode:

data_a_i width = *DATAA Width*,

data_b_i width = *Number of Taps * DATAB Width*

A is a data input that is provided serially, B is an input for coefficients which is provided in a parallel way.

For this mode, the output data is calculated as follows:

$$result = \sum_{n=0}^{NUM\_OF\_TAPS} (A_n * B[(n+1) * DATAB - 1 : n * DATAB])$$

## 2.2. 1D Asymmetry Parallel mode:

data_a_i width = *Number of Taps * DATAA Width*,

data_b_i width = *Number of Taps * DATAB Width*,

A is a data input, B is an input for coefficients; both are provided in a parallel way.

For this mode, the output data is calculated as follows:

$$result = \sum_{n=0}^{NUM\_OF\_TAPS} (A[(n+1) * DATAA - 1 : n * DATAA] * B[(n+1) * DATAB - 1 : n * DATAB])$$

## 2.3. 1D Symmetry mode:

data_a_i width = *DATAA Width*,

data_b_i width:

a. when the *Number of Taps* is odd, data_b_i width = $\frac{\text{Number of Taps} + 1}{2} * DATAB\ Width$,

b. when the *Number of Taps* is even, data_b_i width = $\frac{\text{Number of Taps}}{2} * DATAB\ Width.$

For this mode, the output data is calculated as follows:

$$result = \sum_{n=0}^{K} (A_n + A_{(k-n)}) * B[(n+1) * DATAB - 1 : n * DATAB]),$$

where

a. $K = \frac{\text{Number of Taps} + 1}{2}$, when *Number of Taps* is odd, and

b. $K = \frac{\text{Number of Taps}}{2}$, when *Number of Taps* is even.

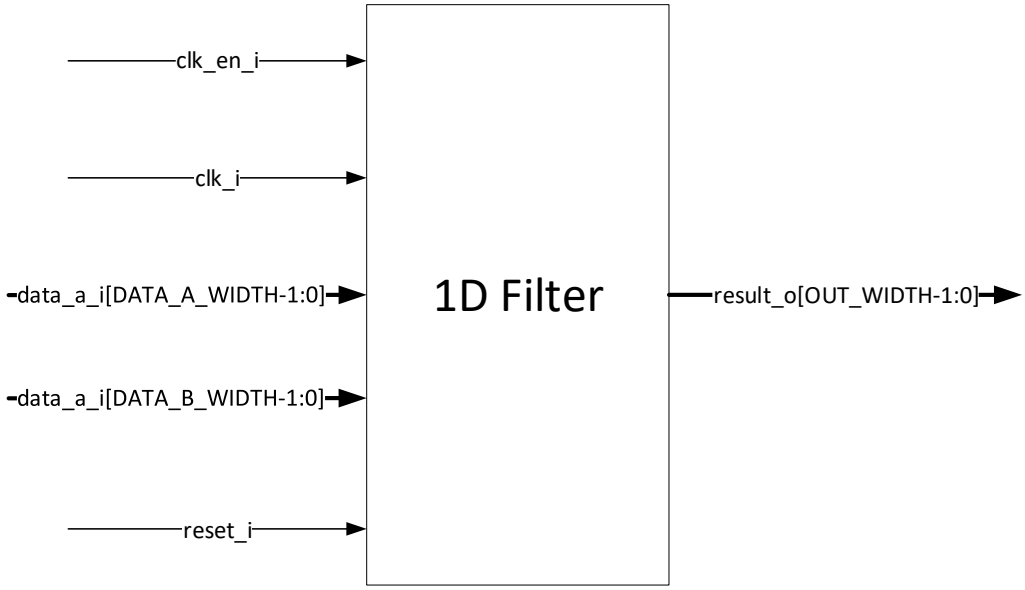


**Figure 2.1. 1D Filter Block Diagram**

## 2.4. Signal Descriptions

**Table 2.1. 1D Filter Module Signal Description**

| Port Name | I/O | Width | Description |
|---|---|---|---|
| **Clock and Reset Ports** | | | |
| clk_i | In | 1 | System clock input. |
| reset_i | In | 1 | Reset input. |
| **User Interface Ports** | | | |
| clk_en_i | In | 1 | Clock enable input. |
| data_a_i | In | *DATAA Width*[1] | Input data for port A. |
| data_b_i | In | *DATAB Width*[1] | Input data for port B. |
| result_o | Out | OUT_WIDTH[2] | Output data result. |

**Notes:**

1. The bit width of some signals is set by the attribute. Refer to Table 2.2 for the description of these attributes.
2. a. If *DATAA Width* <= 9 and *DATAB Width* <= 9, then OUT_WIDTH = *DATAA Width* + *DATAB Width* +6;
   b. If at least one of *DATAA Width* or *DATAB Width* > 9, then OUT_WIDTH = *DATAA Width* + *DATAB Width* + 18

## 2.5. Attribute Summary

The configurable attributes of the 1D Filter Module are shown in Table 2.2 and are described in Table 2.3. The attributes can be configured through the IP Catalog's Module/IP wizard of the Lattice Radiant Software.

**Table 2.2. Attributes Table**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| **Configuration** | | | |
| Mode | 1D Symmetry,<br>1D Asymmetry Serial,<br>1D Asymmetry Parallel | 1D Asymmetry Serial | — |
| Number of Taps | 2 – N | 2 | For Device Type LIFCL-40 or LFD2NX-40:<br>If *Mode* == 1D Symmetry, N = 110,<br>else N = 55<br>For Device Type LIFCL-17:<br>If *Mode* == 1D Symmetry, N = 48,<br>else N = 24 |
| Symmetry | Positive, Negative | Positive | Active if *Mode* == 1D Symmetry |
| Reset Mode | Sync, Async | Sync | — |
| DATAA Sign | Signed, Unsigned | Signed | Active if *Symmetry* == Positive |
| DATAA Width | 2 – 18 | 18 | — |
| DATAB Sign | Signed, Unsigned | Signed | Active if *Symmetry* == Positive |
| DATAB Width | 2 – 18 | 18 | — |
| Bus Ordering Style | Big Endian [MSB : LSB],<br>Little Endian [LSB : MSB] | Big Endian [MSB : LSB] | — |

**Table 2.3. Attributes Descriptions**

| Attribute | Description |
|---|---|
| **Configuration** | |
| Mode | Specifies the mode of 1D Filter Module. Refer to Functional Description section for more details. |
| Number of Taps | Specifies the number of taps. |
| Symmetry | Specifies the Symmetry of the 1D Filter Module. Selectable values are Positive and Negative Symmetry. |
| Reset Mode | Specifies the mode of reset that is used. |
| DATAA Sign | Specifies the sign representation for port data_a_i. |
| DATAA Width | Specifies the data width for port A. The exact value of this attribute can be calculated depending on the type of *Mode*. Refer to Functional Description section for more details. |
| DATAB Sign | Specifies the sign representation for port data_b_i. |
| DATAB Width | Specifies the data width for port B. The exact value of this attribute can be calculated depending on the type of *Mode*. Refer to Functional Description section for more details. |
| Bus Ordering Style | Specifies the bus ordering of input and output data ports.<br>Big Endian: the data_a_i, data_b_i and result_o busses ordering is from MSB to LSB.<br>Little Endian: the data_a_i, data_b_i and result_o busses ordering is from LSB to MSB; |

# 3. IP Generation, Synthesis, and Validation

This section provides information on how to generate and synthesize this module using the Lattice Radiant Software. For more on Lattice Radiant Software, please refer to the Lattice Radiant Software 2.1 User Guide and relevant tutorials.

## 3.1. Licensing the IP

No license is required for this module.

## 3.2. Generating and Synthesizing the IP

The Lattice Radiant Software allows you to customize and generate modules and IPs and integrate them into the device's architecture. The procedure for generating the 1D Filter Module in Lattice Radiant Software is described below.

To generate the 1D Filter Module:

1. Create a new Lattice Radiant Software project or open an existing project.
2. In the IP Catalog tab, double-click on **1D_Filter** under **Module, DSP_Arithmetic_Modules** category.
3. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

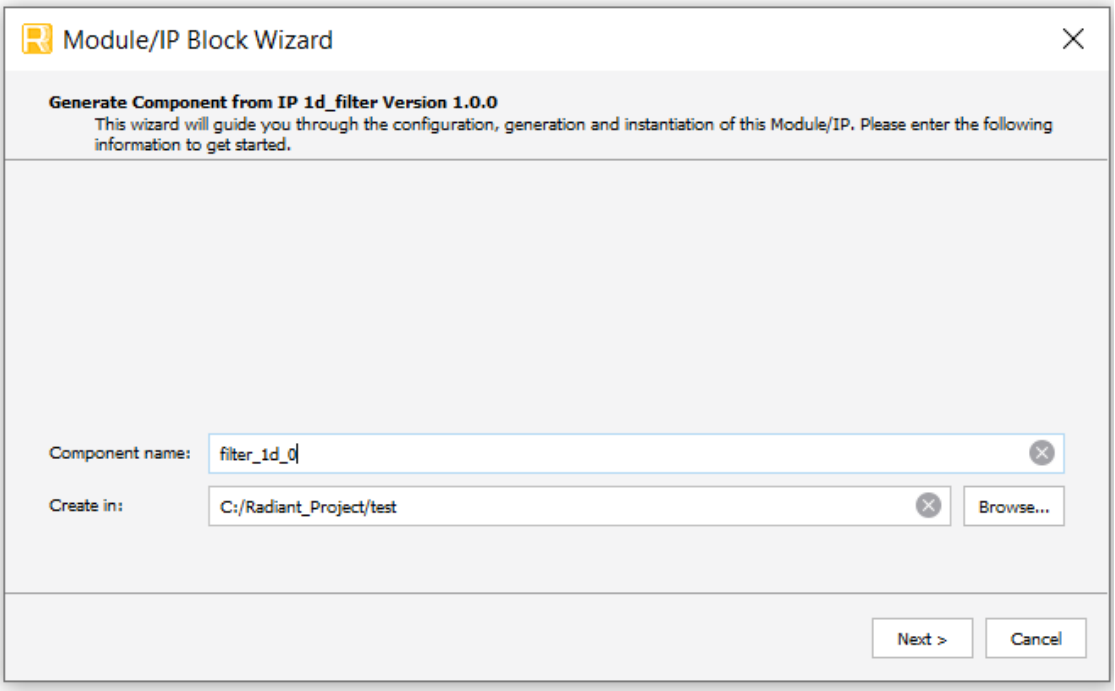


**Figure 3.1. Module/IP Block Wizard**

4. In the module's dialog box of the **Module/IP Block Wizard** window, customize the selected 1D Filter Module using drop-down menus and check boxes. As a sample configuration, see Figure 3.2. For configuration options, see the Attribute Summary section.

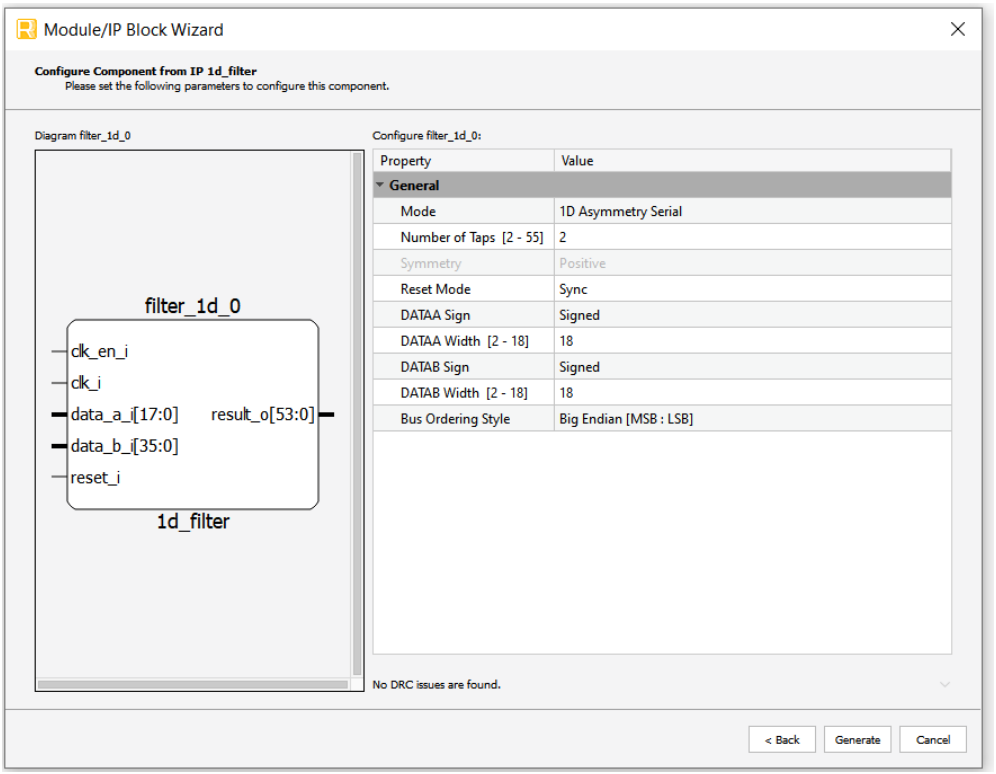


**Figure 3.2. Configure User Interface of 1D Filter Module**

5. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 3.3.

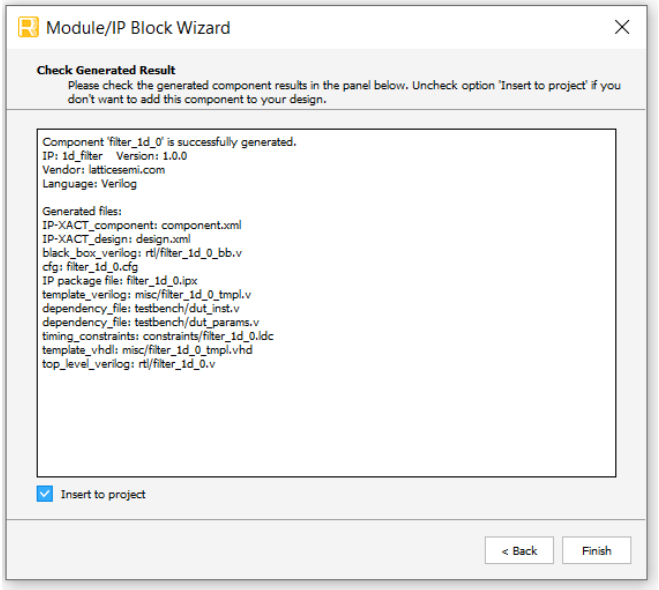


**Figure 3.3. Check Generating Result**

6. Click **Finish**. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 3.1.

The generated 1D Filter Module package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the module in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

**Table 3.1. Generated File List**

| Attribute | Description |
|---|---|
| <Instance Name>.ipx | This file contains the information on the files associated to the generated IP. |
| <Instance Name>.cfg | This file contains the attribute values used in IP configuration. |
| component.xml | Contains the ipxact:component information of the IP. |
| design.xml | Documents the configuration attributes of the IP in IP-XACT 2014 format. |
| rtl/<Instance Name>.v | This file provides an example RTL top file that instantiates the module. |
| rtl/<Instance Name>_bb.v | This file provides the synthesis black box. |
| misc/<Instance Name>_tmpl.v<br>misc /<Instance Name>_tmpl.vhd | These files provide instance templates for the module. |

## 3.3. Running the Functional Simulation

Running functional simulation can be performed after the IP is generated.

To run functional simulation:

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in Figure 3.4.

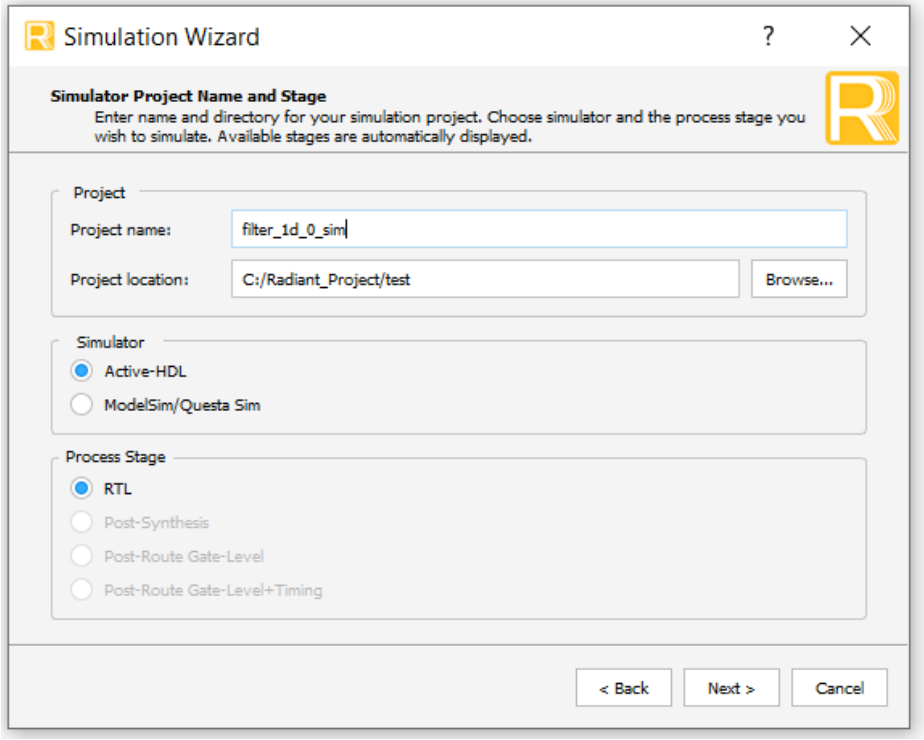


**Figure 3.4. Simulation Wizard**

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

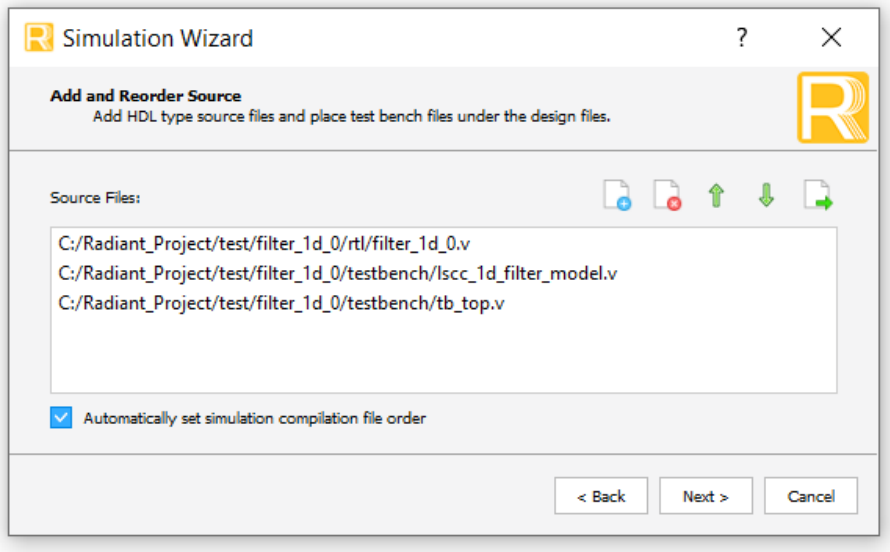


**Figure 3.5. Adding and Reordering Source**

3. Click **Next**. The **Summary** window is shown.
4. Click **Finish** to run the simulation.

**Note:** It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant Software Suite.

The results of the simulation in our example are provided in Figure 3.6.

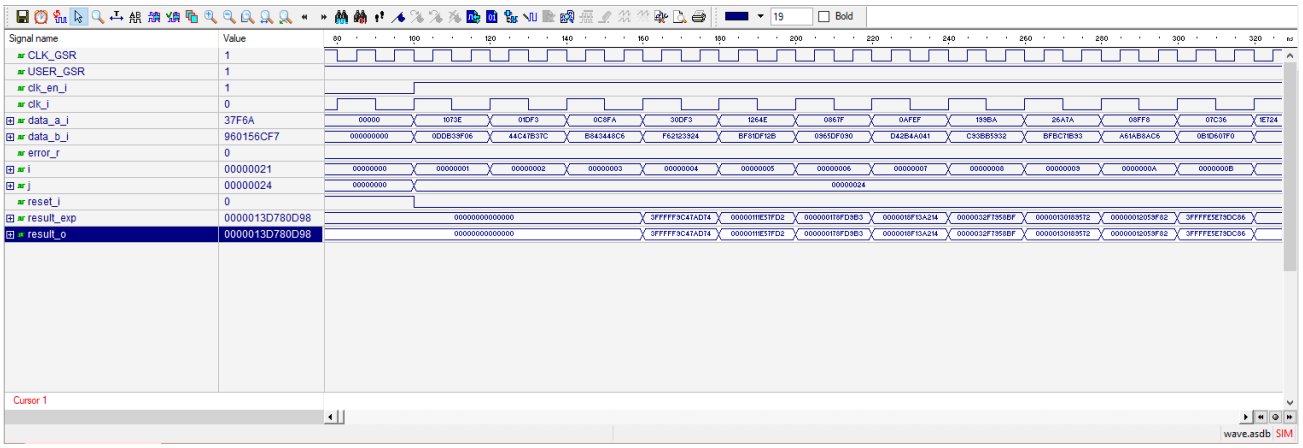


**Figure 3.6. Simulation Waveform**

# Appendix A. Resource Utilization

Table A.1 shows the resource utilization of the 1D Filter Module for the LIFCL-40-9BG400I device, using Lattice Synthesis Engine of Lattice Radiant Software. Default configuration is used and some attributes are changed from the default value to show the effect on the resource utilization.

**Table A.1. Resource Utilization**

| Configuration | Clk Fmax (MHz)* | Slice Registers | LUTs | DSP Slices |
|---|---|---|---|---|
| Default | 200 MHz | 0 | 1 | 1 |
| *DATAA Width* = 2, *DATAB Width* = 2, Others = Default | 200 MHz | 0 | 1 | 1 |
| *Mode* = 1D Symmetry, *Symmetry* = Negative, Others = Default | 200 MHz | 0 | 1 | 1 |
| *Number of taps* = 5, Others = Default | 200 MHz | 0 | 1 | 2 |

***Note:** Fmax is generated when the FPGA design only contains 1D Filter Module and the target frequency is 200 MHz. These values may be reduced when user logic is added to the FPGA design.

# References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software 2.1 User Guide.

# Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

# Revision History

**Document Revision 1.1, Lattice Radiant SW version 2.1, June 2020**

| Section | Change Summary |
|---|---|
| Introduction | Updated Table 1.1.<br>• Added support to Certus-NX<br>• Added LFD2NX-40 as targeted device.<br>• Updated Lattice Implementation to Lattice Radiant 2.1. |
| Attribute Summary | Updated dependency of *Number of Taps* to support LFD2NX-40. |
| Appendix A. Resource Utilization | Updated device to LIFCL-40-9BG400I. |

**Document Revision 1.0, Lattice Radiant SW version 2.0, February 2020**

| Section | Change Summary |
|---|---|
| All | Initial release. |


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