Barrel Shifter Module - Lattice Radiant Software

User Guide

FPGA-IPUG-02088-1.1

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field Programmable Gate Array
RTL	Register Transfer Level
IP	Intellectual Property
MSB	Most Significant Bit
LSB	Least Significant Bit

1. Introduction

The Barrel Shifter Module is a pipeline shifter designed to shift a data word by the specified number of bits either in the left or the right direction. Zero Insert and Rotate types of shifts are available for shifts in either direction. In addition, the Sign Extension type is available for the shift in the right direction.

1.1. Quick Facts

Table 1.1 shows a summary of the Barrel Shifter Module.

Table 1.1. Barrel Shifter Module Quick Facts

IP Requirements	Supported FPGA Families	CrossLink™-NX, Certus™-NX
Resource Utilization	Targeted Devices	LIFCL-40, LIFCL-17, LFD2NX-40
Design Tool Support	Lattice Implementation	Lattice Radiant® Software 2.1
	Synthesis	Lattice Synthesis Engine (LSE)
		Synopsys® Synplify Pro® for Lattice
	Simulation	For the list of supported simulators, see the Lattice Radiant Software 2.1 User Guide.

1.2. Features

The key features of Barrel Shifter Module include:

- Configurable shift direction
- Configurable data width
- Configurable maximum number of shifts
- Configurable Reset Mode
- Supports Enable/Disable of Input, Output and Pipeline Registers
- Configurable Bus Ordering

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- *_n* are active low
- *_i* are input signals
- *_o* are output signals

1.3.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

2.1. Overview

The Barrel Shifter Module shifts a data word by a specified number of bits. Depending on the shift direction chosen, it shifts the values in the register to the left or to the right by the number of bits stipulated by shift_i signal. The right shift means shifting from MSB to LSB while left shift means shifting from LSB to MSB.

For left shift there are two possible shift types: Zero Insert and Rotate. When Zero Insert shift type is selected, the freed LSB bits are replaces by '0'. When Rotate shift type is selected, the freed LSB bits are replaces by MSB bits which came out of the word after left shift. For example, if the previous binary representation of eight bits original word is *1100 1001* and it is shifted to the left by 3 bits, then for Zero Insert shift type the result is *0100 1000* while for Rotate shift type the final result is *0100 1110*.

For right shift, besides described for left shift two shift types (Zero Insert and Rotate), there is one additional shift type called Sign Extension. For that shift type, the freed MSB bits is replaced by the original MSB bit's value. For example, if binary representation of the eight bits original word is *1101 1001* and it is shifted to the right by 3 bits, then for Sign Extension shift type the result is *1111 1011*. If the previous binary representation of eight bits original word is *0101 1001* (or original MSB was zero) and it is shifted to the right by 3 bits, then for Sign Extension shift type the final result is *0001 1011*.

There are two possible bus ordering modes: Big Endian and Little Endian. When Big Endian is chosen, the data_i, shift_i and result_o busses ordering is from MSB to LSB, otherwise from LSB to MSB.

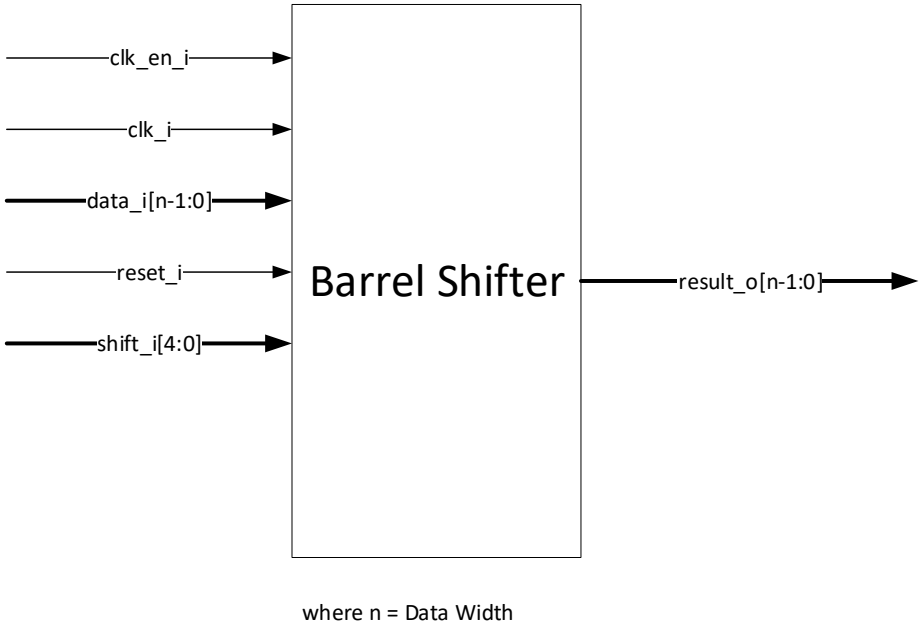

Figure 2.1. Barrel Shifter Block Diagram

2.2. Signal Descriptions

Table 2.1. Barrel Shifter Module Signal Description

Port Name	I/O	Width	Description
Clock and Reset Ports			
clk_i	In	1	System clock input. Available if any of the following attributes is/are enabled: *Enable Input Register, Enable Pipeline Register or Enable Output Register.*
reset_i	In	1	Reset input. Available if any of the following attributes is/are enabled: *Enable Input Register, Enable Pipeline Register or Enable Output Register.*
User Interface Ports			
clk_en_i	In	1	Clock enable input. Available if any of the following attributes is/are enabled: *Enable Input Register, Enable Pipeline Register or Enable Output Register.*
data_i	In	*Data Width**	Data input.
shift_i	In	*5*	Shift input. This signal shows the number of bits by which data input is shifted.
result_o	Out	*Data Width**	Result output.

***Note:** The bit width of some signals is set by the attribute. Refer to Table 2.2 for the description of these attributes.

2.3. Attribute Summary

The configurable attributes of the Barrel Shifter Module are shown in Table 2.2 and are described in Table 2.3. The attributes can be configured through the IP Catalog's Module/IP wizard of the Lattice Radiant Software.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
Configuration			
Shift Direction	Left, Right	Left	—
Type	Zero Insert, Rotate, Sign Extension	Zero Insert	Sign Extension is only available when *Shift Direction* == Right
Data Width	2 – 40	36	—
Maximum Number of Shifts	1 – 35	31	—
Reset Mode	Sync, Async	Sync	Active if: *Enable Fully Pipelined Mode* == Checked or *Enable Input Register* == Checked or *Enable Output Register* == Checked
Enable Input Register	Checked, Unchecked	Checked	—
Enable Pipeline Register	Checked, Unchecked	Checked	—
Enable Output Register	Checked, Unchecked	Checked	—
Bus Ordering Style	Litte Endian, Big Endian	Big Endian	—

Table 2.3. Attributes Descriptions

Attribute	Description
Configuration	
Shift Direction	Specifies the direction of the shift. Left: shifting from MSB to LSB, Right: shifting from LSB to MSB.
Type	For detailed description see Overview section.
Data Width	Specifies the width of input and output data.
Maximum Number of Shifts	Specifies the maximum possible shift value coming from shift_i input.
Reset Mode	Specifies the mode of reset to be used. *Reset Mode* can only be configured if any of the following attributes is/are enabled: *Enable Fully Pipelined Mode, Enable Input Register or Enable Output Register.*
Enable Input Register	Specifies if input register is enabled or not.
Enable Pipeline Register	Specifies if the data pipeline is enabled or not.
Enable Output Register	Specifies if output register is enabled or not.
Bus Ordering Style	Specifies the bus ordering of shift, input and output data ports. Little Endian: the data_i, shift_i and result_o busses ordering is from LSB to MSB; Big Endian: the data_i, shift_i and result_o busses ordering is from MSB to LSB

3. IP Generation, Synthesis, and Validation

This section provides information on how to generate and synthesize this module using the Lattice Radiant Software. For more on Lattice Radiant Software, please refer to the Lattice Radiant Software 2.1 User Guide and relevant tutorials.

3.1. Licensing the IP

No license is required for this module.

3.2. Generating and Synthesizing the IP

The Lattice Radiant Software allows you to customize and generate modules and IPs and integrate them into the device's architecture. The procedure for generating the Barrel Shifter Module in Lattice Radiant Software is described below.

To generate the Barrel Shifter Module:

1. Create a new Lattice Radiant Software project or open an existing project.
2. In the IP Catalog tab, double-click on Barrel Shifter under Module, Arithmetic_Modules category.
3. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

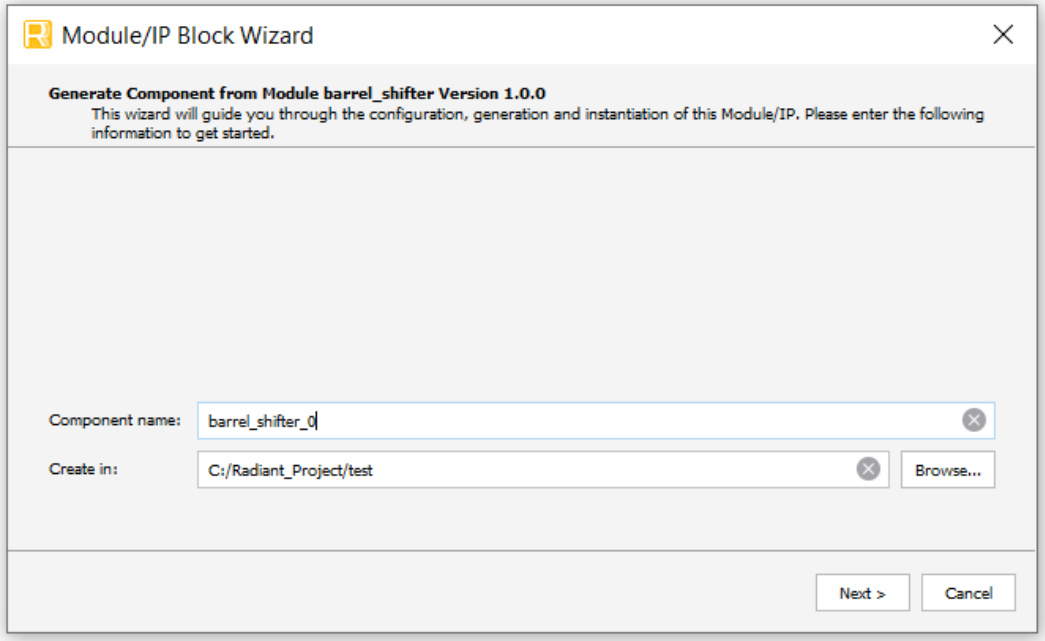

Figure 3.1. Module/IP Block Wizard

4. In the module's dialog box of the **Module/IP Block Wizard** window, customize the selected Barrel Shifter Module using drop-down menus and check boxes. As a sample configuration, see Figure 3.2. For configuration options, see the Attribute Summary section.

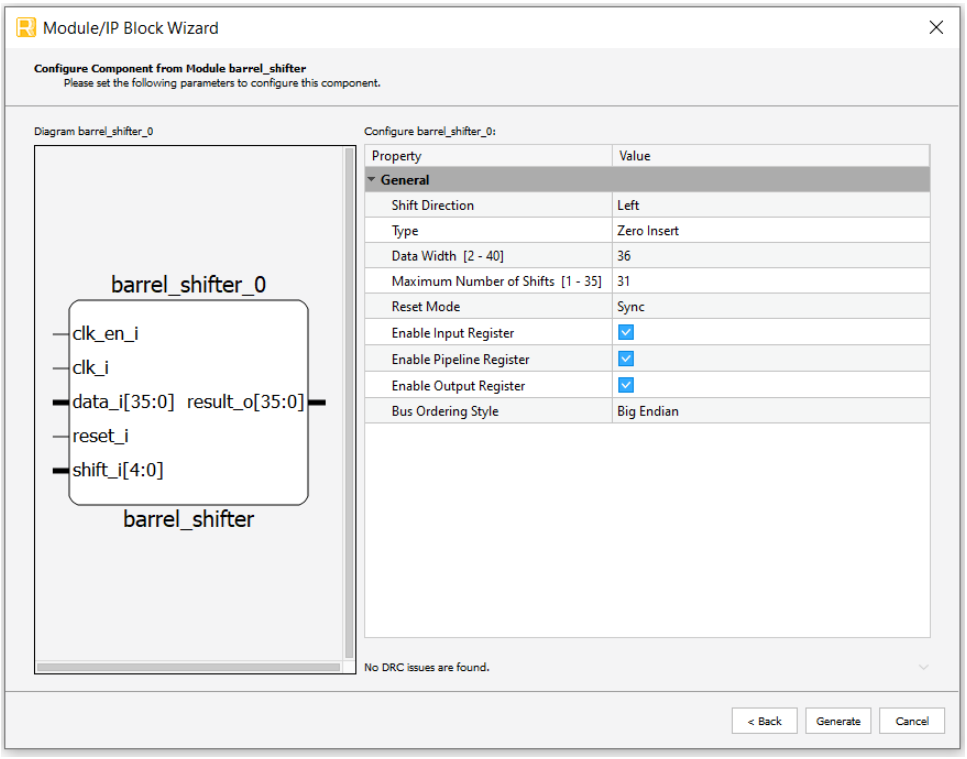

Figure 3.2. Configure User Interface of Barrel Shifter Module

5. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 3.3.

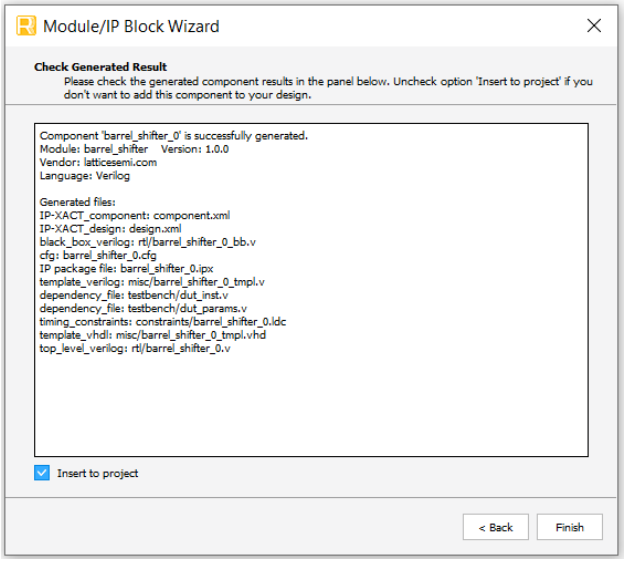

Figure 3.3. Check Generating Result

6. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 3.1.

The generated Barrel Shifter Module package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the module in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the attribute values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration attributes of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the module.

3.3. Running the Functional Simulation

Running functional simulation can be performed after the IP is generated.

To run functional simulation:

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in Figure 3.4.

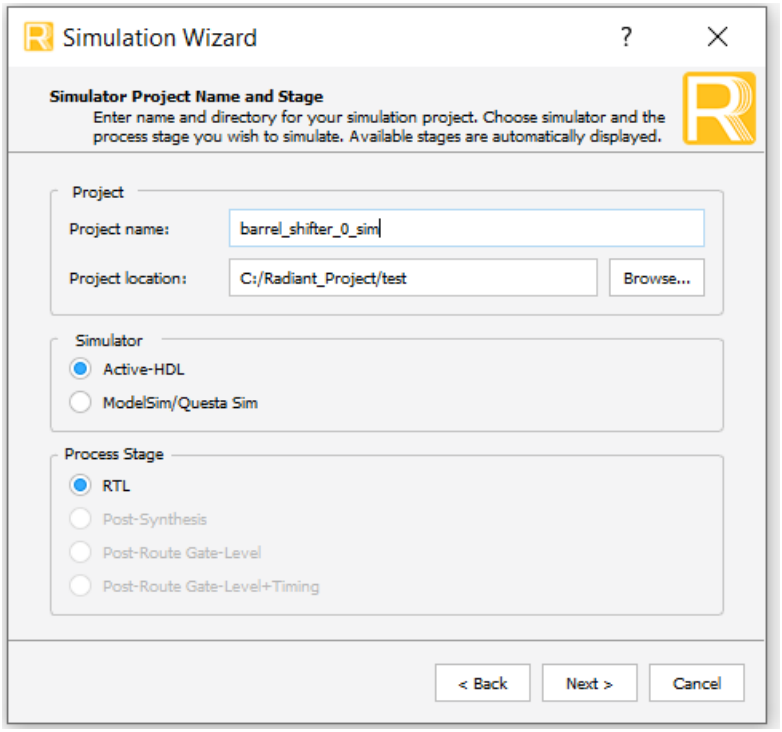

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

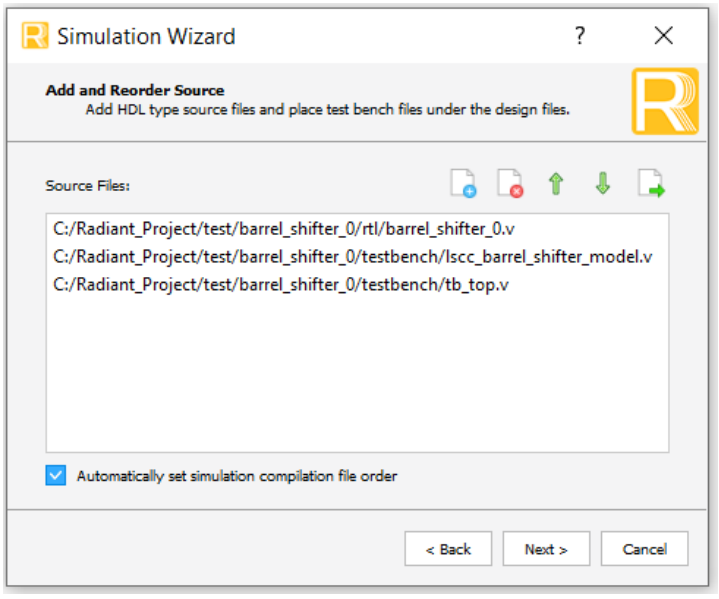

Figure 3.5. Adding and Reordering Source

3. Click **Next**. The **Summary** window is shown.
4. Click **Finish** to run the simulation.

Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant Software Suite.

The results of the simulation in our example are provided in Figure 3.6.

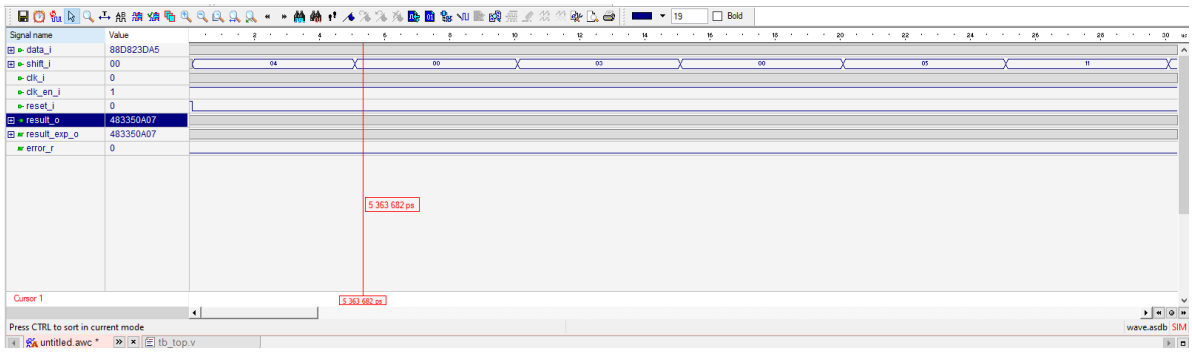

Figure 3.6. Simulation Waveform

Appendix A. Resource Utilization

Table A.1 shows the resource utilization of the Barrel Shifter Module for the LIFCL-40-9BG400I device, using Lattice Synthesis Engine of Lattice Radiant Software. Default configuration is used and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.1. Resource Utilization

Configuration	Clk Fmax (MHz)*	Slice Registers	LUTs	EBRs
Default	200 MHz	113	175	0
Shift Direction = Right, *Reset Mode* = Async, Others = Default	200 MHz	113	175	0
Data Width = 10, *Maximum Number of Shifts* = 9, Others = Default	200 MHz	32	34	0
Enable Input Register = Unchecked, *Enable Pipeline Register* = Unchecked, *Enable Output Register* = Unchecked, Others = Default	N/A	0	175	0

***Note:** Fmax is generated when the FPGA design only contains Barrel Shifter Module and the target frequency is 200 MHz. These values may be reduced when user logic is added to the FPGA design.

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software 2.1 User Guide.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Document Revision 1.1, Lattice Radiant SW version 2.1, June 2020

Section	Change Summary
Introduction	Updated Table 1.1. • Added Certus-NX support. • Updated Table 1.1 to add LFD2NX-40 as targeted device. • Updated Lattice Implementation to Lattice Radiant 2.1.
Appendix A. Resource Utilization	Updated device to LIFCL-40-9BG400I.

Document Revision 1.0, Lattice Radiant SW version 2.0, February 2020

Section	Change Summary
All	Initial release.

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