APB Interconnect Module - Lattice Propel Builder

User Guide

FPGA-IPUG-02054-1.2

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
APB	Advanced Peripheral Bus
AMBA	Advanced Microcontroller Bus Architecture
FPGA	Field Programmable Gate Array
RTL	Register Transfer Level

1. Introduction

The Lattice Semiconductor APB Interconnect Module is a fully parameterized soft IP for low latency interconnect fabric for APB system. It can be used to connect one or more APB bus master to one or more APB bus slave. Master-side arbitration is implemented within the module to minimize resource utilizaton. This means only one master can access any of the slaves at any given time. The APB Interconnect Module supports round-robin based and fixed priority based arbitration when multiple bus masters access the same slave port. The arbitration completes in one clock cycle, which means that the transaction is delayed by one clock cycle when arbitration occurs.

The design is implemented in Verilog HDL. The IP can be configured and generated based on Table 1.1.

Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation

Supported FPGA Family	IP Configuration and Generation	IP Implementation (Synthesis, Map, Place and Route)
MachXO2™	Lattice Propel™ Builder software	Lattice Diamond® software
MachXO3™	Lattice Propel Builder software	Lattice Diamond software
MachXO3D™	Lattice Propel Builder software	Lattice Diamond software
Mach™-NX	Lattice Propel Builder software	Lattice Diamond software
CrossLink™-NX	Lattice Propel Builder software	Lattice Radiant™ software
Certus™-NX	Lattice Propel Builder software	Lattice Radiant software

1.1. Features

The key features of the APB Interconnect Module include:

- Compliance with AMBA 3 APB Protocol v1.0
- Fully parameterized design
- Data Bus width of up to 32 bits [8, 16, 32]
- Address width of up to 32 bits [11,12,...,32]
- Support to up to 32 masters and 32 slaves
- Slave port address decoding
- Master side arbitration
- Selectable arbitration scheme:
  - Round robin
  - Fixed priority

2. Functional Description

2.1. Overview

The Lattice Semiconductor APB Interconnect Module is a fully parameterized soft IP, low latency interconnect fabric for AMBA 3 APB based systems, enabling one or more bus masters to be connected to one or more slaves. This module is compliant with AMBA 3 APB Protocol v1.0.

AMBA3 advanced peripheral bus (APB) is a low-cost interface that is optimized for minimal power consumption and reduced interface complexity. APB should be used for any peripherals that are low-bandwidth and do not require the high performance of a pipelined bus interface. For example, UART, I^2C, and GPIO. The APB is an unpipelined protocol, which means that the APB master can only initiate a new transfer after the previous transfer is completed.

The APB-3 interface protocol does not have any *size* or *byte enable* signals to indicate transfer size. That is, all APB transfers are accessing the full width of the data bus. Thus, in a 32-bit processor system application, the data bus should be 32 bits.

2.2. Interface Description

Figure 2.1 shows the interface diagram for the APB Interconnect Module. The diagram shows all of the available ports for the IP core.

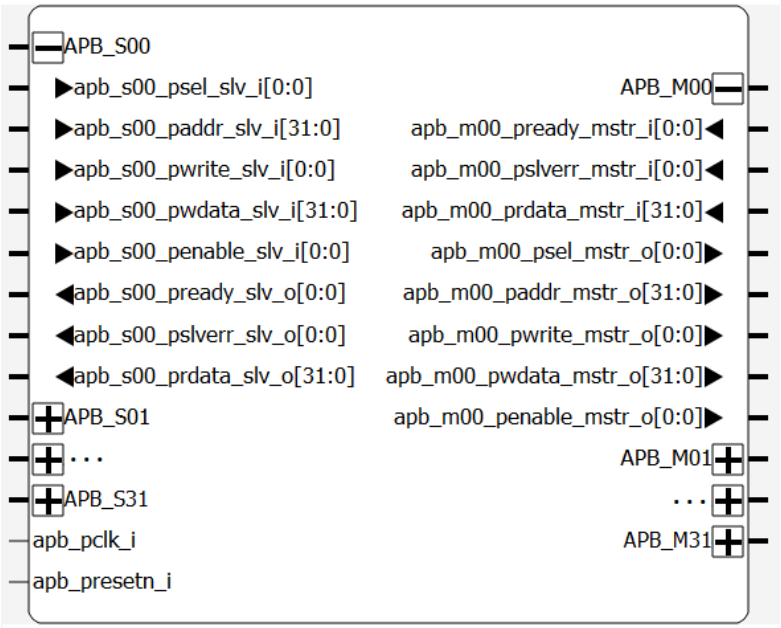

Figure 2.1. APB Interconnect Module Interface Diagram

Table 2.1. APB Interconnect Module Signal Description

Pin Name	Direction	Width (Bits)	Description
Clock and Reset			
apb_pclk_i	In	1	APB clock
apb_presetn_i	In	1	APB active LOW reset
APB Slave Interface 00 (APB_M00)			
apb_m00_psel_mstr_o	Out	1	Select signal Indicates that the slave device is selected and that a data transfer is required.
apb_m00_paddr_mstr_o	Out	*M_ADDR_WIDTH*	Address signal
apb_m00_pwdata_mstr_o	Out	*DATA_WIDTH*	Write data signal
apb_m00_pwrite_mstr_o	Out	1	Direction signal Write = 1, Read = 0
apb_m00_penable_mstr_o	Out	1	Enable signal Indicates the second and subsequent cycles of an APB transfer.
apb_m00_pready_mstr_i	In	1	Ready signal Indicates transfer completion. Slave uses this signal to extend an APB transfer.
apb_m00_pslverr_mstr_i	In	1	Error signal Indicates a transfer failure. In case APB Slave does not have this signal, it should be tied to 1'b0.
apb_m00_prdata_mstr_i	In	*DATA_WIDTH*	Read data signal
APB Slave Interface 01 (APB_M01)			
apb_m01_psel_mstr_o	Out	1	Select signal Indicates that the slave device is selected and that a data transfer is required.
apb_m01_paddr_mstr_o	Out	*M_ADDR_WIDTH*	Address signal
apb_m01_pwdata_mstr_o	Out	*DATA_WIDTH*	Write data signal
apb_m01_pwrite_mstr_o	Out	1	Direction signal Write = 1, Read = 0
apb_m01_penable_mstr_o	Out	1	Enable signal Indicates the second and subsequent cycles of an APB transfer.
apb_m01_pready_mstr_i	In	1	Ready signal Indicates transfer completion. Slave uses this signal to extend an APB transfer.
apb_m01_pslverr_mstr_i	In	1	Error signal Indicates a transfer failure. In case APB Slave does not have this signal, it should be tied to 1'b0.
apb_m01_prdata_mstr_i	In	*DATA_WIDTH*	Read data signal
…			—
APB Slave Interface xx (APB_Mxx)			
apb_mxx_psel_mstr_o	Out	1	Select signal Indicates that the slave device is selected and that a data transfer is required.
apb_mxx_paddr_mstr_o	Out	*M_ADDR_WIDTH*	Address signal
apb_mxx_pwdata_mstr_o	Out	*DATA_WIDTH*	Write data signal
apb_mxx_pwrite_mstr_o	Out	1	Direction signal Write = 1, Read = 0
apb_mxx_penable_mstr_o	Out	1	Enable signal Indicates the second and subsequent cycles of an APB transfer.

Pin Name	Direction	Width (Bits)	Description
apb_mxx_pready_mstr_i	In	1	Ready signal Indicates transfer completion. Slave uses this signal to extend an APB transfer.
apb_mxx_pslverr_mstr_i	In	1	Error signal Indicates a transfer failure. In case APB Slave does not have this signal, it should be tied to 1'b0.
apb_mxx_prdata_mstr_i	In	*DATA_WIDTH*	Read data signal
APB Master Interface 00 (APB_S00)			
apb_s00_psel_mstr_i	In	1	Select signal Indicates that this APB interface is selected and that a data transfer is required.
apb_s00_paddr_mstr_i	In	*M_ADDR_WIDTH*	Address signal
apb_s00_pwdata_mstr_i	In	*DATA_WIDTH*	Write data signal
apb_s00_pwrite_mstr_i	In	1	Direction signal Write = 1, Read = 0
apb_s00_penable_mstr_i	In	1	Enable signal Indicates the second and subsequent cycles of an APB transfer.
apb_s00_pready_mstr_o	Out	1	Ready signal Indicates transfer completion. This signal is used to extend an APB transfer.
apb_s00_pslverr_mstr_o	Out	1	Error signal Indicates a transfer failure.
apb_s00_prdata_mstr_o	Out	*DATA_WIDTH*	Read data signal
APB Master Interface 01 (APB_S01)			
apb_s01_psel_mstr_i	In	1	Select signal Indicates that this APB interface is selected and that a data transfer is required.
apb_s01_paddr_mstr_i	In	*M_ADDR_WIDTH*	Address signal
apb_s01_pwdata_mstr_i	In	*DATA_WIDTH*	Write data signal
apb_s01_pwrite_mstr_i	In	1	Direction signal Write = 1, Read = 0
apb_s01_penable_mstr_i	In	1	Enable signal Indicates the second and subsequent cycles of an APB transfer.
apb_s01_pready_mstr_o	Out	1	Ready signal Indicates transfer completion. This signal is used to extend an APB transfer.
apb_s01_pslverr_mstr_o	Out	1	Error signal Indicates a transfer failure.
apb_s01_prdata_mstr_o	Out	*DATA_WIDTH*	Read data signal
…			
APB Master Interface yy (APB_Syy)			
apb_syy_psel_mstr_i	In	1	Select signal Indicates that this APB interface is selected and that a data transfer is required.
apb_syy_paddr_mstr_i	In	*M_ADDR_WIDTH*	Address signal
apb_syy_pwdata_mstr_i	In	*DATA_WIDTH*	Write data signal
apb_syy_pwrite_mstr_i	In	1	Direction signal Write = 1, Read = 0
apb_syy_penable_mstr_i	In	1	Enable signal Indicates the second and subsequent cycles of an APB transfer.

Pin Name	Direction	Width (Bits)	Description
apb_syy_pready_mstr_o	Out	1	Ready signal Indicates transfer completion. This signal is used to extend an APB transfer.
apb_syy_pslverr_mstr_o	Out	1	Error signal Indicates a transfer failure.
apb_syy_prdata_mstr_o	Out	*DATA_WIDTH*	Read data signal

Notes:

- xx – Possible values are (02, 03,…, *Total APB Slaves* -1).
- yy – Possible values are (02, 03,…, *Total APB Masters* -1).

All APB Master/Slave Interfaces are compliant with APB protocol. Refer to AMBA 3 APB Protocol v1.0 Specification for the timing diagrams and for more information on the protocol.

2.3. Attributes Summary

Table 2.2 provides a list of the user configurable attributes of the APB Interconnect Module. The attribute values are specified using the IP core configuration user interface in the Propel Builder software as shown in Table 2.2.

Table 2.2. Attributes Table[5]

Attribute	Selectable Values	Default	Dependency on Other Attributes[3]
General Tab			
General Group			
Total APB Masters	1–32	2	*Total APB Masters* and *Total APB Slaves* cannot be both 1
Total APB Slaves	1–32	2	
Master Address Width(bits) (M_ADDR_WIDTH)	11–32	32	—
Full Address Decoding up to 1kB[1]	Checked, Unchecked	Checked	—
Data Bus Width(bits) (DATA_WIDTH)	8, 16, 32	32	—
Registered Output[2]	Checked, Unchecked	Unchecked	—
Main Settings Tab[3]			
Slave 0 Settings Group			
S0 Base Address	0–($2^{M\_ADDR\_WIDTH}$ – 'h400)	32'h00000000	en_s0
S0 Address Range	'h400–$2^{M\_ADDR\_WIDTH}$	32'h00000400	en_s0
Slave 1 Settings Group	—	—	—
S1 Base Address	0–($2^{M\_ADDR\_WIDTH}$ – 'h400)	32'h00002000	en_s1
S1 Address Range	'h400–$2^{M\_ADDR\_WIDTH}$	32'h00000400	en_s1
…			
Slave 31 Settings Group	—	—	—
S31_FRAGMENT_CNT	1–8	1	en_s31
S31 Base Address	0–($2^{M\_ADDR\_WIDTH}$ – 'h400)	32'h0003E000	en_s31
S31 Address Range	'h400–$2^{M\_ADDR\_WIDTH}$	32'h00000400	en_s31
Master Priority Settings Tab			
Slave 0 Settings Group			
Arbiter Scheme[4]	Round Robin, Fixed Priority, Weighted Round Robin	Round Robin	en_s0
Master 0 Priority	0–32	1	en_s0 and en_m1 and
Master 1 Priority	0–32	2	(*Arbiter Scheme* == Fixed Priority)
Master 2 Priority	0–32	3	en_s0 and en_m1 and
…	—	—	(*Arbiter Scheme* == Fixed Priority)
Master 31 Priority	0–32	32	en_s0 and en_m2 and

Attribute	Selectable Values	Default	Dependency on Other Attributes[3]
Slave 1 Settings Group			
Arbiter Scheme[4]	Round Robin, Fixed Priority, Weighted Round Robin	Round Robin	*Total APB Slaves* >= 2
Master 0 Priority	0–32	1	en_s1 and en_m1 and
Master 1 Priority	0–32	2	(*Arbiter Scheme* == Fixed Priority)
Master 2 Priority	0–32	3	en_s1 and en_m1 and
…	—	—	(*Arbiter Scheme* == Fixed Priority)
Master 31 Priority	0–32	32	en_s1 and en_m2 and
…			
Slave 31 Settings Group			
Arbiter Scheme[4]	Round Robin, Fixed Priority, Weighted Round Robin	Round Robin	en_s31
Master 0 Priority	0–32	1	en_s31 and en_m1 and
Master 1 Priority	0–32	2	(*Arbiter Scheme* == Fixed Priority)
Master 2 Priority	0–32	3	en_s31 and en_m1 and
…	—	—	(*Arbiter Scheme* == Fixed Priority)
Master 31 Priority	0–32	32	en_s31 and en_m2 and

Notes:

1. [*Full Address Decoding up to 1kB* = Checked] is currently not supported.
2. [*Registered Output* = Unchecked] is currently not supported.
3. Settings under Main Settings Tab are not configurable when the IP is being configured using System Builder because the tool manages the address map.
4. [*Arbiter Scheme* = Weighted Round Robin] is currently not supported.
5. To simplify the condition, en_s0, en_s1 to en_s31 are used for the condition that the corresponding connection to external slave is enabled. Similarly, en_m0, en_m1, en_m2, and en_m31 are used for the condition that the corresponding connection to external master is enabled.

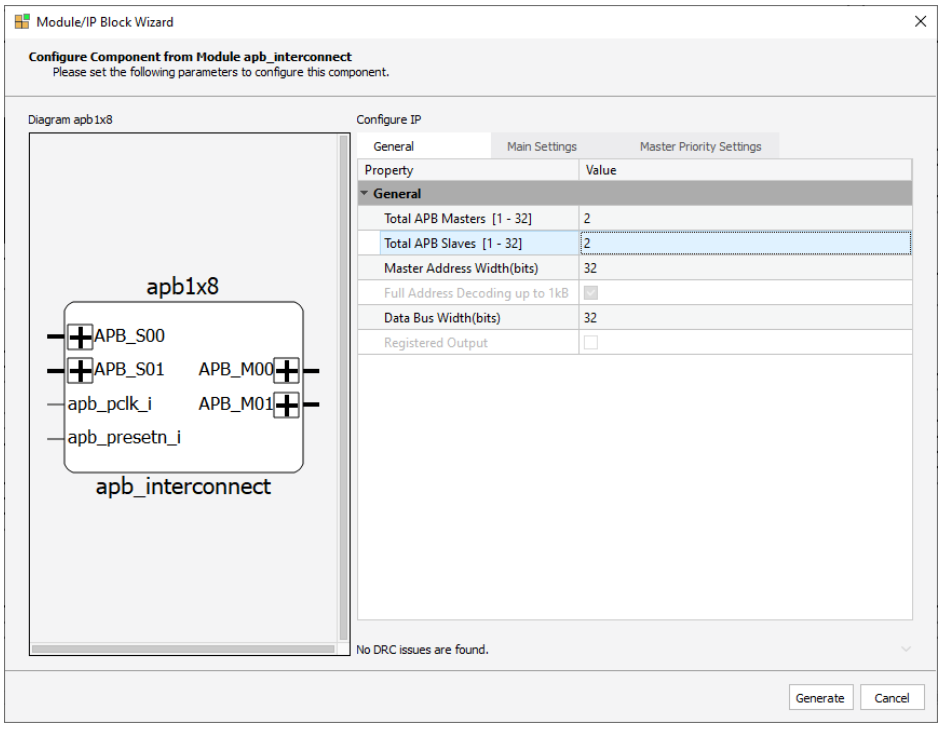

Figure 2.2. APB Interconnect Module/IP Block Wizard

Table 2.3. Attributes Description

Attribute	Description
General Tab	
General Group	
Total APB Masters	Specifies the number of APB masters that are connected to this Soft IP.
Total APB Slaves	Specifies the number of APB slaves that are connected to this Soft IP.
Master Address Width(bits) (M_ADDR_WIDTH)	Specifies the bit width of the all PADDR signals.
Full Address Decoding up to 1kB	Selects the decoder implementation. Refer to section for more information.
Data Bus Width(bits) (DATA_WIDTH)	Specifies the bit with of the all PWDATA and PRDATA signals.
Registered Output	Unchecked: Output register is disabled (bypassed) Checked: Output register is enabled – this option is currently not supported
Main Settings Tab	
Slave <N> Settings Group	
Base Address <N>	Specifies base address for APB slave <N>. If [*Full Address Decoding up to 1kB* = Checked]: The value must be aligned to 1 kB If [*Full Address Decoding up to 1kB* = Unchecked]: The value must be aligned to (or multiple of) the value of Address Range rounded up to power of 2.
Address Range <N>	Specifies address range for APB slave <N>. If [*Full Address Decoding up to 1kB* = Checked]: The value must be multiple of 1 kB.
Master Priority Settings Tab	
Slave <N> Settings Group	
Arbiter Scheme	Specifies the arbitration scheme to be implemented for APB slave <N>.
Master <M> Priority	Specifies priority index of APB master <M> to access APB slave <N>. [0]: disabled connection – master cannot access the slave [1]: Highest priority … [31]: Lowest priority

Notes:

- <N> - Slave index [0,1,…,(*Total APB Slaves*)-1]
- <M> - Master index [0,1,…,(*Total APB Masters*)-1]

2.4. Use Models

The APB Interconnect module connects one or more APB master devices to one or more APB slave devices. Each connected APB master device could either be:

- A device that originates APB transactions (endpoint master) or
- A master interface of an upstream APB Interconnect core being cascaded

Similarly, each connected APB slave device could either be:

- The final target of APB transactions (endpoint slave) or
- A slave interface of a downstream APB Interconnect core being cascaded

In general, APB Interconnect Module can be configured for the following connectivity patterns:

- Single Master Interconnect – refer to the Single Master Interconnect section.
- Multi-Master Interconnect – refer to the Multi-Master Interconnect section.

An example of Single Master Interconnect application is shown in Figure 2.3. The arrows in the figure are APB interface connections, where *M* stands for an APB master port, and *S* stands for an APB slave port. In this example, AHB-Lite to APB (AHBL2APB) Bridge is the endpoint APB master. In an embedded system, this module usually converts the register access AHB-Lite transaction to APB. The APB master must be registered output for better routing in the FPGA fabric.

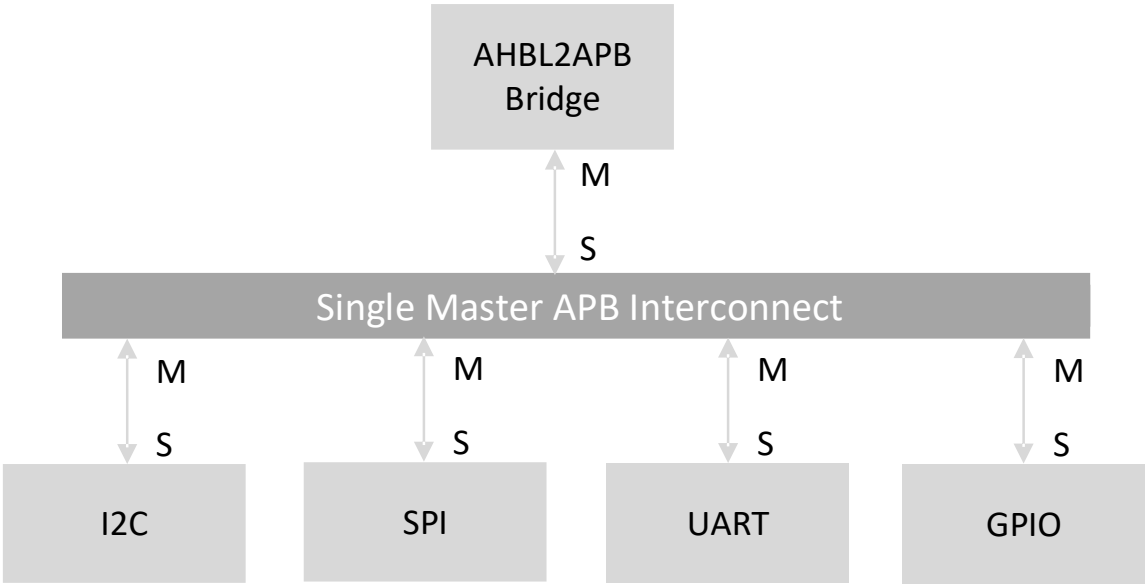

Figure 2.3. Example of Single Master Interconnect Application

An example of a Multi-Master Interconnect application is shown in Figure 2.4. This is similar to Figure 2.3 with the addition of the I2CS2APB Bridge. In this example, the I2CS2APB Bridge may be used to perform read and write access to the peripheral registers through the I^2C interface that is connected to the external I^2C Master. If the two APB masters attempt to access the slaves (either the same slave or a different slave) at the same time, arbitration occurs and only the granted master gains access to the target slave. This master-side arbitration optimizes resource utilization at the expense of reduced performance. This is acceptable for APB interconnect since APB is not intended for high performance application.

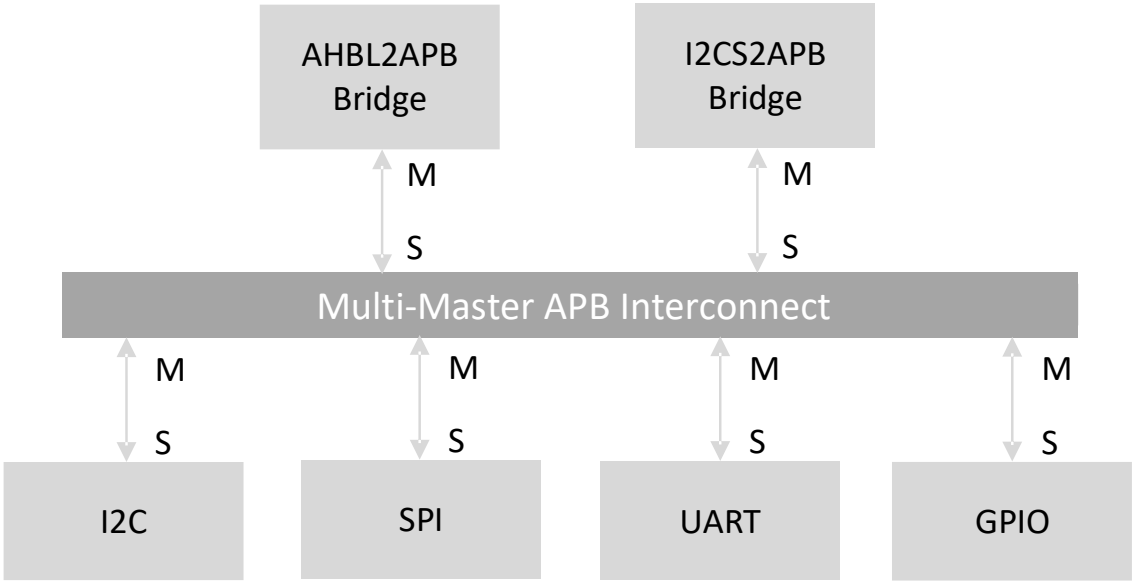

Figure 2.4. Example of Multi-Master Interconnect Application

2.5. Single Master Interconnect

The Single Master Interconnect described in this document is a single master to multiple slave configuration of the Lattice Semiconductor APB Interconnect Module. The bus interconnect logic is encapsulated inside the soft IP, which consists of an address decoder, a slave-to-master multiplexor, and a default slave. This is shown in Figure 2.5. The master-to-slave APB signals (PENABLE, PWRITE, PWDATA, PADDR), not including PSELx, are connected directly from the master to all the slaves. The PADDR also goes to the Decoder component, which generates individual PSELx signals to each slaves. The slave treats the transaction as valid when its PSELx input is asserted. When no slave is selected, the PSELx going to the Default Slave asserts. In this case, the Default Slave sends an error response to the multiplexor. The Multiplexor uses the PSELx signals from the Decoder to select the slave to master signals (PREADY, PRDATA, PSLVERR) from the target slave and route it to the master.

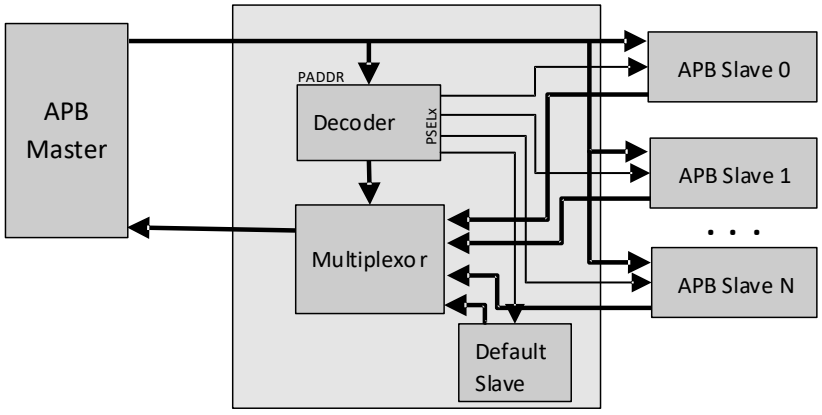

Figure 2.5. Functional Block Diagram of Single Master Interconnect

2.5.1. Decoder

The Decoder component performs address decoding for each bus transfer and provides a select signal for each slave on the bus. Decoding is done by comparing the appropriate address bits with the user-provided memory-map (*Base Address* and *Address Range*) settings during configuration. This is shown in Figure 2.6. The memory map is static setting; it cannot be changed during operation. During a bus transfer, the select signal goes high for a single slave involved in the transfer. The decoder also sends the PSELx signals to the multiplexor.

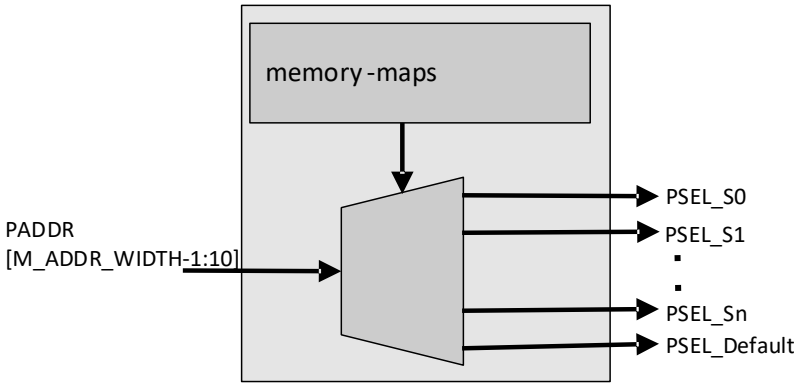

Figure 2.6. Block Diagram of AHB-Lite Decoder

The minimum address space that can be allocated to a single slave is 1 kB. This is done to be consistent with AHB-Lite Interconnect and to reduce the combinatorial delay of address decoding. When configuring the IP, The slave *Address Range* attribute value must be in multiple of 1 kB.

The PSELx signal is a combinatorial decode of the high-order address signals. This is done by comparing the higher bits of the address signal with the *Base Address* and *Address Range* settings. The behavior of decoder is controlled by the *Full Address Decoding up to 1 kB* attribute as follows:

- [*Full Address Decoding up to 1kB* is Checked]: PSEL signal asserts if the following conditions are met:
- apb_sxx_paddr_slv_i[*M_ADDR_WIDTH* – 1:10] >= *Base Address*[*M_ADDR_WIDTH* – 1:10]
- apb_sxx_paddr_slv_i[*M_ADDR_WIDTH* – 1:10] <= (Max Address + Address Range)[*M_ADDR_WIDTH* – 1:10]
- [*Full Address Decoding up to 1kB* is Unchecked]: PSEL signal asserts if the following condition is met:
- apb_sxx_paddr_slv_i[*M_ADDR_WIDTH* – 1:XBIT] == *Base Address*[*M_ADDR_WIDTH* – 1: XBIT]
  Wherein XBIT = Round_up($\log_2$(*Address Range*))

When *Full Address Decoding up to 1 kB* is Unchecked, the *Address Range* is not in used in comparison because it is in a power of 2 value. Thus, the behavior of the interconnect is undefined if this attribute is not in a power of 2 value.

The user-defined memory maps of the slaves are parameters to the decoder IP and are used to select the appropriate slave. If a system design does not contain a completely filled memory map, a default slave is selected when a transfer is attempted to a nonexistent address location.

2.5.2. Default Slave

When a transfer is attempted to an address that does not map to a slave, the Default Slave provides an error response to the multiplexor. An error response is the assertion of the PSLVERR signal when PENABLE and PREADY are both asserted. The PRDATA signal from Default Slave is fixed to 0.

2.5.3. Multiplexor

A Multiplexor component is a slave-to-master multiplexor. It selects the PRDATA, PREADY, and PSLVERR signals from the slaves going to the master as shown in Figure 2.7. The Multiplexor registers the PSELx signals from the Decoder and uses it to route the appropriate signals from the selected slave to the master. The registering of the PSELx signal is necessary to break the combinatorial delay. This is important because the PSELx signals are part of the critical path.

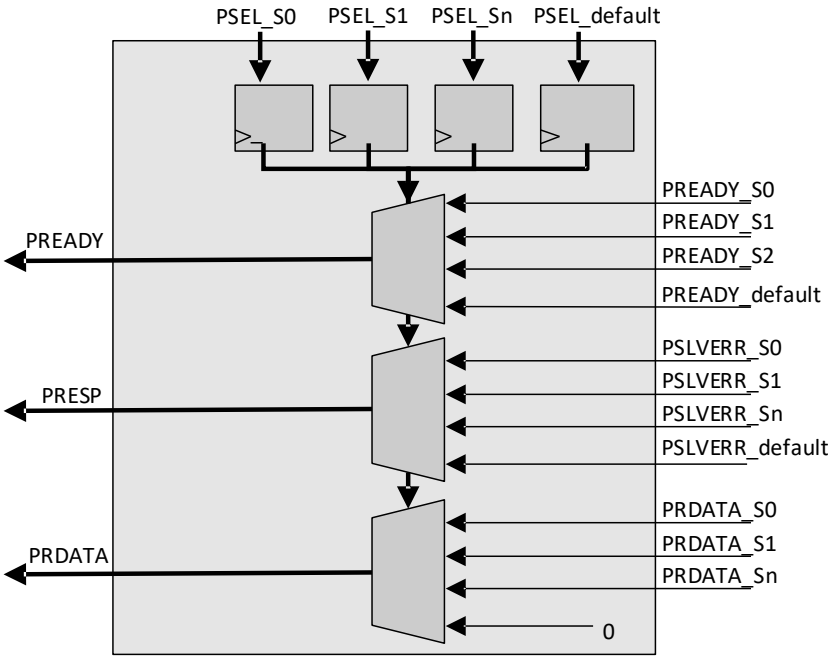

Figure 2.7. Block Diagram of APB Multiplexor

2.6. Multi-Master Interconnect

The Multi-Master Interconnect described in this document is a single master to multiple slave configuration of the Lattice Semiconductor APB Interconnect Module. It implements master-side arbitration as shown in Figure 2.8. All the APB masters go to the Arbiter Mux, which selects only one transaction to go through the Single Master Interconnect. This means that when two or more APB masters perform transaction to any slaves at the same time, arbitration takes place. Only the granted master can access any of the slaves at a given time. You can specify a different arbitration scheme for each slave, which is used to select a master during bus contention. Currently, there are two arbitration scheme options:

- Round-robin (default) – Each master is serviced in round-robin manner, giving each master equal access to the slave.
- Fixed priority – High priority masters are always given access to the slave in preference over lower priority masters.

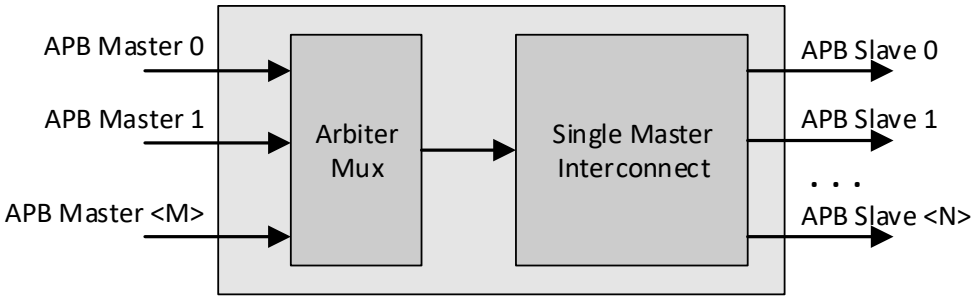

Figure 2.8. Block Diagram of Multi-Master Interconnect

2.6.1. Arbiter Mux

The Arbiter Mux receives an APB interface from each master and routes one APB interface to the slave as shown in Figure 2.9. The Arbiter component arbitrates any potential contention between masters. When PSELx is high from multiple masters, the Arbiter generates the grant signal to the Multiplexors. The Master to Slave Multiplexor routes the APB signals from the granted master to the slave. These signals are PADDR, PSELx PENABLE, PWRITE, and PENABLE. On the other hand, the Slave to Master multiplexor routes the PREADY, PRDATA, and PSLVERR signals to the granted master. The masters that are not granted have their PREADY input low, thus, the transaction is pended. The pended master that is recently granted is already in access state. The FSM generates the necessary IDLE and SETUP states of the APB transaction for the newly granted master.

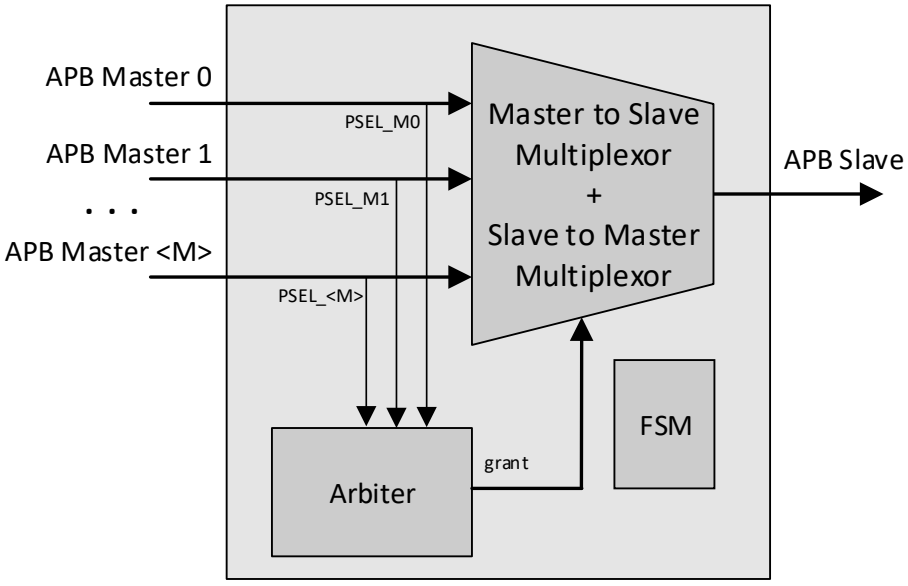

Figure 2.9. Block Diagram of APB Arbiter Mux

References

- MachXO2 FPGA Web Page in latticesemi.com
- MachXO3 FPGA Web Page in latticesemi.com
- MachXO3D web page at www.latticesemi.com
- Mach-NX web page at www.latticesemi.com
- CrossLink-NX web page at www.latticesemi.com
- Certus-NX web page at www.latticesemi.com

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.2, May 2021

Section	Change Summary
Introduction	Updated Table 1.1 to add MachXO2 and MachXO3 as supported FPGA family.
References	Updated content to add reference for MachXO2 and MachXO3.

Revision 1.1, December 2020

Section	Change Summary
Introduction	Modified second paragraph and added Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation.
Functional Description	Updated footnote markers in Table 2.2. Attributes Table. Removed footnote markers from Registered Output and Arbiter Scheme in Table 2.3. Attributes Description.
References	Updated this section.

Revision 1.0, May 2020

Section	Change Summary
All	Initial release.

www.latticesemi.com