AHB-Lite to APB Bridge Module - Lattice Propel Builder

User Guide

FPGA-IPUG-02053-1.2

May 2021

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
FPGA	Field Programmable Gate Array
RTL	Register Transfer Level

1. Introduction

The Lattice Semiconductor AHB-Lite to APB Bridge Module provides an interface between the high-speed AHB-Lite and the low power APB. In many applications, the AHB-Lite system runs on a higher frequency clock with the APB system. This module has an optional clock crossing bridge, which can be enabled during IP configuration.

The design is implemented in Verilog HDL. The IP can be configured and based on Table 1.1.

Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation

Supported FPGA Family	IP Configuration and Generation	IP Implementation (Synthesis, Map, Place and Route)
MachXO2™	Lattice Propel™ Builder software	Lattice Diamond® software
MachXO3™	Lattice Propel Builder software	Lattice Diamond software
MachXO3D™	Lattice Propel Builder software	Lattice Diamond software
Mach™-NX	Lattice Propel Builder software	Lattice Diamond software
CrossLink™-NX	Lattice Propel Builder software	Lattice Radiant™ software
Certus™-NX	Lattice Propel Builder software	Lattice Radiant software

1.1. Features

The key features of the AHB-Lite to APB Bridge Module include:

- Compliance with AMBA 3 AHB-Lite Protocol v1.0 and AMBA 3 APB Protocol v1.0
- Data Bus width of up to 32 bits [8, 16, 32]
- Address width of up to 32-bits [11,12,...,32]
- Support of optional clock domain crossing bridge
- Registered output

2. Functional Description

2.1. Overview

The Lattice Semiconductor AHB-Lite to APB Bridge Module is used for interfacing one AHB-Lite Master and one APB Slave. When interfacing to multiple APB Slaves, this IP should be used together with an APB interconnect. The read and write transfers on the AHB-Lite are converted into equivalent transfers on the APB. In a single clock application, the bridge has enough write buffers to sustain continuous write access without additional wait states. However, for read access, the bridge adds two waits states. This is due to the output register in both the AHB-Lite side and the APB side. When the optional clock domain crossing bridge is enabled, the bridge is added in the APB side.

2.2. Interface Description

Figure 2.1 shows the interface diagram of the AHB-Lite to APB Bridge Module. The diagram shows all the available ports for the IP core.

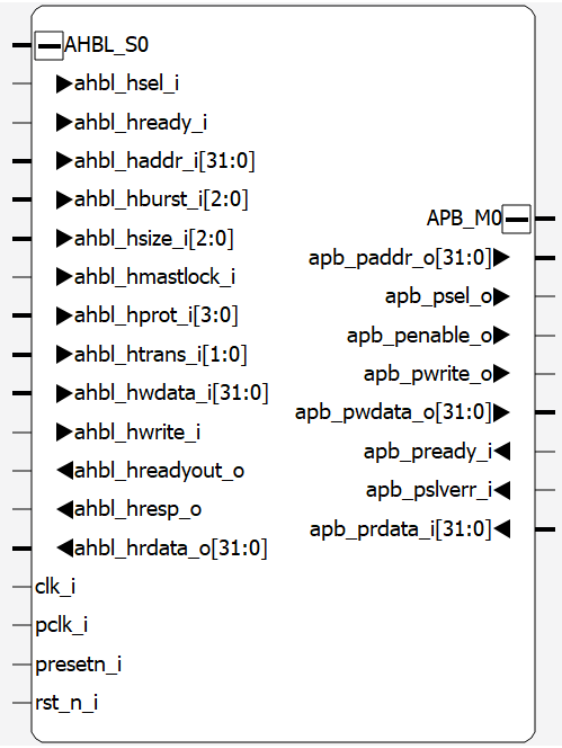

Figure 2.1. AHB-Lite to APB Bridge Module Interface Diagram

Table 2.1. AHB-Lite to APB Bridge Module Signal Description

Pin Name	Direction	Width (Bits)	Description
Clock and Reset			
clk_i	In	1	Clock input for AHB-Lite I/F If the APB Clock Enable attribute is unchecked, this signal also clocks the APB I/F.
pclk_i	In	1	Clock input for APB I/F This is only present when the APB Clock Enable attribute is checked.
rst_n_i	In	1	Asynchronous active LOW reset input for AHB-Lite I/F Reset negation should be synchronous to clk_i. If the APB Clock Enable attribute is unchecked, this signal also resets APB I/F.
presetn_i	In	1	Asynchronous active LOW reset input for APB I/F Reset negation should be synchronous to pclk_i.
AHB-Lite Master Interface (AHBL_S0)			
ahbl_hsel_slv_i	In	1	Slave select
ahbl_haddr_slv_i	In	*ADDR_WIDTH*	Adddress
ahbl_hburst_slv_i	In	3	Burst type (SINGLE, INCR, INCR4/8/16) This signal is unused; all transactions are treated as SINGLE.
ahbl_hsize_slv_i	In	3	Transfer size (8/16/32/64/128/256/512/1024) This signal is unused; the actual transfer size is *DATA_WIDTH*.
ahbl_hmastlock_slv_i	In	1	Current transfer is part of a locked transfer. This signal is unused.
ahbl_hprot_slv_i	In	4	Protection control This signal is unused.
ahbl_htrans_slv_i	In	2	Transfer type of the current transfer (IDLE/BUSY/NSEQ/SEQ)
ahbl_hwdata_slv_i	In	*DATA_WIDTH*	Write data bus
ahbl_hwrite_slv_i	In	1	This indicates access direction: Write = 1, Read = 0.
ahbl_hready_slv_i	In	1	This indicates transfer completion.
ahbl_hready_slv_o	Out	1	This indicates transfer completion. This signal is driven low by the slave to extend the transfer.
ahbl_hresp_slv_o	Out	1	Slave response (OKAY/ERROR)
ahbl_hrdata_slv_o	Out	*DATA_WIDTH*	Read data bus
APB Slave Interface (APB_M0)			
apb_psel_o	Out	1	Select signal This indicates that the slave device is selected and that a data transfer is required.
apb_paddr_o	Out	*ADDR_WIDTH*	Address signal
apb_pwdata_o	Out	*DATA_WIDTH*	Write data signal
apb_pwrite_o	Out	1	Direction signal Write = 1, Read = 0
apb_penable_o	Out	1	Enable signal This indicates that the second and subsequent cycles of an APB transfer.
apb_pready_i	In	1	Ready signal This indicates transfer completion. Slave uses this signal to extend an APB transfer.
apb_pslverr_i	In	1	Error signal This indicates a transfer failure. In case APB Slave does not have this signal, it should be tied to 1'b0.
apb_prdata_i	In	*DATA_WIDTH*	Read data signal

2.3. Attributes

Table 2.2 provides the list of user-configurable attributes for the AHB-Lite to APB Bridge Module. The attribute values are specified using the IP core Configuration user interface in the Propel Builder software as shown in Figure 2.2.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
Address Width(bits) (ADDR_WIDTH)	11–32	32	—
Data Bus Width(bits) (DATA_WIDTH)	8, 16, 32	32	—
APB Clock Enable	Checked, Unchecked	Unchecked	—

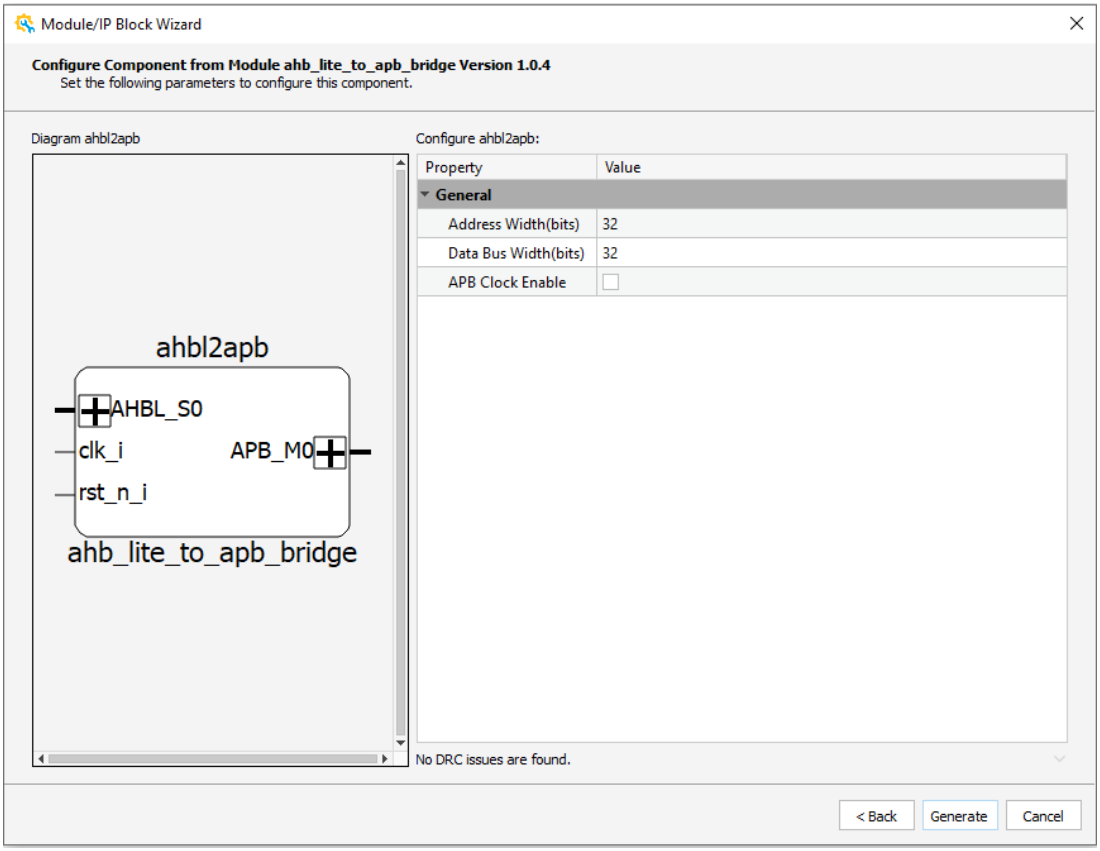

Figure 2.2. AHB-Lite to APB Bridge Module Configuration User Interface

Table 2.3. Attributes Description

Attribute	Description
Address Width(bits)	Specifies the bit width of address bus signals.
Data Bus Width(bits)	Specifies the bit with of ahbl_hwdata_slv_i and ahbl_hrdata_slv_o signals.
APB Clock Enable	Enables pclk_i and presetn_i signals as well as the clock domain crossing (CDC) logic generation. When enabled, the CDC logic is added in the APB side. Unchecked: pclk_i and presetn_i signals and CDC logic are generated Checked: pclk_i and presetn_i signals and CDC logic are generated

References

- MachXO2 FPGA Web Page in latticesemi.com
- MachXO3 FPGA Web Page in latticesemi.com
- MachXO3D FPGA Web Page in latticesemi.com
- CrossLink-NX Web Page in latticesemi.com
- Certus-NX Web Page in latticesemi.com
- Mach-NX FPGA Web Page in latticesemi.com

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.2, May 2021

Section	Change Summary
Introduction	Updated Table 1.1 to add MachXO2 and MachXO3 as supported FPGA family.
References	Updated content to add reference for MachXO2 and MachXO3.

Revision 1.1, November 2020

Section	Change Summary
Introduction	Added Table 1.1.
Functional Description	Updated Figure 2.2.
References	Updated content to remove reference links for Lattice Propel and Lattice Diamond user guide; and to add reference links for Mach-NX, CrossLink-NX and Certus-NX web page.

Revision 1.0, May 2020

Section	Change Summary
All	Initial release

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