



Designing Power Manager II with PAC-Designer®

PAC-Designer Tutorial

Introduction

Welcome to the *Designing Power Manager II with PAC-Designer* tutorial!

This tutorial is intended for new users or those who use PAC-Designer software infrequently. This tutorial will help you to implement multiple designs into a variety of Power Manager devices to illustrate key solutions such as power sequencing, monitoring, and supervision. Along the way you will perform analysis, configure the software to implement the logic into the physical device, and review output reports as you make progress. It covers the most common procedure and software options so you'll have a base of understanding before you design more sophisticated applications.

This tutorial shows you how to use several processes, tools, and reports of the PAC-Designer software suite to program digital and analog elements of the ispPAC®-POWR1220AT8 device to meet the sequencing and management needs of a simple circuit board with a variety of voltage rails and ICs.

Learning Objectives

When you have completed this tutorial, you should be able to:

- Find major functions within the PAC-Designer user interface.
- Use PAC-Designer to create a POWR1220AT8 project.
- Configure input, driver, and output pins with the Schematic Editor.
- Define power management logic with the LogiBuilder feature.
- Compile, simulate, and implement the project.

Time to Complete This Tutorial

The time to complete this tutorial is about 60 minutes.

System Requirements

The following hardware/software configuration is required to complete the tutorial.

- PAC-Designer Version 4.96 or later
- PAC-POWR1220AT8-EV evaluation board (optional)

About the Tutorial Design

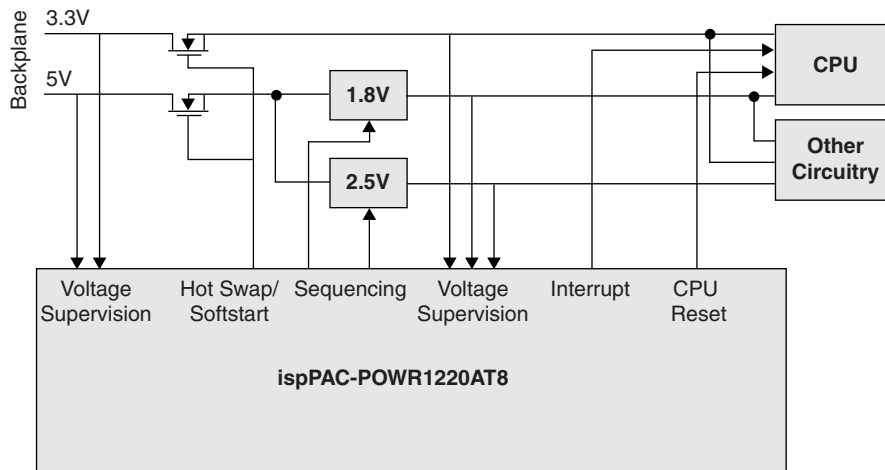
The tutorial design demonstrates a Power Manager II device in an application where it supplies the following management features:

- Soft Start
- Sequence
- Generate CPU Reset
- Interrupt CPU on Supply Faults
- Turn Supplies Off

Figure 1 illustrates the application scenario where the following power supply rails are managed:

- 5V (10% tolerance) and 3.3V (5%) supplied from a backplane.
 - 3.3V (5%) after soft start used for I/O supply.
 - 2.5V (5%) used for other board ICs.
 - 1.8V (3%) used for CPU core voltage.
-

Figure 1. The Tutorial Design

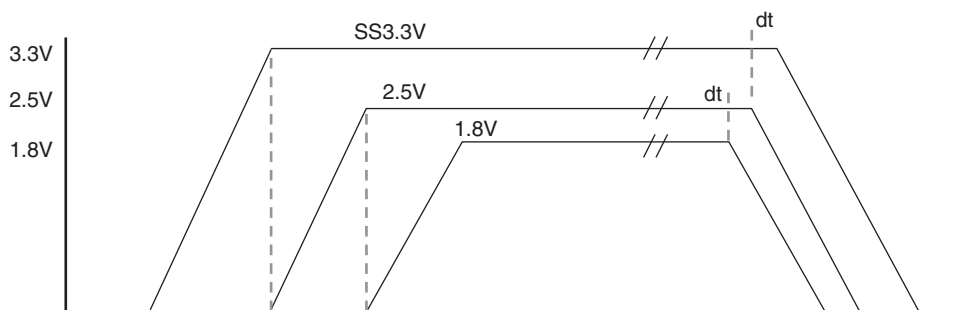


The power sequencing required is:

- 3.3V for I/O
- 2.5V supply rail
- 1.8V supply rail

Figure 2 illustrates the voltage rails controlled by the POWR1220A8 IC in the schematic. Two softstart 3.3V and 5V rails are controlled with a MOSFET transistor and two 2.5V and 1.8V rails are sequenced based on the requirements of the Other Circuitry block. You will examine the logic to describe this scenario in a later task of the tutorial.

Figure 2. Sequencing Scenario



About the Tutorial Process Flow

You will use the basic PAC-Designer software process flow to create a POWR1220A8 programming file to implement the sample application. While the specific steps may vary across ispPAC device families, the tutorial follows a typical flow.

1. Start a new ispPAC-POWR1220AT8 design
2. Configure the Analog Inputs block for voltage monitoring
3. Configure the Digital Input block for control inputs and status monitoring
4. Configure the High Voltage Outputs block for MOSFET driver outputs
5. Configure Logic Outputs block for sequencing and other control outputs

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6. Set the Clocks & Timers block parameters for delay and clock source configuration
7. Implement power management logic of the Sequence Controller block
8. Set up the I²C interface block
9. Save the design
10. Compile the design
11. Simulate the design
12. Print the design
13. Download the design into POWR1220AT8 Evaluation Board and verify operation (optional)

Recommended Reference Materials

The following reference materials are recommended for this tutorial.

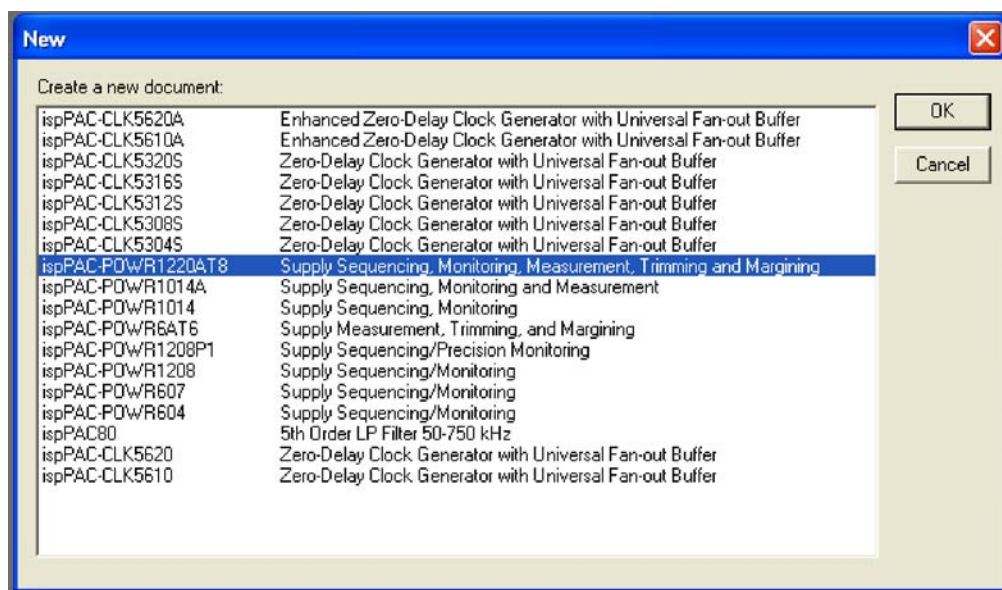
- ispPAC-POWR1220AT8 Data Sheet
- AN6065 - PAC-POWR1220AT8-EV Evaluation Board

Task 1: Start a New Design

In this task you will...

To create a new design:

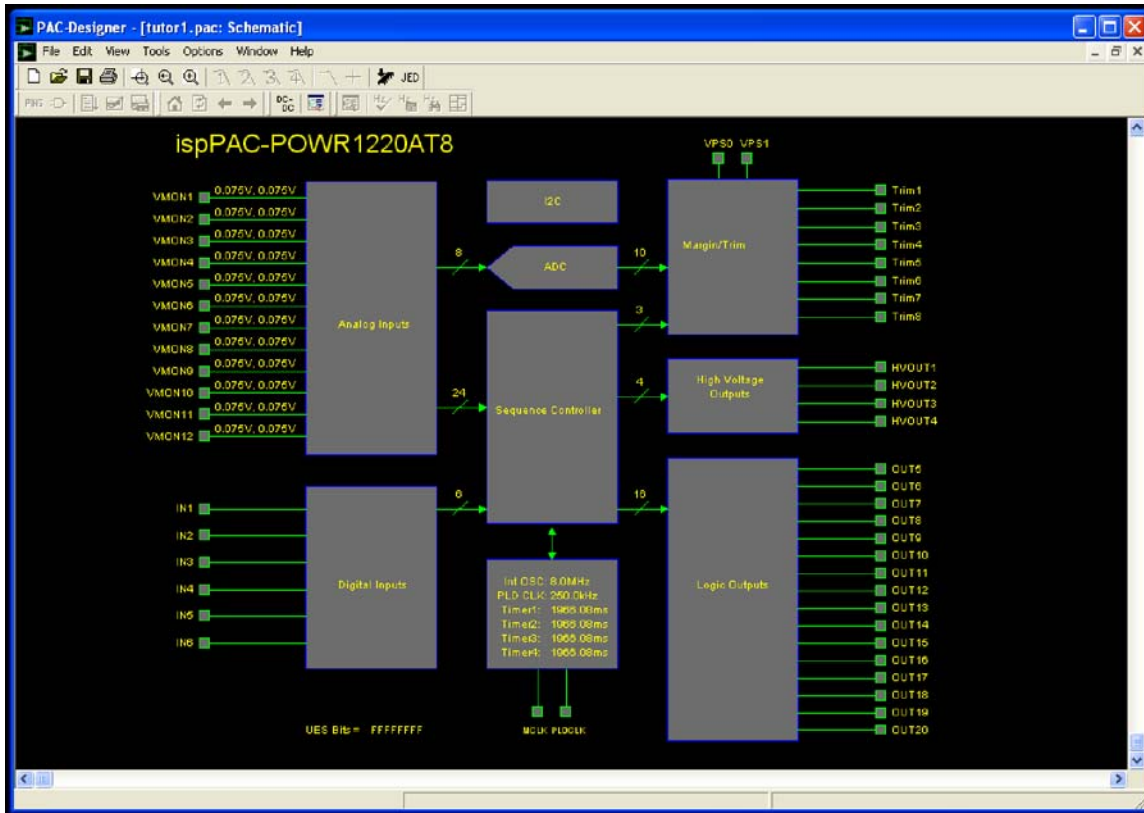
1. Start the PAC-Designer system, if it is not already running.
2. In the Project Navigator, choose **File > New...**
The New dialog appears.
3. From the document list, choose **ispPAC-POWR1220AT8 Supply Sequencing, Monitoring, Measurement, Trimming and Margining** and click **OK**.
The Save As dialog appears.



- Browse to the `<install_path>\Examples` directory, specify File name as `tutor1.pac`, and click **Save**.
tutor1.pac: Schematic appears.

The schematic editor of PAC-Designer is a hierarchical design entry tool that provides features to configure the device:

- Pull-down menus for selecting clock signaling specifications
- Dialogs to configure analog and digital functional blocks
- Schematic entry features to set internal connections and set parametric circuit values



Move the cursor over the block diagram. Notice the cursor changes shape as it moves over different regions. The cursor feedback feature indicates what actions you can take on a particular object or how to navigate between levels of hierarchy.

To navigate the design hierarchy:

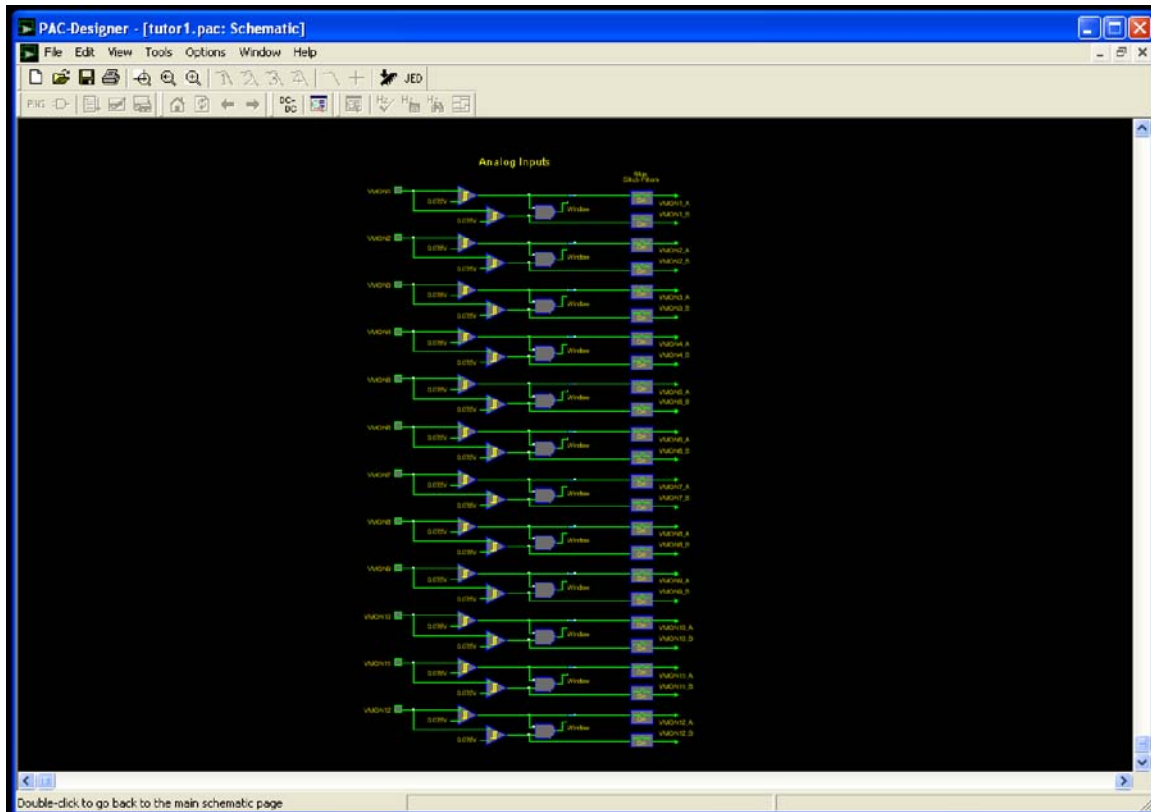
- Place the cursor over the **Analog Inputs** block of the diagram.
The cursor changes to a down arrow. This indicates the block can be pushed into for editing.
- Double-click the block.
The Analog Inputs schematic appears.
- Place the cursor towards the top of the schematic. When it changes to an up arrow, double-click.
The top-level schematic reappears.
- Place the cursor over the **I²C** block. When the cursor changes to an edit arrow with brackets, double-click.
The I²C Configuration dialog appears.
- Change the I²C address to 12h and click **OK**.

Task 2: Configure Voltage Monitoring Inputs

In this task you modify the Analog Inputs block of the POWR1220AT8 to set voltage threshold, specify net names, enable window comparison, and glitch filter options. In the application example, five voltage rails are supervised: 3.3V and 5V from the backplane, a hot-swap/softstart 3.3V, and sequenced 1.8V and 2.5V DC supplies used by the CPU and Other Circuitry blocks of the example circuit.

To edit the Analog Inputs block:

1. Place the cursor over the Analog Inputs block of the diagram and double-click. The Analog Inputs schematic appears.



2. Place the cursor over the schematic until it appears as an edit arrow with brackets. Double-click. The Analog Input Settings dialog appears.

The Analog Input Dialog Box allows you to define the programming of each POWR1220 analog input pin used for voltage monitoring.

Schematic Net Name - a user-defined name to be used for voltage rail to be monitored.

Logical Signal Name - a user-defined name to be assigned for the voltage monitor comparator circuit outputs that drive the Sequence Controller block.

Monitoring Type - programs the Over-Voltage (OV) threshold or Under-Voltage (UV) threshold type for each Logical Signal. The Monitoring Type setting ensures that hysteresis is applied after the monitored voltage crosses the threshold to prevent rapid switching if a monitored signal drifts around the threshold value.

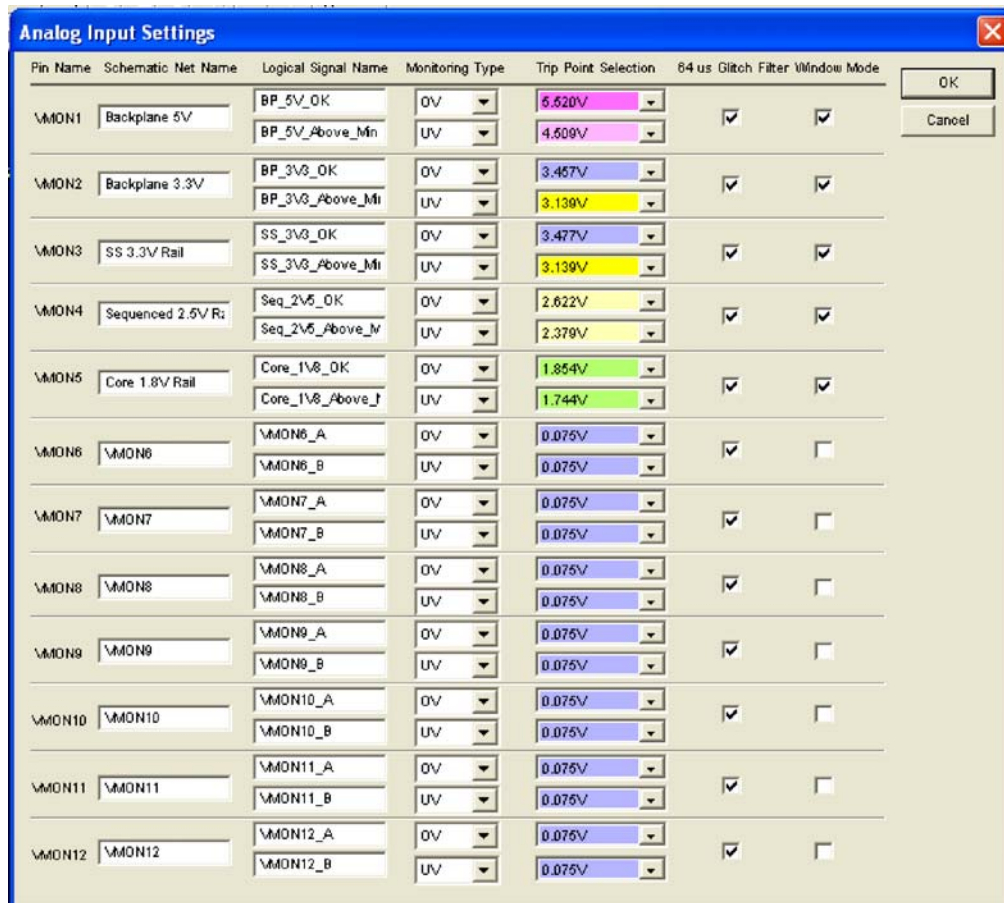
Trip Point Selection - a list of 368 pre-defined trip point voltages (5.73V to 0.668V and 75mV) related to each Logical Signal Name.

64µs Glitch Filter - an optional flag that causes events shorter than 64µs to be ignored. Enable if the monitored power supply is noisy.

Window Mode - enables the window comparator logic. Window Mode should be enabled when:
Lower Threshold < Input Voltage < Upper Threshold

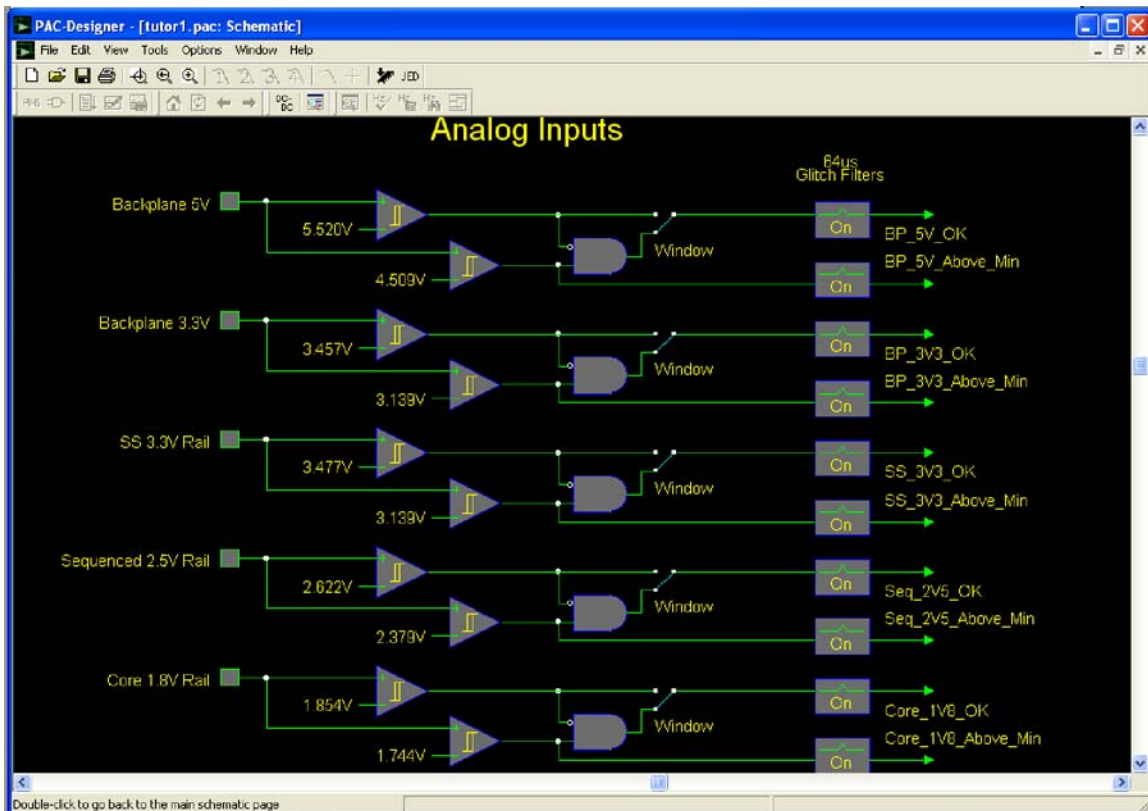
- Enter the Schematic Net Name and Logical Signal Name fields and select the Trip Point Selection voltages for each input pin using the table below. To save typing, use copy/paste from this document into the respective text fields of the dialog.

Pin Name	Schematic Net Name	Logical Signal Names	Monitoring Type	Trip Point Selection	64µs Glitch Filter	Window Mode
VMON1	Backplane 5V	BP_5V_OK	OV	5.520V	✓	✓
		BP_5V_Above_Min	UV	4.509V		
VMON2	Backplane 3.3V	BP_3V3_OK	OV	3.457V	✓	✓
		BP_3V3_Above_Min	UV	3.139V		
VMON3	SS 3.3V Rail	SS_3V3_OK	OV	3.477V	✓	✓
		SS_3V3_Above_Min	UV	3.139V		
VMON4	Sequenced 2.5V Rail	Seq_2V5_OK	OV	2.622V	✓	✓
		Seq_2V5_Above_Min	UV	2.379V		
VMON5	Core 1.8V Rail	Core_1V8_OK	OV	1.854V	✓	✓
		Core_1V8_Above_Min	UV	1.744V		



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4. Click **OK**.
The Analog Inputs schematic appears.
5. Choose **View > Zoom In Select**.
The cursor changes to a Zoom shape.
6. Select the area of the first five analog input pins.
The area selected fills the schematic view.



Settings you specified in the Analog Input Settings dialog now appear annotated on the schematic:

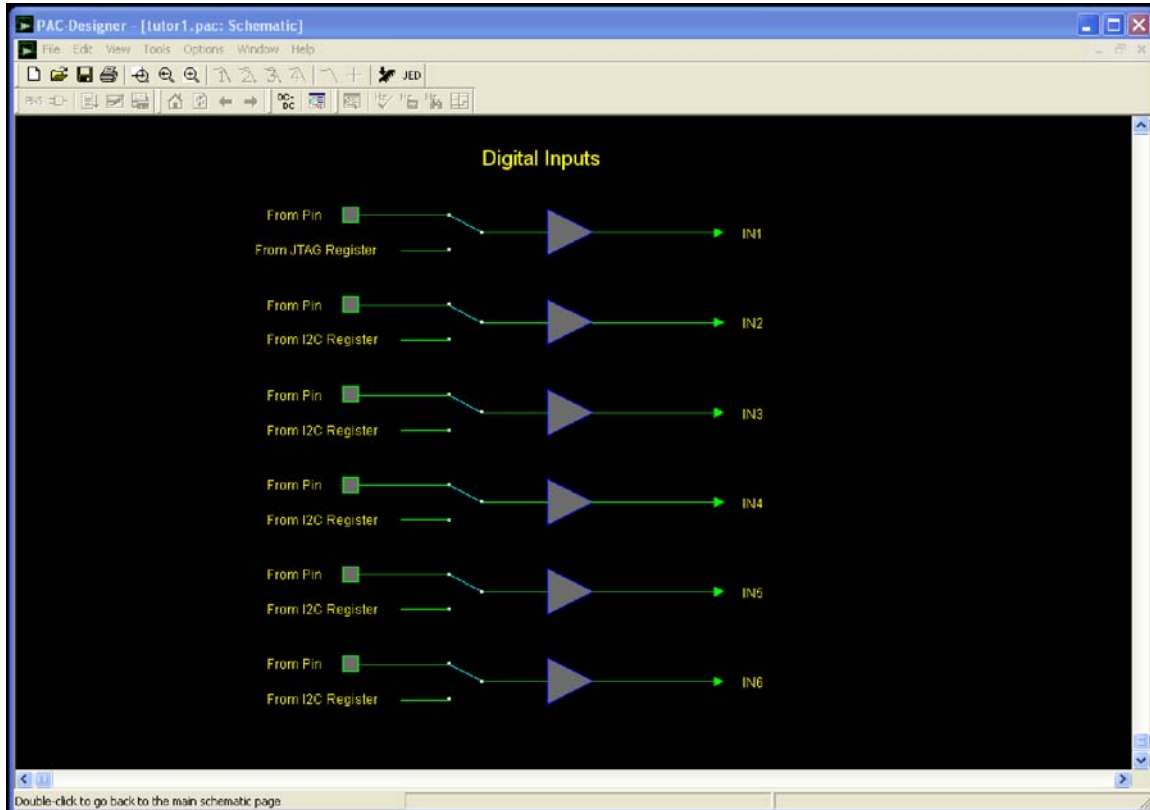
- Schematic Net Names appear as input names to the left of the pins
 - Trip Point voltages appear as inputs to each comparator pair
 - Window Mode settings appear as a switch
 - Enabled glitch filters appear with On notation
 - Logical Signal Names appear as output signals of the Analog Input block
7. Place the cursor towards the top of the schematic. When it changes to an up arrow, double-click.
The top-level schematic reappears.

Task 3: Configure Digital Input Pins

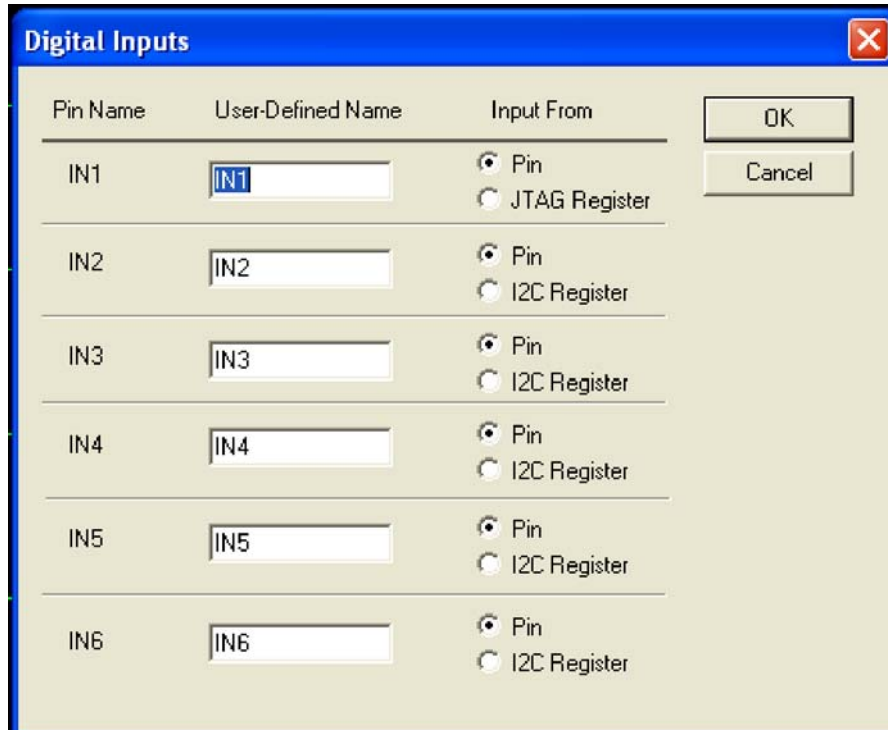
In this task you examine the digital input block of the POWR1220AT8 where you may specify user-defined pin names and input signal source as: input pin, JTAG register, or I²C register. The example design does not utilize any digital inputs so in the procedure below you will keep the default settings. You may skip to Task 4 without impacting the tutorial flow.

To edit the Digital Inputs block:

1. Place the cursor over the Digital Inputs block of the diagram and double-click. The Digital Inputs schematic appears.



- Place the cursor over the schematic until it appears as an edit arrow with brackets. Double-click. The Digital Input Settings dialog appears.



The Digital Inputs Dialog Box allows you to define the programming of each POWR1220 digital input pin. You may define signal names to be used in the documentation files and the Sequence Controller instructions. Inputs are controlled by an input pin or a register of the I²C or JTAG interface.

- Click **OK** to accept the defaults.
- Place the cursor towards the top of the schematic. When it changes to an up arrow, double-click. The top-level schematic reappears.

Task 4: Configure High Voltage Outputs

In this task you configure the high voltage output (HVOUT) block that serves as gate drivers for N-Channel MOSFET transistors on the circuit board. N-Channels MOSFETs may be necessary to turn on a single power rail at different instances during sequencing. In this tutorial design the HVOUT block drives two external MOSFETs to softstart the board.

To edit the High Voltage Outputs block:

- Place the cursor over the Digital Inputs block of the diagram and double-click. The High Voltage Outputs schematic appears.
- Place the cursor over the schematic until it appears as an edit arrow with brackets. Double-click.

The High Voltage Output Settings dialog appears. The High Voltage Output Settings Dialog Box allows you to define the programming of each of the POWR1220 analog output pins.

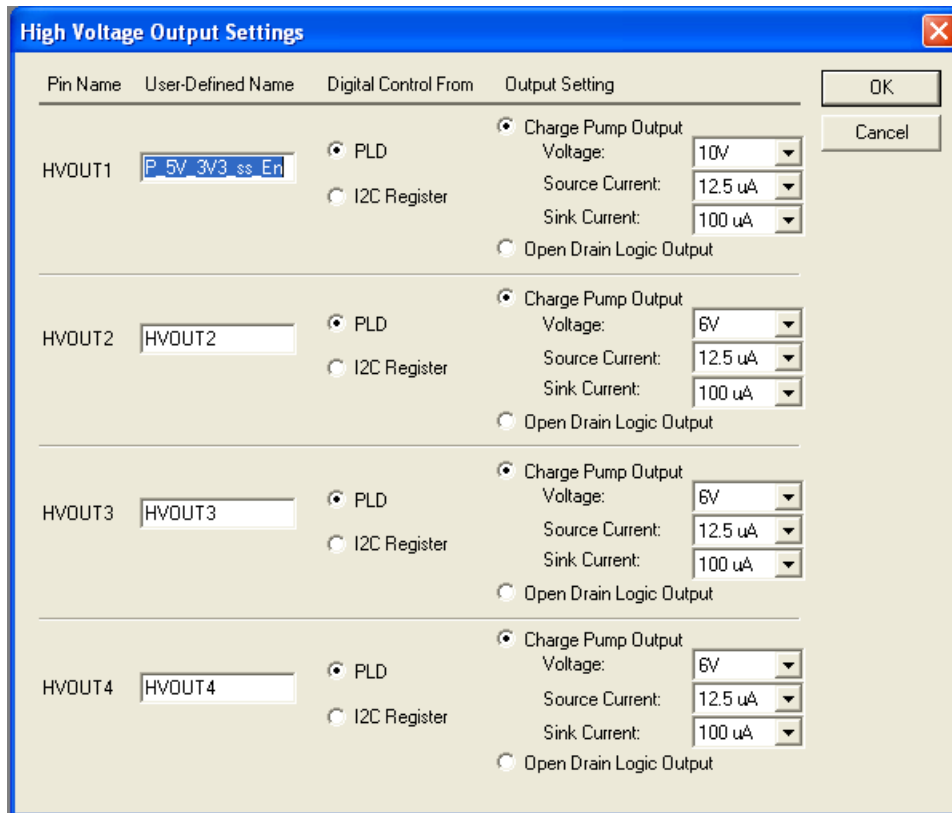
User-Defined Name - a user-defined name to be used for high voltage output pins.

Digital Control From - the source of the enable input of the FET driver. The pin may be controlled via the Sequence Controller logic or a register of the I²C interface.

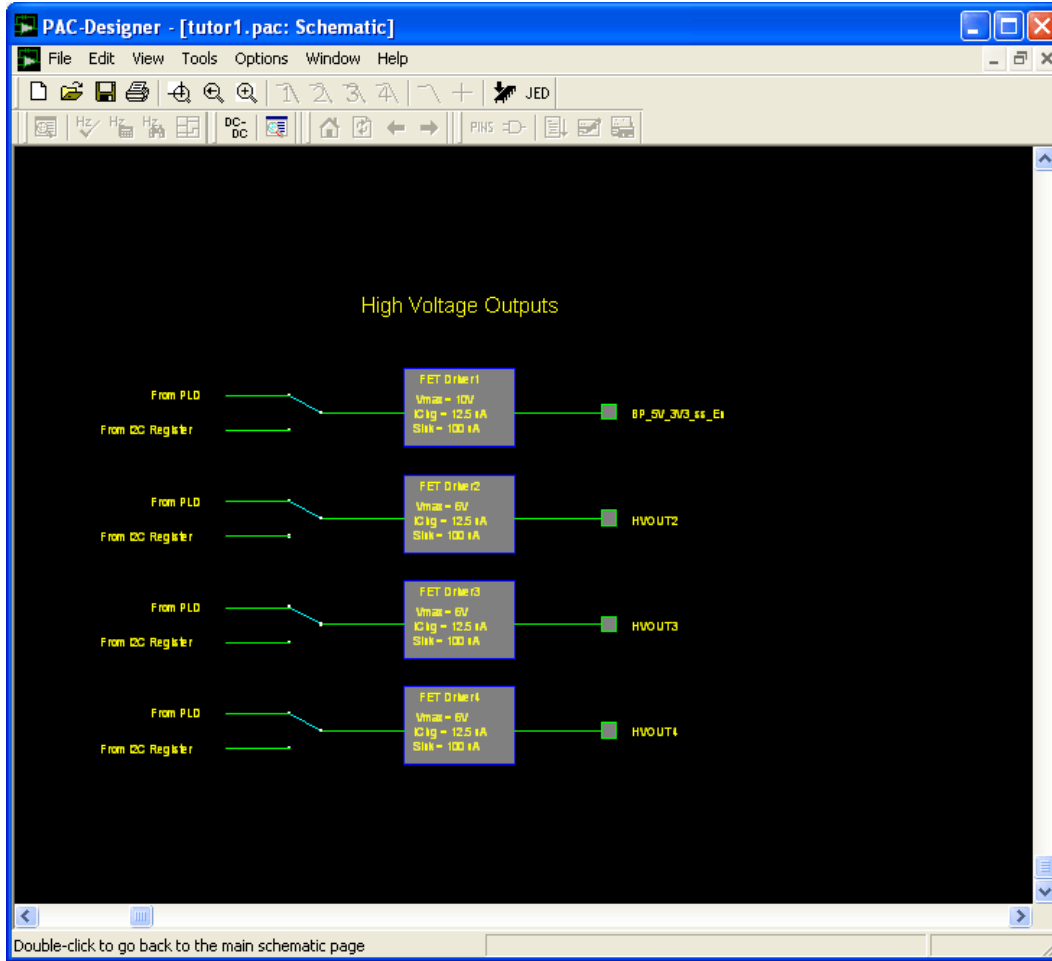
Output Setting - programs the output pin to operate as a charge pump for driving a MOSFET transistor or an open-drain logic mode. When set in the Charge Pump Output mode, you may specify the gate drive voltage, gate charge and discharge current.

- Enter the User-Defined Name and Digital Control From fields for each input pin using the table below. To save typing, use copy/paste from this document into the respective text fields of the dialog.

Pin Name	User-Defined Name	Digital Control From	Output Setting
HVOUT1	BP_5V_3V3_SS_En	PLD	Charge Pump Output Voltage: 10V Source Current: 25µA Sink Current: 100µA



- Click **OK**.
The High Voltage Outputs schematic is updated.



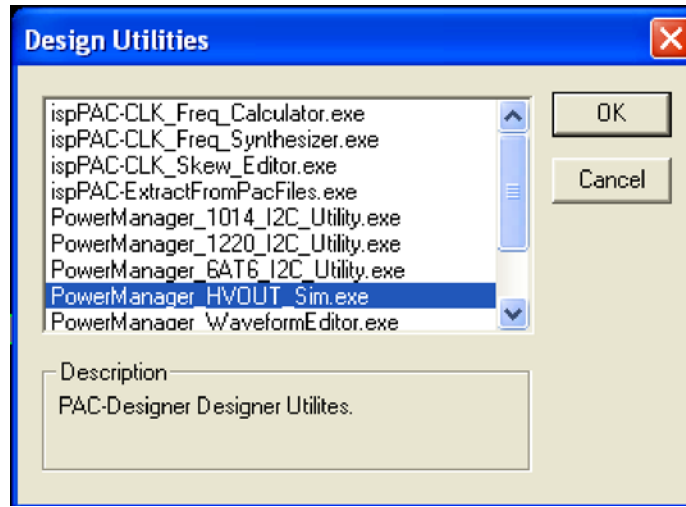
- Place the cursor towards the top of the schematic. When it changes to an up arrow, double-click. The top-level schematic reappears.

Task 5: Estimate MOSFET Turn-On Delay

In this task you use a design utility of PAC-Designer to simulate the rise time of a power supply driven by an N-Channel MOSFET and the HVOUT drivers on the Power Manager II device. This simulator uses parameters from the MOSFET data sheet to build a model then the circuit is simulated based on inputs from the user interface. These results are important as part of static timing analysis of the PCB or the sequencing of FPGA power supplies.

To edit the High Voltage Outputs block:

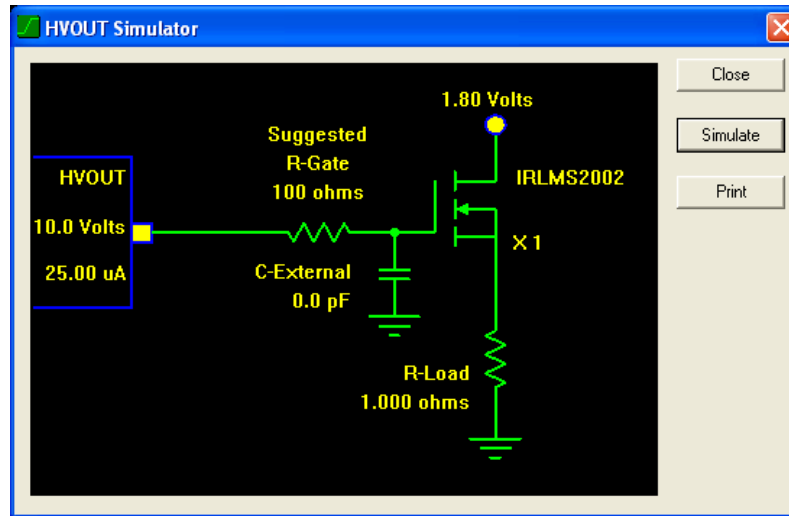
1. Choose **Tools > Design Utilities...**
The Design Utilities dialog appears.



2. Select **PowerManager_HVOUT_Sim.exe** from the list and click **OK**.
The HVOUT Simulator window appears.

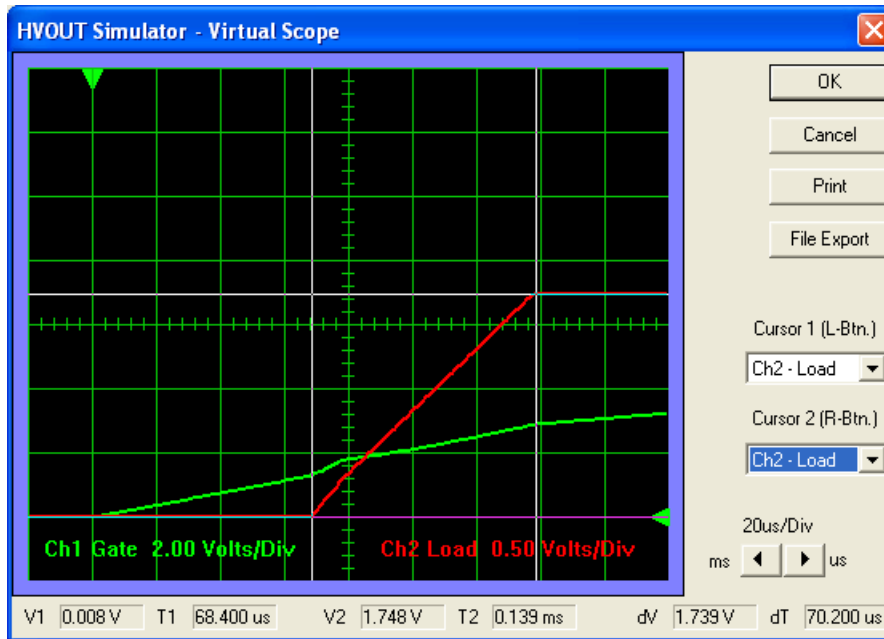
The simulator schematic includes the HVOUT block of the Power Manager II, the MOSFET transistor, resistors and capacitor of the PC board.

3. Place the cursor over the 0.50 μA field of the HVOUT block and double-click.
The HVOUT Current dialog appears.
4. Enter **25** into the μA (0.5 to 400) field and click **OK**.
The HVOUT block of the schematic is updated. The block now matches the HVOUT settings you set in Task 4: Configure High Voltage Outputs.



- Click the **Simulate** button.
The HVOUT Simulator - Virtual Scope window appears with a plot of the Ch1 Gate and Ch 2 Load waveforms.
- Click the time scale button until a resolution of **20 μ s/Div** appears.
The plot display resolution increases. To produce a comma separated value (CSV) export of the waveform plots, use the File Export button. This data can be easily imported into a spreadsheet program for additional analysis and formatting.

Select both Cursor 1 (L-Btn) to **Ch2 - Load** and Cursor 2 (R-Btn.) to **Ch2 - Load**.
Two white crosshair cursors appear on the plot.
- Click and hold the left mouse button then move the cursor.
The cursor follows the **Ch2 - Load** waveform plot.
- Release the mouse button at the transition point along the **Ch2 - Load** waveform plot where it begins to increase in voltage from 0V.
- Click and hold the right mouse button then more the cursor.
The cursor follows the Ch2 Load waveform plot.
- Release the mouse button at the point along the Ch2 Load waveform plot where it reaches a steady **1.748V**.



Note the dT value in the status bar. The turn-on delay time for Ch2 Load is about 71 μ s.

11. Click **OK**.
The HVOUT Simulator - Virtual Scope closes.
12. Click the **Close** button of the HVOUT Simulator window.

Note: See the Using the HVOUT Simulator Utility to Estimate FET Ramp Times (AN6070) Application Note for more details.

Task 6: Configure Logic Output Pins

In this task you examine the digital output block of the POWR1220AT8. You may specify user-defined pin names and each output signal source as the sequence controller PLD or a register of the I²C interface. Logic outputs are commonly used as enable signals for DC-to-DC supplies used in the power sequencing circuit of a FPGA. In the tutorial circuit the output signals serve as enable inputs to the 1.8V and 2.5V DC-DC supplies, a CPU interrupt to be enabled if any supply fails, a CPU reset to be enabled after the supply sequence completes or if any supply fails, and a “power good” signal (not pictured) to indicate the supply sequencing is complete.

To edit the Logic Outputs block:

1. Place the cursor over the Logic Outputs block of the diagram and double-click.
The Logic Outputs schematic appears.
2. Place the cursor over the schematic until it appears as an edit arrow with brackets. Double-click.
The Logic Outputs dialog appears.

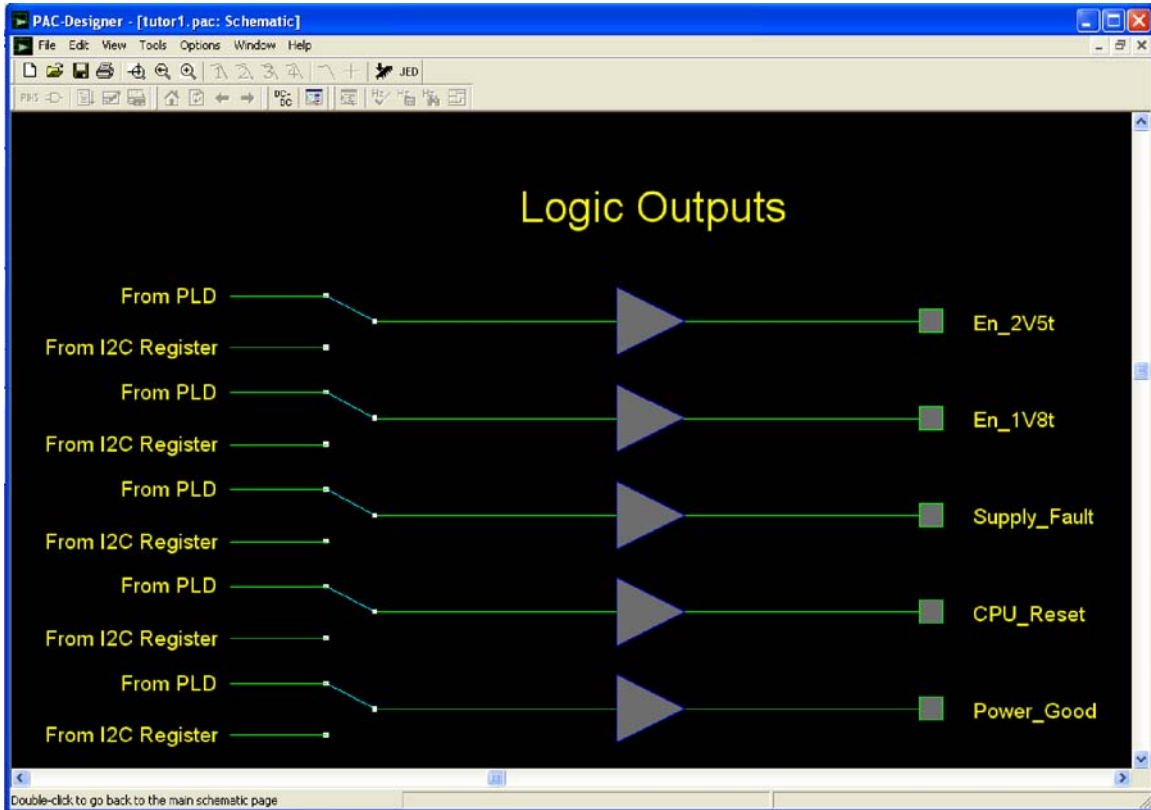
The Logic Outputs Dialog Box allows you to specify user-defined names to be used within the sequence controller PLD and specify the source of the digital control as the PLD or a register of the I²C interface.

- Enter the User-Defined Name and Digital Control From fields for each input pin using the table below. To save typing, use copy/paste from this document into the respective text fields of the dialog.

Pin Name	User-Defined Name	Digital Control From
OUT5	En_2V5	PLD
OUT6	En_1V8	PLD
OUT7	CPU_Reset	PLD
OUT8	Supply_Fault	PLD
OUT9	Power_Good	PLD



- Click **OK**.
The Logic Outputs schematic is updated.



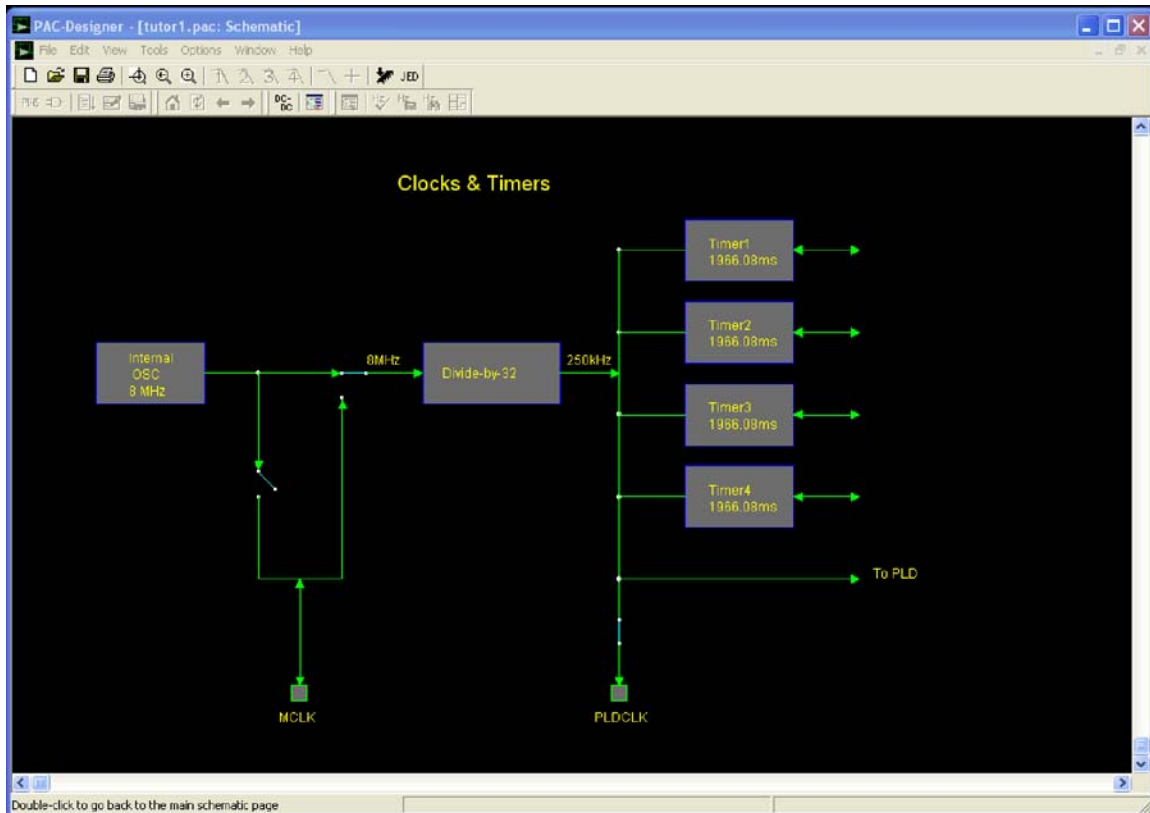
5. Place the cursor towards the top of the schematic. When it changes to an up arrow, double-click. The top-level schematic reappears.

Task 7: Set Timer Delay Parameters

In this task you set up the Clocks & Timers block of the POWR1220AT8. The POWR1220AT8 provides an internal oscillator that is used to drive the sequence controller PLD clock and timer circuits. The PLD clock has a prescaler that divides down the clock frequency to 250kHz. Timers can be set individually and range from 32 μ s to 1966ms.

To edit the Clock & Timers block:

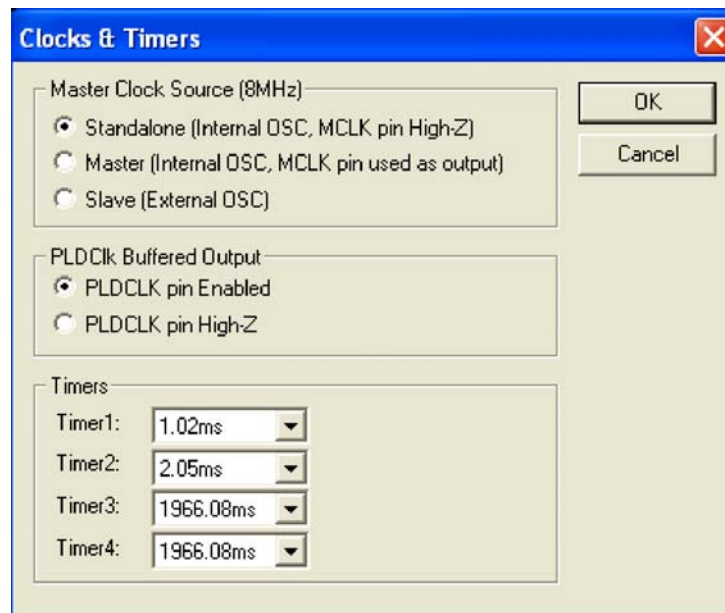
1. Place the cursor over the Clocks & Timers block of the diagram and double-click. The Clocks & Timers schematic appears.



2. Place the cursor over the schematic until it appears as an edit arrow with brackets. Double-click. The Clocks & Timers dialog appears. The dialog allows you to control circuit paths related to the master clock source and if the PLDCLK pin will be driven by the internal oscillator circuit or not.
3. Select the Timer values using the information below:

Timer1: 1.02ms

Timer2: 2.05ms



4. Click **OK**.
The Timers blocks of the Clocks & Timers schematic are updated with the new values.
5. Place the cursor towards the top of the schematic. When it changes to an up arrow, double-click.
The top-level schematic reappears.

Task 8: Implement Power Management Logic

In this task you describe the power management algorithm of the POWR1220AT8 embedded sequencing controller PLD. The PAC-Designer LogiBuilder feature allows you to create control sequences and define logic functions that will monitor voltage levels and control and supervisory signals of the sequencing circuit. From these inputs the algorithm will produce power-up/down control sequences, hot-swap controls, and power supply trim controls. The tutorial design includes a partially completed set of sequencer instructions that you will import and complete using the LogiBuilder feature. LogiBuilder input and output variables are based on the default or user-defined names you specified in earlier tasks including: Analog Input Settings, Digital Inputs, Logic Outputs, and High Voltage Output Settings.

The complete pseudo code of the sequence algorithm is described in 23 steps (0-22).

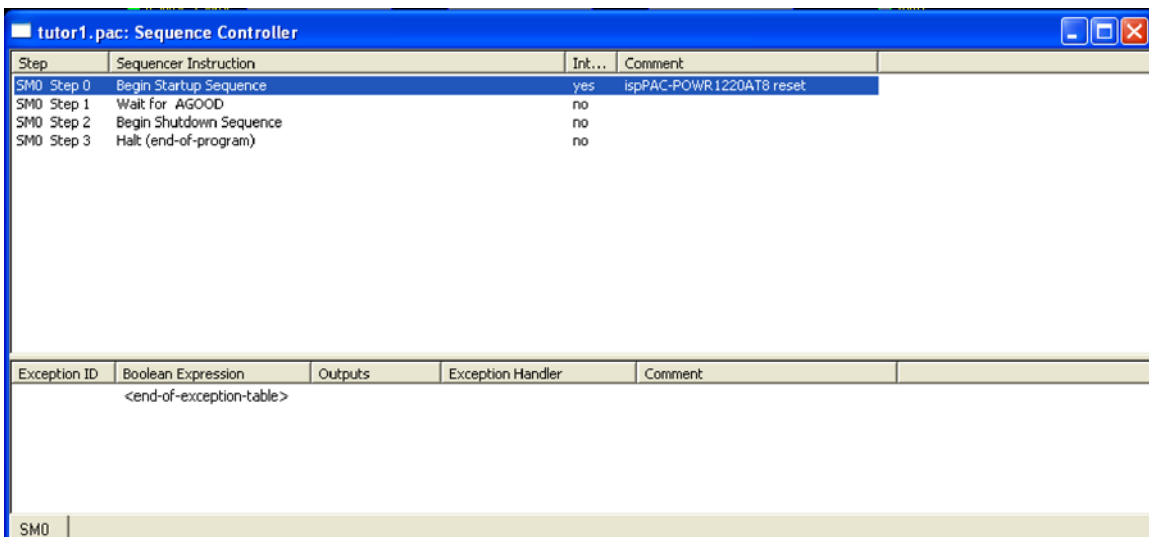
0. ispPAC-POWR1220AT8 reset
1. The analog section is ready to monitor voltages
2. Initialize all logic and MOSFET outputs
3. Wait for 5V and 3.3V to stabilize
4. Soft start 3.3V and 5V supply rails from backplane
5. Soft started 3.3V for I/O is stable
6. Enable sequenced 2.5V supply
7. 2.5V supply is stable

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8. Enable core 1.8V power supply
9. All supplies are stable
10. Reset pulse stretch
11. Release CPU reset, activate power good signal
12. Wait for a supply fault
13. Begin Shutdown
14. Signal a supply fault to CPU, deactivate power good signal
15. Toggle the interrupt back
16. Wait for 2 ms for processor to save status
17. Hold CPU in reset and turn off 1.8V core supply
18. Wait for 1.8V supply to turn off
19. Turn off 2.5V supply
20. Wait for 2.5V supply to turn off
21. Backplane supply is turned off
22. Halt (end-of-program)

To edit the Sequence Controller block:

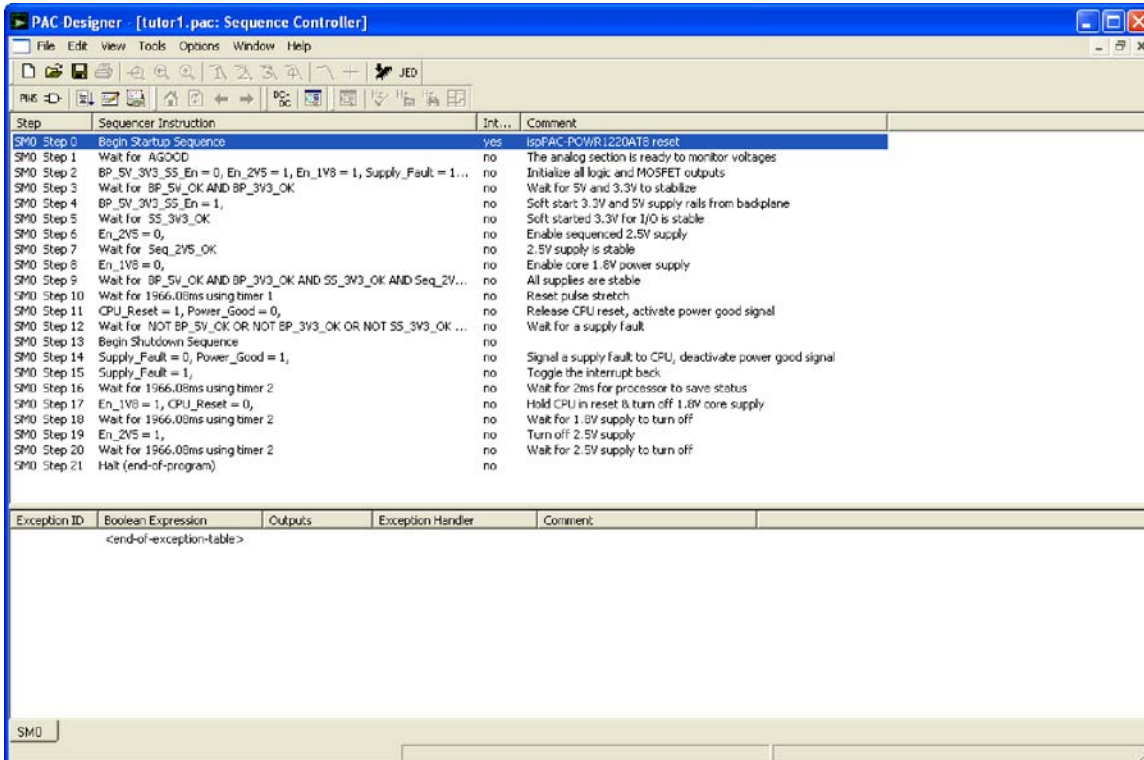
1. Place the cursor over the Sequence Controller block of the diagram and double-click. The tutor1.pac: Sequence Controller window appears.



The LogiBuilder interface provides a sequence control frame and an exception logic frame.

Note the four steps (Step 0 - Step 3) instructions of the sequence control frame. This default template is applicable for most power sequencing designs. In the following steps you'll customize the programmable steps of the sequence.

2. Choose **File > Import LogiBuilder**.
The Import LogiBuilder dialog appears.
3. Browse to <install_path>\Examples\Tutor_Example\tutor1_partial.pac and click **Open**.
4. Click **OK** to dismiss the Import complete dialog box.
A partial implementation of the sequencing logic appears. Note the Comment field matches the pseudo code of the algorithm described at the beginning of the tutorial task.



In the next steps you'll complete the design using dialogs to build the logic expressions.

5. Double-click the last instruction, **Halt (end-of-program)**.
The Insert Step dialog appears.
6. Choose **Outputs** from the list and click **OK**.
An output type sequencer instruction appears in the list as <no outputs specified>.

LogiBuilder provides several pre-defined instruction templates to create sequence controller actions. For more information see the *LogiBuilder Sequence Controller Instruction Set* topic of online help.

Tip: You can also adjust Timer settings from LogiBuilder.

7. Double-click **Step 21**.
The Edit "Output" properties dialog appears.
8. Select **BP_5V_3V3_SS_En** from the Outputs list and click the **Turn off / Deassert** radio button of the Set Value section.
The Output list view is updated with the expression BP_5V_3V3_SS_En=0.

Tip: Even if the output value you require is selected by default, you must click the selection to set the output signal expression. The Output list view will be updated with the equal to (=) sign with each Set To action you take.

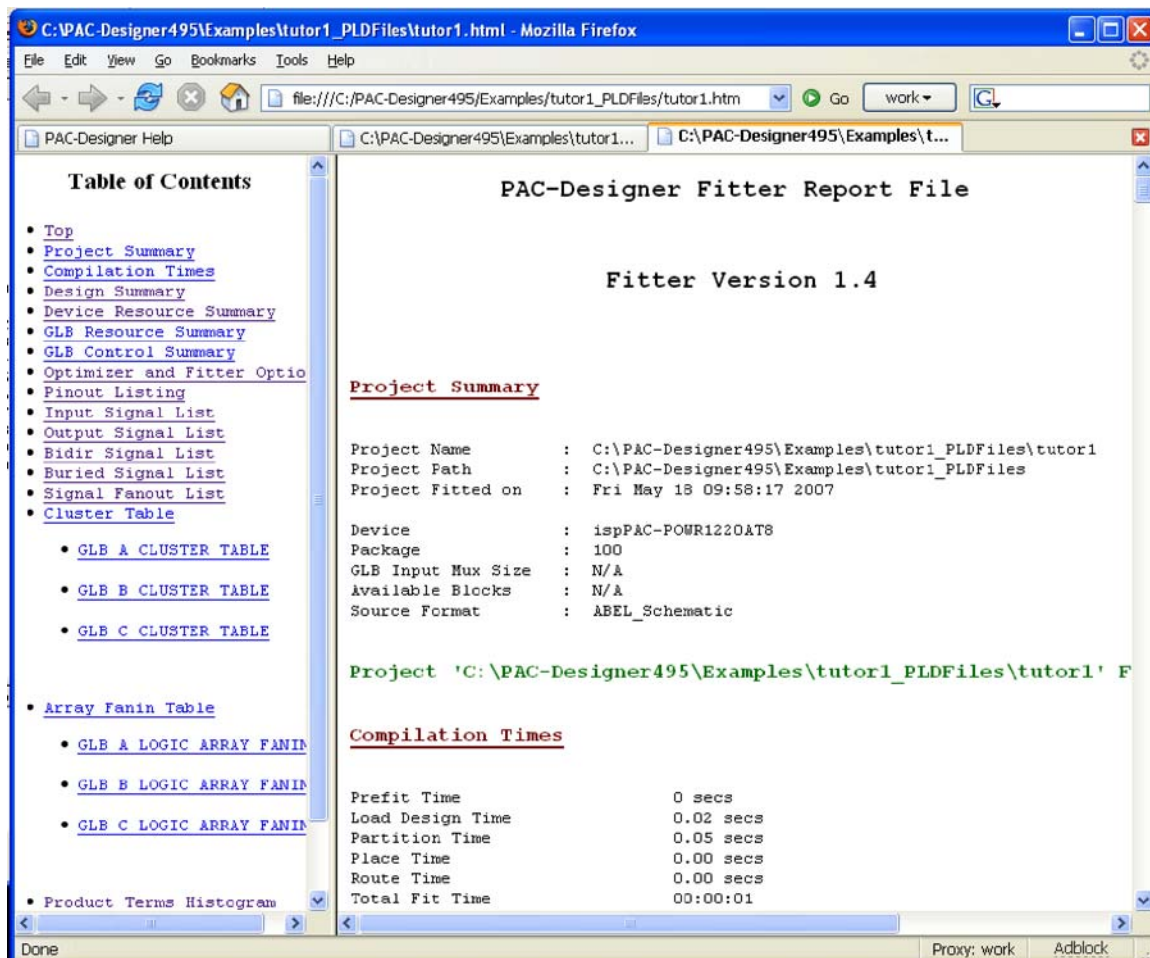
9. Enter **Backplane supply is turned off** into the Comment field and click **OK**.
Step 21 of the Sequencer Instruction list is updated with the new logic expression. Refer to the tutorial schematic design to see how the BP_5V_3v3_SS_En output signal is used in the design.
10. Choose **File > Save**.
tutor1.pac is updated.

Task 9: Compile the Design

In this task you compile sequence controller logic defined in Task 7 into a JEDEC programming file using the Compile to JEDEC feature.

To compile the design:

1. From the LogiBuilder interface, choose **Tools > Compile LogiBuilder Design**.
After a few moments the Compilation Result dialog appears.
2. Click the [Click here to see the fitter report](#) hyperlink.
The PAC-Designer Fitter Report File appears in your system's default web browser.



3. Click the [Device Resource Summary](#) hyperlink of the Table of Contents.
The Device Resource Summary section appears.

The table provides statistics about the resource utilization of the sequence controller PLD of the POWR1220AT8. The tutorial design uses ~30% of the available logic resources. This leaves plenty of room to expand or update the power manager functionality in the future.

- Click the [Input Signal List](#) hyperlink of the Table of Contents.
The Input Signal List section appears.

Note the user-defined names you created in earlier tasks. These names are used as input variables for the sequence controller and appear in the design documentation.

- Click the [PostFit Equations](#) hyperlink of the Table of Contents.
The optimized logic equations implemented into the PLD appear as Boolean expressions in the ABEL syntax. Expressions with “.D” notation indicate data inputs to D-type flip-flops and “.T” notation indicates data input to T-type flip-flops.
- From PAC-Designer, click **OK** to dismiss the Compilation Result dialog box.

Task 10: Simulate the Design

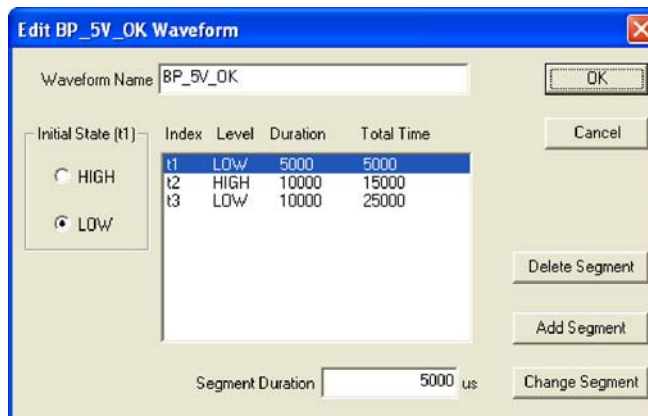
In this task you will verify the logic of the power management algorithm you created in Task 7. After the design has been entered, compiled, and fitted, it can be simulated. Functional simulation is used to verify the correctness of the design but does not simulate gate delays or analog transient analysis. A stimulus file captured in the Power Manager Waveform Editor is used to tell the simulator how and when the input signals change state.

To create waveform stimulus:

- From the LogiBuilder interface, choose **Tools > Run Waveform Editor**.
The Power Manager Waveform Editor appears.

CLK_IN and RESET input stimuli are predefined.
- Click the **Zoom In** toolbar button until the time scale appears as 500 µs/div.
- Double-click the 5V backplane monitor signal, **BP_5V_OK**.
The Edit BP_5V_OK Waveform dialog appears.
- Define the following waveform pattern using the Initial State radio button and Segment Duration entry box.

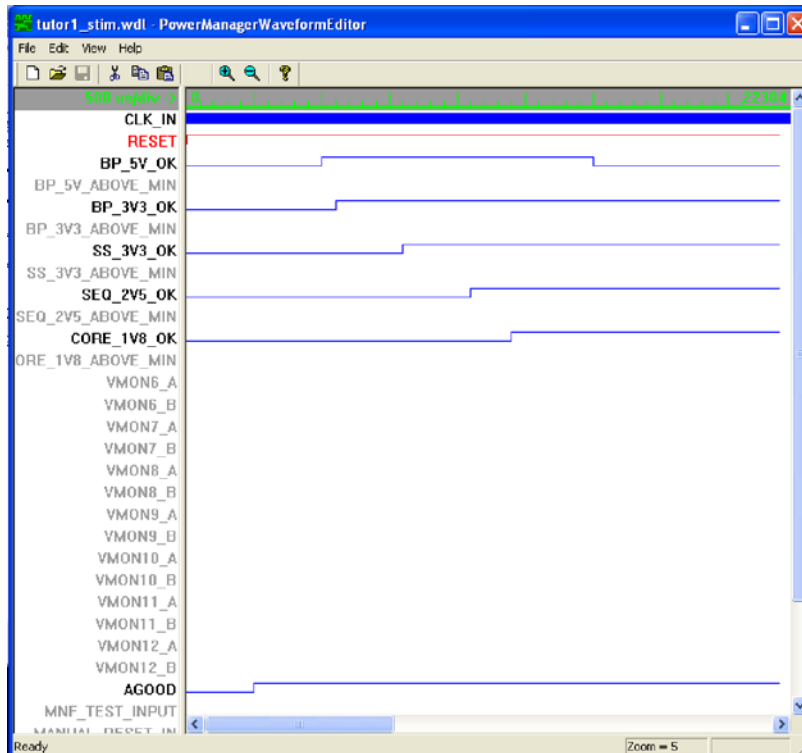
Signal	Pattern
BP_5V_OK	t1, LOW, 5000 t2, HIGH, 10000 t3, LOW, 10000



5. Click **OK**.
The new waveform pattern appears.
6. Define the input stimulus waveform patterns for the remaining input signals using the table below or if you prefer skip to the next procedure and use a pre-defined stimulus file:

Signal	Pattern
BP_3V3_OK	t1, LOW, 5500 t2, HIGH, 97500
SS_3V3_OK	t1, LOW, 8000 t2, HIGH, 97500
SEQ_2V5_OK	t1, LOW, 10500 t2, HIGH, 97500
CORE_1V8_OK	t1, LOW, 12000 t2, HIGH, 97500
AGOOD	t1, LOW, 2500 t2, HIGH, 97500

7. Choose **File > Save**.

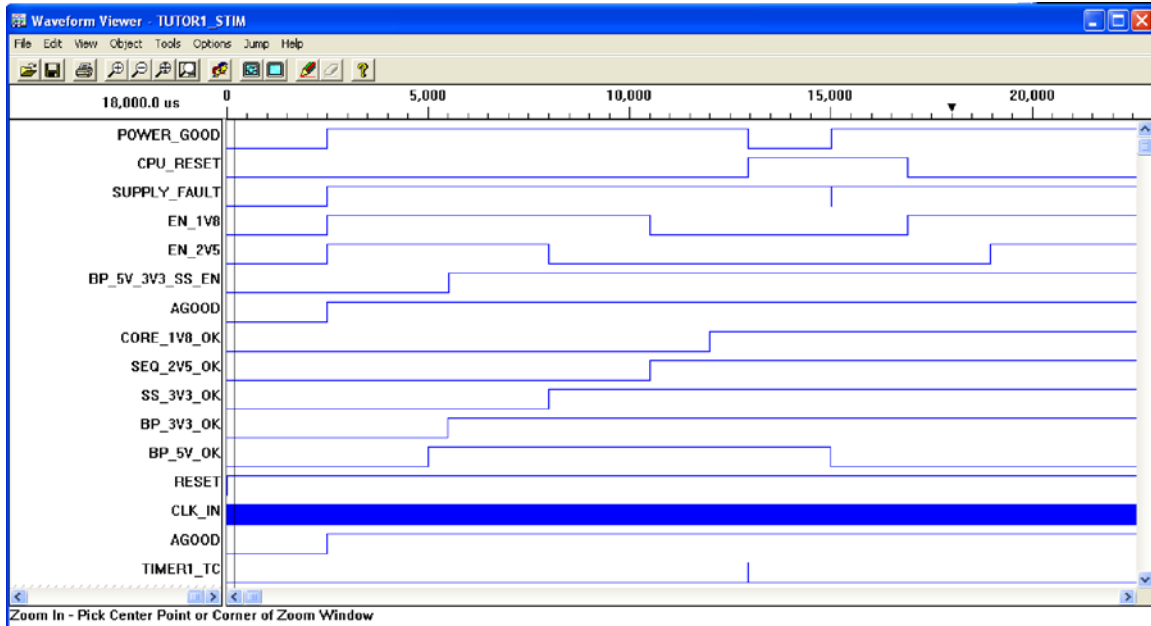


To simulate the design:

1. From the LogiBuilder interface, choose **Tools > Run PLD Simulator**.
The Launch Simulator dialog appears.

- Accept the default Design File and Stimulus File or if you skipped the “create waveform stimulus” procedure above, browse for the **tutor1_stim.wdl** file in the **<install_path>\Examples\Tutor_Example** folder and click **OK**.

After a few moments the Waveform Viewer appears.



Tip: You can use the Show Waves button of the toolbar to add additional signals to the wave display or adjust the arrangement of waveforms by click-and-drag of the mouse.

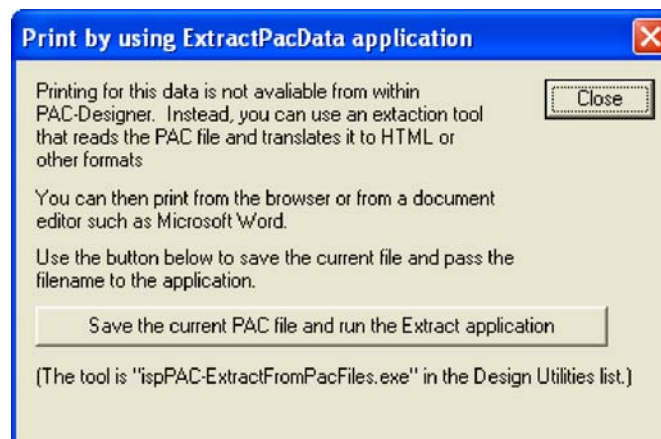
- Choose **File > Exit**.

Task 10: Printing the Design/ Saving the Design to Microsoft Word

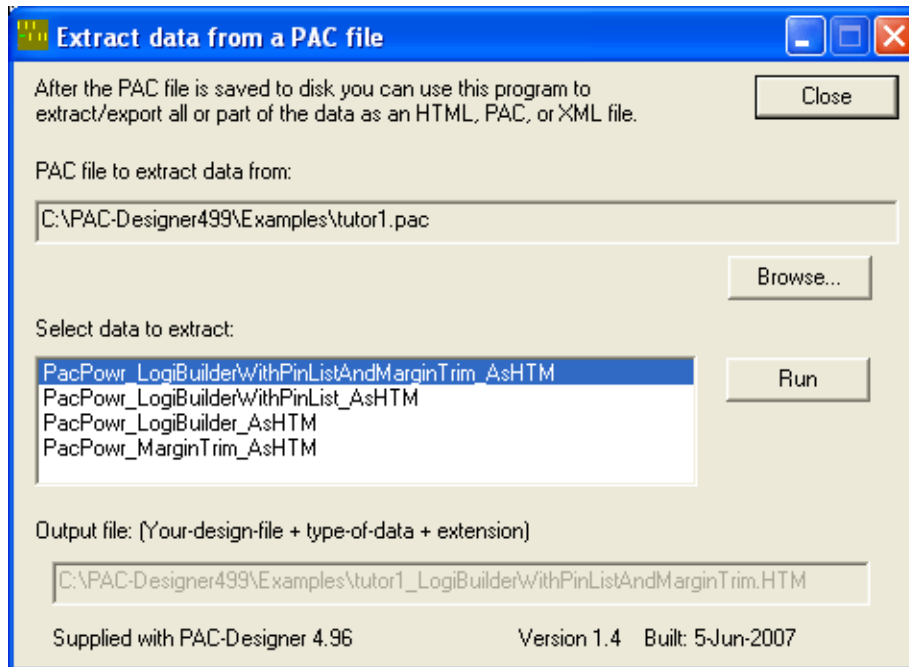
In this task you will print the entire power management algorithm you created in Task 7. After the design is successfully simulated, it can be documented / printed. Because a Power Manager II design has both digital and analog settings, the PAC-Designer software provides a mechanism to combine all these settings along with the power management algorithm into a HTML file. You can then import this HTML file into a Microsoft Word document.

To create the complete design documentation in HTML format:

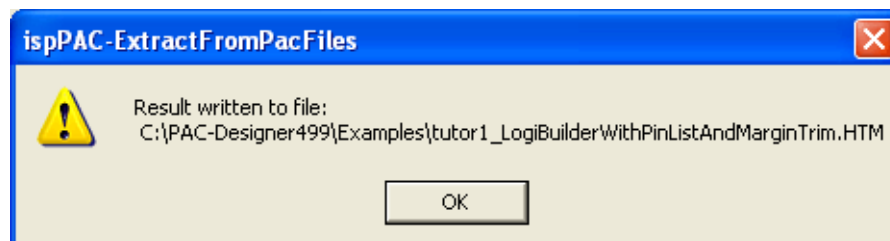
- From the LogiBuilder interface, choose **File > Print**.
The following dialog appears.



- Click the **Save the current PAC file and run the Extract application** button in the center of the dialog box. The following dialog appears.



- Select **PacPowr_LogiBuilderWithPinListAndMarginTrim_AsHTM**.
- Click the **Run** button. The following confirmation dialog box appears showing the location and name of the .htm file.



- Click **OK** to dismiss the dialog box. The software creates a new file with a .htm extension in the same directory as the PAC file.
- Open a new Word document file.
- Read this newly created .htm file into the document.
- Save the document in the required directory and, if necessary, print the document.
- Choose **File > Exit**.

Congratulations

You have completed the *Designing Power Manager II with PAC-Designer* tutorial. In this tutorial you have learned how to:

- Start a new design and navigate the major functional blocks of the POWR1220AT8 block diagram.
- Configure analog and digital input pins to monitor a power sequencing circuit.

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- Configure a high voltage output pin and simulate the turn-on delay of an external MOSFET device.
- Set timer delay values for the embedded timer circuits.
- Implement sequencing logic of the Sequence Controller block using the LogiBuilder feature.
- Compile and simulate the PLD logic using stimulus captured using the Waveform Editor.
- Create a design document.

Additional Study and Resources

The following exercises are recommended for additional study with PAC-Designer and the POWR1220AT8 device:

- Program the PAC-POWR1220AT8-EV evaluation board using the tutorial design.
- Review the I²C block and how it can be used to interface to the device to a supervisory microcontroller.

A summary of the technical notes referenced by this tutorial and additional Lattice resources we highly recommend for Power Manager II design are provided here for your reference.

Data Sheet

- [ispPAC-POWR1220AT8 Data Sheet](#)

PAC-Designer Application Notes

- AN6070 - Using the HVOUT Simulator Utility to estimate FET Ramp Times
- AN6054 - Using PAC-Designer's Power Manager Waveform Editor

Hardware Application Notes

- AN6065 - ispPAC-POWR1220AT8 Evaluation Board
- AN6067 - ispPAC-POWR1220AT8 I²C Hardware Verification Utility
- AN6068 - Programming the ispPAC-POWR1220AT8 in a JTAG chain using the ATDI pin
- AN6069 - Programmable Comparator Options for ispPAC-POWR1220AT8
- AN6073 - Powering Up and Programming the ispPAC-POWR1220AT8
- AN6076 - Optimizing the Accuracy of ispPAC Power Manager Timers
- AN6077 - Stable Operation of DC-DC Converters with Power Manager Closed Loop Trim

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Revision History

Date	Version	Change Summary
June 2007	01.0	Initial release.
August 2008	01.1	Screen shots updated to reflect the new location for Tutorial files.