Lattice Radiant Software 3.0 Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant Software 3.0

- **Device Support:**
  - CertusPro™-NX Device Family (LFCPNX):
    - 100K (-7/-8/-9) HP/LP 1.0V (COM/IND) - ASG256
    - 100K (-7/-8/-9) HP/LP 1.0V (COM/IND) - BBG484
    - 100K (-7/-8/-9) HP/LP 1.0V (COM/IND) - LFG672
    - 100K devices bitstream enabled

- **Tool and Other Enhancements:**

  - **Device Selector** – When creating a new project in the Radiant software, the Device Selector now defaults to LICFL (CrossLink-NX), Performance Grade: 9_High-Performance_1.0 V, Part Number: LICFL-17-9BG256C. Also, the Device Selector now shows both device Part Name and device Family Name in the Family list. For example: LIFCL (CrossLink-NX).

  - **FPGA Libraries** – FPGA Libraries have been added for the CertusPro-NX Device Family (LFCPNX).

  - **License Debug** – Added license debug capability to specify the location of the license file and show the features that are available with the license in the Help > License Debug menu.

  - **Security Settings Tool** – The Security Settings Tool now supports .pem and .der file formats.

  - **Signal Traceability** – This new feature allows you to trace signals from Report View and Output Window and display signals in Netlist Analyzer.

  - **Standalone FlexLM Floating License Package –** For floating license enablement without installing the Radiant Design Software.

  - **Tutorial** – The Lattice Radiant 3.0 Tutorial with CrossLink-NX (LIFCL) adds support for the newest CrossLink-NX Evaluation Board, Revision B. Tasks for programming the chip and for on-board logic analysis have been added.

- **Unified Constraints and Timing Analysis Flow** – Pre-synthesis Timing Constraints Editor now works for both Lattice Synthesis Engine (LSE) and Synplify Pro.

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro for Lattice synthesis tool and the Siemens ModelSim Lattice Edition simulator tool are included in the Radiant software.

- **Synopsys Synplify Pro® FPGA synthesis software version Q-2020.03LR**
  - Release Notes for Synplify Pro are located in ..\<*install_directory*>\radiant\3.0\synpbase\doc\. The file name is release_notes.pdf.
  - A full set of documents for Synplify Pro are also located in ..\<*install_directory*>\radiant\3.0\synpbase\doc\.
- **Siemens ModelSim® Lattice Edition 2020.3 revision 2021.02**
  - Release Notes for ModelSim Lattice Edition are located in ..\<*install_directory*>\radiant\3.0\modeltech\. The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.
  - A full set of documents for ModelSim Lattice Edition are located in ..\<*install_directory*>\radiant\3.0\modeltech\doc\.
- **Siemens Questa® 2020.4**

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-generate some IP, per the procedures described in the following table. These procedures adapt the project for the changes in Radiant software.

Find out which version of Radiant software your project was created with. Then work through the changes for that and every later version, starting with the earliest and going to the most recent. For example, if your project was created with Radiant software 1.0, you would start with the changes for Radiant software 1.0. After completing those changes, you would work on the changes for Radiant software 2.0, and so on.

Once saved, the project will not be compatible with earlier Radiant software versions.

Versions	IP		IP Regeneration Procedures
	CrossLink-NX (LIFCL), Certus-NX (LFD2NX), and CertusPro-NX	**iCE40UP**	
3.0	PLL (Phase Locked Loop)	N/A	These IP used in designs created in Radiant 2.2.1 must be re-generated in Radiant 3.0
	DDR_Generic (DDR Generic Interfaces)		
	GDDR7:1 (LVDS Interface)		
	DDR_MEM (DDR Memory Interfaces)		
	MIPI_DPHY (MIPI D-PHY Interface)		
	LFSR (Linear Feedback Shift Register)		
	ADC_Sequencer (Analog to Digital Converter)		
	RAM_DP_True (True Dual Port RAM)		
	RAM_DQ (Single Port RAM)		
	ROM (Read-only Memory)		
	FIFO		
	FIFO_DC		
	Shift Register		
	Sine-Cosine Table		
	Convert		
2.2.1	PLL (Phase Locked Loop)	N/A	These IP used in designs created in Radiant 2.2 must be re-generated in Radiant 2.2.1
	DDR_Generic (DDR Generic Interfaces)		
	GDDR7:1 (LVDS Interface)		
	DDR_MEM (DDR Memory Interfaces)		
	MIPI_DPHY (MIPI D-PHY Interface)		
	LFSR (Linear Feedback Shift Register)		
	ADC_Sequencer (Analog to Digital Converter)		
	RAM_DP (Pseudo Dual Port RAM)		
2.2	PLL (Phase Locked Loop)	PLL (Phase Locked Loop)	These IP used in designs created in Radiant 2.1 must be re-generated in Radiant 2.2
	DDR_Generic (DDR Generic Interfaces)		
	GDDR7:1 (7:1 LVDS Interface)		
	SDR (Single Data Rate)		
	DDR_MEM (DDR Memory Interfaces)		
	ADC (Analog to Digital Converter)		
	SEDC (Soft Error Detection/Correction)		
	Sin_Cos_Table (Sine Cosine Table)		
	OSC (Oscillator)		
	RAM_DQ (Single Port RAM)		
	RAM_DP_True (True Dual Port RAM)		
	FIFO		
	FIFO_DC (FIFO Dual Clock)		
2.1	PLL (Phase Locked Loop)	N/A	These IP used in designs created in Radiant 1.0, 2.0, or 2.0 SP1 must be re-generated in Radiant 2.1
	GDDR7:1 (7:1 LVDS Interface)		
	DDR_MEM (DDR Memory Interfaces)		
	DDR_Generic (DDR Generic Interfaces)		
	MIPI_DPHY (MIPI Interface)		
	ADC (Analog to Digital Converter)		
	SEDC (Soft Error Detection/Correction)		
	OSC (Oscillator)		
All IP: • Starting with Radiant 2.1, PMIs for any IP created in Radiant software versions 1.0, 2.0, 2.0 SP1, user must add the Family attribute in all PMI instantiations.			

Versions	IP		IP Regeneration Procedures
	CrossLink-NX (LIFCL), Certus-NX (LFD2NX), and CertusPro-NX	**iCE40UP**	
• For designs created in previous versions of Radiant software (2.0 or prior), it is necessary to re-generate PLL IP in Radiant software 2.1. Otherwise, Radiant software 2.1 will issue an error when the previous generated PLL IP is detected in the design. Designs created using Radiant Software 2.0 SP1 with PLL will work without any errors. • The IO_TYPE HDL attribute default value has been changed since Radiant 2.0 SP1 from LVCMOS18 to LVCMOS33. • If a LARGE_RAM IP generated from a previous Radiant version needs to be re-configured in Radiant 2.1, the IP must be re-created.			

The following server IP are not compatible with Radiant 3.0. Use the latest versions of the IP that work with Radiant 3.0:

- I2S Master version 1.0.3
- UART 16550 version 1.0.4
- DDR3 SDRAM Controller version 1.1.1
- DDR3 SDRAM Controller version 1.2.1
- LPDDR2 SDRAM Controller Lite version 1.1.1
- LPDDR2 SDRAM Controller Lite version 1.2.1

Help Resources

Available information resources for the Radiant software include the following:

- Online Help updated with CrossLink-NX (LIFCL), Certus-NX (LFD2NX), and CertusPro-NX (LFCPNX) content.
  - To view the Online Help, start the Lattice Radiant software and select the  "Getting Started" icon under Information Center.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel Pentium or Pentium-compatible PC
- 64-bit OS:
  - Windows 10
  - Red Hat Enterprise Linux 7.8 or 8.2
  - Ubuntu version 18.04 LTS or 20.04 LTS
- Approximately 10 GB free disk space
- Computer Memory Requirement: 16 GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.

- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Acrobat Reader

Known Issues for Radiant 3.0

The following are known issues for the Radiant Software 3.0.

MAP incorrectly reports number of DPHY and PCIE/ADC resources for CrossLink-NX (LIFCL) QFN72 package.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-8297

When simulating Generic DDR, there may be a mismatch in the RTL and post-route simulation. Silicon is not affected.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX), CertusPro-NX (LFCPNX)

Bug number: DNG-9639

CSI-2/D-PHY Transmitter IP hangs during Post synthesis/PAR simulations.

For some configurations of CSI-2/DSI D-PHY-TX IP, post-synthesis and post-PAR simulation hangs (runs indefinitely without stopping) when LSE is used.

Workaround: Use Synplify Pro for synthesis and generating the post-PAR netlist if you run into this issue.

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX)

Bug number: DNG-9697

For some SystemVerilog designs, Synplify Pro fails to identify multi-driven nets and the flow passes with no errors.

Workaround: Check the design for multi-driven nets and run the flow using LSE to verify.

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX), CertusPro-NX (LFCPNX)

Bug number: DNG-10132

Modify default INIT value for HardDPHY RX soft IP when running at DPHY v1.1 data rate (<=1.5 Gbps).

When Hard DPHY is used, the input Tsu/Thd is unbalanced resulting in marginal Tsu performance at line rate <= 1.5 Gbps in this release. The following devices and IP are affected:

Device: Crosslink-NX (LIFCL)

IP: MIPI_DPHY (Hard DPHY, Receive Mode)

Workaround: To satisfy datasheet specification compliance, it is necessary to re-center the Tsu/Thd using the Manual De-Skew Calibration Delay Control feature in the Hard DPHY by performing the following on the generated RTL:

If MIPI_DPHY IP is used as the Receive interface with the Hard DPHY option at Data Rate <= 1.5 Gbps, modify the DPHY module instantiation's hard coded TEST_PATTERN[31:0] parameter setting from "0b00000000000000000000000000000000" (0x00000000) to "0b10000000001000000000000000000000" (0x80200000) in the <instance_name)_ipgen_lscc_mipi_wrapper_rx module inside <instance_name>.v which is located in the RTL files folder of the generated IP.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-10731

Simulation of LRAM-based IP core on Linux based OS, has a long startup time.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX), CertusPro-NX (LFCPNX)

Bug number: DNG-10862

Radiant post-synthesis simulation may fail with LSE when the inputs to an arithmetic function are synchronously preset to a value other than 0.

Workaround: Set the following LSE Strategy setting to:

DSP Style = Logic

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX), CertusPro-NX (LFCPNX)

Bug number: DNG-11193