PCIe x8 IP

IP Version: v2.2.0

Release Notes

FPGA-RN-02061-1.1

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Contents

1. Introduction

This document contains the Release Notes for the PCIe x8 IP and PCIe x8 Driver. For specific details about the IP and the driver, refer to the following:

- PCIe x8 IP Core User Guide (FPGA-IPUG-02243)
- Avant-G/X PCIe Host DMA Driver Software User Guide (FPGA-TN-02405)
- CertusPro-NX and Avant-G/X PCIe Basic Memory-Mapped Host Driver (Non-DMA) User Guide (FPGA-TN-02387)
- PCI Express for Avant FPGAs web page

PCIE x8 IP v2.2.0

Software	Software Version	Summary of Changes

Lattice Radiant	2024.2.1	• Feature Updates
		  • Active State Power Management (ASPM) capability enablement
		• Example Design Updates
		  • Added Harden DMA Gen4x8 Example Design hardware support.
		  • Added non-DMA Gen4x8 Example Design hardware support.
		• Driver Updates
		  • Added official driver support for Harden DMA and non-DMA

PCIE x8 IP v2.1.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	• Enabled Harden DMA Gen4x8 support for Synthesis/Timing/Simulation. • Enabled Harden DMA Gen4x8 Example Design simulation. • Updated the PCIe PCS/PHY parameters for hardware support (official hardware support in Radiant 2025.1). • Fixed bugs related to PCIe BAR, PF, VF, MSI and MSI-X.

PCIE X8 IP Earlier Versions

IP Version	Summary of Changes

2.0.0	• PHY Configuration
	  • Increased aggregation and bifurcation up to x8 lanes
	  • Increased data rates of 8.0 Gbps and 16.0 Gbps
	  • Added 128b/130b encoding at 8 Gbps and 16 Gbps
	  • Added support for PCIe L1-substate power management and Separate RefClk Independent SSC Architecture (SRIS)
	• Hard IP Link Layer Features
	  • PCI Express Base Specification Revision 4.0 compliant including compliance with earlier PCI Express Specifications
	  • Backward compatible with PCI Express 3.x, 2.x, 1.x
	  • x8 PCI Express Lanes with support for bifurcation
	  • Supported lane configurations: 1 × 8, 1 × 4, 1 × 2, 1 × 1

1.1.0	• PHY Configuration
	  • Aggregation and bifurcation up to x4 lanes
	  • Data rates of 2.5 Gbps and 5.0 Gbps
	  • Selectable parallel data widths such as 8, 16, 32, and 64
	  • 8b/10b encoding at 2.5 Gbps and 5 Gbps
	  • Adaptive and configurable RX Continuous Time Linear Equalizer (CTLE) and Decision Feedback Equalizer (DFE)
	  • Adaptive and programmable TX equalization

IP Version	Summary of Changes
	• Extensive PMA debug capability through read/write and read-only registers in PCS • Register-based control of all PCS-to-PMA signals • A wide range of reference clock frequencies with optional fractional frequency correction capability • A wide range of divided clock frequencies for external-to-PHY usage with optional spread-spectrum clock (SSC) capability • Built-in, on-chip SSC generation and full configuration from –5000 to +5000 ppm • Test support features such as near-end loopback, PLL bypass modes, and others • Protocol-compatible features such as LOS, squelch, power modes, and others • Hard IP Link Layer Features • PCI Express Base Specification Revision 2.0 compliant including compliance with earlier PCI Express Specifications • Backward compatible with PCI Express 1.x • x4 PCI Express Lanes with support for bifurcation • Supported lane configurations: 1 × 4, 1 × 2, 1 × 1
1.0.1	• Supports Synthesis/Timing/Simulation • Supports Gen1/2 x1/x2/x4 Endpoint • Supports AXI-L/LMMI for config bus • Supports AXI-S/TLP interface for data bus • Supports Example Design simulation using QuestaSim (refer to IPUG for details) • Supports up to 8 PF with workaround (refer to IPUG or ED. To be addressed in 2023.2 SP1)

References

- PCIe x8 IP Core User Guide (FPGA-IPUG-02243)
- Avant-G/X PCIe Host DMA Driver Software User Guide (FPGA-TN-02405)
- CertusPro-NX and Avant-G/X PCIe Basic Memory-Mapped Host Driver (Non-DMA) User Guide (FPGA-TN-02387)
- Avant-E web page
- Avant-G web page
- Avant-X web page
- PCI Express for Avant FPGAs web page
- Lattice Propel Builder software
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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