SGDMA Controller IP

IP Version: v2.4.0

Release Notes

FPGA-RN-02058-1.0

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Contents

1. Introduction

This document contains the Release Notes for the SGDMA Controller IP and SGDMA Controller Driver. For specific details about the IP and driver, refer to the following:

- SGDMA Controller IP Core (FPGA-IPUG-02131)
- SGDMA Driver API Reference (FPGA-TN-02340)
- Scatter-Gather DMA Controller IP Core web page

SGDMA Controller IP v2.4.0

Software	Software Version	Summary of Changes

Lattice Radiant™	2024.2	• Bug Fixes
		  • Corrected a functional bug, where the AWADDR of the AXI-MM interface in the SGDMAC IP does not increment if the Write Response (BRESP) handshake took longer than one clock cycle to complete.
		  • Improved metadata to resolve compatibility issues with Lattice Propel™ software when using the APB interface for Control and Status Register access.
		  • Addressed the issue where the clock for the AMBA APB Control and Status Register interface was not constrained.
		• Driver Changes
		  • Added driver support for multiple instances of the SGDMA IP.
		  • Separated the configuration of the SGDMA descriptors and the initiation of the SGDMA transfers into two distinct functions.

SGDMA Controller IP v2.3.0

Software	Software Version	Summary of Changes

Lattice Radiant	2024.2	• Feature Changes
		  • Enabled independent clock support for AXI-MM and AXI-S interfaces to ease system design flexibility and timing closure.
		  • Enabled additional AMBA APB interface as an option for accessing the IP Control and Status Registers.
		  • Fixed interface backpressure-related bugs in both AXI-MM and AXI-S interfaces present within the IP.
		  • Fixed bug within the IP Descriptor module that does not execute pending MM2S or S2MM transfer that is issued while the DMA engine is active.
		  • Fixed issue where reading the status register for *_XFER_CMPL or *_ERR flags always clears the concurrent completion or error flag event that happens during the same clock cycle.
		• Example Design Changes
		  • Modified the Example Design simulation top-level (tb_top.sv) and hardware testing top-level (eval_top.sv) to be near identical with the inclusion of a clock oscillator, PLL, and a button debouncer module in both. Simulation now closely reflects hardware behaviour.
		  • Updated Example Design simulation to support AMBA APB interface for Control and Status Register access.
		  • Updated Example Design hardware to support independent clock for AXI-MM and AXI-S interfaces.
		  • Tested the Example Design hardware on Certus-NX VERSA board, CertusPro-NX Evaluation Board, Certus Pro-NX PCIe Bridge Board, and Avant-X VERSA board.
		• Driver Changes
		  • Fixed the logic in polling SGDMA descriptor status.

SGDMA Controller IP Earlier Versions

IP Version	Summary of Changes
2.2.0	Driver Changes: mm2s_get_desc_complete_bit and s2mm_get_desc_complete_bit, enabling users to continuously poll for the descriptor's status. Within sgdma_instance_t, new variables have been added to allow independent configuration of MM2S and S2MM.
2.1.1	Fixed protocol error on the AXI4-Lite interface that is used to access IP's Control and Status Registers.
2.1.0	Fixed an issue with CDC-related SDC constraints being dropped. Added support for Lattice Certus-NX and Avant devices and for Questasim OEM Example Design Simulation.
2.0.1	Fixed an issue on AXI-S tlast and tvalid behavior. Macros renamed and added external read/write APIs.
2.0.0	Re-architected SGDMA, enabling AXI protocol. Not backward compatible with previous versions.
1.2.0	Added LFMXO5 support.
1.1.0	Added LFCPNX support.
1.0.0	Initial release.

References

- SGDMA Controller IP Core (FPGA-IPUG-02131)
- SGDMA Driver API Reference (FPGA-TN-02340)
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Certus-N2 web page
- Certus-NX web page
- CertusPro-NX web page
- Scatter-Gather DMA Controller IP Core web page
- Lattice Propel Builder software
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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