CSI-2/DSI D-PHY Tx IP

IP Version: v2.2.0

Release Notes

FPGA-RN-02041-1.0

December 2024

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Contents

1. Introduction

This document contains the Release Notes for the CSI-2/DSI D-PHY Tx IP. For specific details about the IP, refer to the following:

- CSI-2/DSI D-PHY Tx IP User Guide (FPGA-IPUG-02080)

Note: These release notes document the changes from IP version 2.2.0 and Lattice Radiant software version 2024.2 and above.

CSI-2/DSI D-PHY Tx IP v2.2.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	• Added internal reset synchronizer to byte_clk_o clock domain. • Removed the requirement to have output byte clock (byte_clk_o) active when accessing CSR. • Updated maximum data rate to be consistent with the Lattice device datasheet. • Added an example design. • Added support for Certus-N2 devices. • Added support for LFD2NX-9 and LFD2NX-28 devices. • Other minor IP enhancements.

CSI-2/DSI D-PHY Tx IP v2.1.0 and Below

Software	Software Version	Summary of Changes
Lattice Radiant	2024.1 and below	Refer to the Release Notes section in *introduction.html* in the Radiant software installation folder or the IP server for details on changes made in previous versions of this IP.

References

- CSI-2/DSI D-PHY Tx IP User Guide (FPGA-IPUG-02080)
- Certus-NX web page
- Certus-N2 web page
- CertusPro-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- CSI-2/DSI D-PHY Transmitter IP Core web page
- Lattice Propel Builder software
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase

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