DDR3 SDRAM Controller IP

IP Version: v2.1.0

Release Notes

FPGA-RN-02032-1.1

March 2025

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

1. Introduction

This document contains the Release Notes for the DDR3 SDRAM Controller IP and the DDR3 Memory Controller Driver. For specific details about the IP and driver, refer to the following:

- DDR3 SDRAM Controller IP Core for Nexus Devices (FPGA-IPUG-02086)
- Certus-NX DDR3 Memory Controller Driver User Guide (FPGA-TN-02401)

DDR3 SDRAM IP v2.1.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	Added driver support

DDR3 SDRAM IP v2.0.1

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	• Added support for AXI4 Interface as data bus and APB Interface as control bus. • Added example design. Updated testbench to make use of the example design in simulation. • Disabled obfuscation to enable the constraints in Radiant flow. • Added GUI options: MC CK/Command Delay value and MC DQS/DQ ODT Value. • Fix em_ddr_clk_t and em_ddr_clk_c alignment for Gearing ratio 4:1

DDR3 SDRAM Controller IP Earlier Versions

IP Version	Summary of Changes
1.4.2	• Fixed timing parameters for gearing ratio 8:1. • Removed tRFC wait time when issuing a precharge during auto-refresh. • Removed set_max_delay of synchronizers for the de-assertion of reset in top_constraint.pdc.
1.4.1	• Fixed the missing activate issue when cmd_rdy_o are cmd_valid_i are changed from invalid to valid at the same time. • Added cmd_burst_cnt_i sweep in the testbench/testcase.vh. • Removed global clock constraint in the top_constraint.pdc and improve the constraints. • Synchronized the reset de-assertion inside the IP. • Added Enable External PLL Reset attribute. • Added external ports for write leveling start and done. • Added support for both internal and external refresh when Enable External PLL Reset and External Auto Refresh Port are selected. • Fixed precharge all command during internal auto refresh.
1.4.0	• Updated read training logic based on validation in the board. • Added option to disable the internal PLL • Updated the selectable values for Select Memory and RefClock attributes. • Changed the default value of Controller Reset to Memory attributes. • Updated the testbench to add write delay that would match with the PHY delay settings that worked on the board. Fixed the cmd_burst_cnt_i=2 issue when 8:1 gearing ratio.
1.3.0	Updated for Radiant 3.0.
1.2.1	Updated PLL instance.
1.2.0	Added LFCPNX support.
1.1.1	Improved performance for 8:1 gearing ratio.

IP Version	Summary of Changes
1.1.0	• Updated for Radiant 2.1. • Added 8:1 gearing ratio support. • Added eval folder. Added Certus-NX support. • Updated clock signal names: clk_i, sclk_o. • Updated PLL instance.
1.0.1	Updated for Radiant 2.0 Service Pack 1.
1.0.0	Preliminary release.

References

- DDR3 SDRAM-Controller IP Core for Nexus Devices (FPGA-IPUG-02086)
- Certus-NX DDR3 Memory Controller Driver User Guide (FPGA-TN-02401)
- Lattice Nexus Platform web page
- IP Core for Lattice Nexus devices
- Lattice Propel Builder software
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase

www.latticesemi.com