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Inclusive Language
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About Lattice Propel™ 2024.1

Welcome to the Lattice Propel 2024.1 design environment for Lattice FPGA system design. Lattice Propel is a complete set of graphical and command-line tools to create, analyze, compile, and debug both FPGA-based hardware and software processor systems.

What’s New in Lattice Propel 2024.1

New Operating System (OS) Support
- Ubuntu 22.04 LTS

New Device Support
- Lattice ECP5U™
- Lattice ECP5UM™
- Lattice ECP5UM5G™

Tools and Enhancements
- Supports user custom application templates
- Supports TCL in IP Packager
- Supports ECPS and ECP5-5G devices
- Supports Lattice Avant RISC-V MC/RX SoC templates
- Supports "Attach to running target" in debugger
- Supports GUI color customization options for schematic
- Supports code coverage and timing profiling on RISC-V RX SoC Project
- Supports an extension on C projects created for RISC-V RX SoC Project
- Supports a new entry to distinguish SoC creation from custom templates or built-in templates
- Supports QuestaSim instead of ModelSim
- Supports DRC of generating default value in top RTL file for AMBA4 dangling optional ports
- Supports DRC of cacheable address range on SoC including RISC-V RX processor
- Supports DRC of connection compatibility between RISC-V RX processor and TCM
- Supports VHDL for RTL module of glue logic
- Supports friendlier interface names in IP Packager GUI Display
- Supports QEMU Virtual Platform
- Supports creating application template Hello World Project for RISC-V MC/SM/RX minimum system
- Supports creating application template RX Demo Project for RISC-V RX minimum system
- Supports creating default debug launch configuration when creating a C project
- Supports enabling/disabling automatically build the project when creating a C project
- Hides glue logics from verification project view
- Supports read-only address map for verification projects
- Adds a new entry of importing Lattice C/C++ Projects into Workspace
- Adds application template FreeRTOS-LTS-Minimal Project
- Former FreeRTOS Project is renamed to FreeRTOS-LTS PMP-Blinky Project
- FreeRTOS Kernel update from v10.0.1 to v10.5.1 based on FreeRTOS 202210.01 LTS
Key Features

Device Family Support
- Lattice LAV-AT (Avant™)
- Lattice LFMXO5 (MachXO5™-NX)
- Lattice LIFCL (CrossLink™-NX)
- Lattice LFCPNX (CertusPro™-NX)
- Lattice LFMNX (Mach™-NX)
- Lattice LFD2NX (Certus™-NX)
- Lattice MachXO3D™
- Lattice MachXO2™
- Lattice MachXO3L™
- Lattice MachXO3LF™
- Lattice ECP5U
- Lattice ECP5UM
- Lattice ECP5UM5G

Processor Support
- RISC-V Micro Controller (MC)
- RISC-V State Machine (SM)
- RISC-V Real Time OS (RX)
- Dual processors

Operating System Support
- Microsoft Windows 11 Pro (64-bit)
- Microsoft Windows 10 Enterprise (64-bit)
- Red Hat Enterprise Linux 7.9 (64-bit)
- Red Hat Enterprise Linux 8.8 (64-bit)
- Ubuntu 20.04 LTS (64-bit)
- Ubuntu 22.04 LTS (64-bit)

Lattice Propel SDK
- Integrated picolibc as the default standard C library to support three levels of printf.
- Built-in industry standard components and tools for embedded software development and debugging.
- Optimized project management flow for Lattice FPGA platform.
- Supports creating both C and C++ software projects based on Lattice SoC platform.
- Supports Lattice Diamond®, Lattice Radiant™, and Propel Builder bridges.
- Integrated GNU Debugger (GDB) and Open On-Chip-Debugging (OCD) with chained JTAG.
- Supports peripherals view with register description during debug session.
- Supports syntax highlighting for various development languages.
- Supports semihosting for On-Chip-Debugging and QEMU Virtual Platform.
- Supports multiple channels for On-Chip-Debugging.
- Supports “Attach to running target” for On-Chip-Debugging.
- Supports user custom application templates.
- Supports QEMU Virtual Platform.
- Supports creating application template QEMU_hello world Project for QEMU Virtual Platform.
- Supports creating application template Hello World Project for RISC-V MC/SM/RX minimum system.
- Supports creating application template RX Demo Project for RISC-V RX minimum system.
- Supports creating application template FreeRTOS-LTS-Minimal Project and FreeRTOS-LTS PMP-Blinky Project for RISC-V RX SoC project.
- Supports creating application template Timing Profiling Project for RISC-V RX SoC Project.
- Supports code coverage on FreeRTOS-LTS PMP-Blinky Project and RX Demo Project.
Lattice Propel Builder

- Supports adding some Lattice Radiant foundation IP.
- Supports modifying a device.
- Supports displaying board information.
- Supports managing IP.
- Supports schematic design.
- Supports creating SoC project and SoC verification in project wizard Graphic User Interface (GUI).
- Supports Lattice Diamond, Lattice Radiant, QuestaSim, and Propel SDK bridges.
- Supports generating simulation environment, testbench, and script.
- Integrated ModelSim Original Equipment Manufacturer (OEM).
- Supports glue logic.
- Supports IP Packager flow control.
- Supports hierarchical IP.
- Supports displaying the latest IP version in the Propel Builder catalog by default.
- Supports AXI4 and AXI4-Lite interfaces.
- Supports creating more flexible AXI-based SoC.
- Supports new GUI options, new interface, and VHDL.
- Supports input ports, output ports, and glue logic to be connected to inout ports.
- Supports using TCL command line to clear Tcl Console, create SoC, reconfigure glue logic, connect grouping signals.
- Supports Auto Connect grouping signals.
- Supports reference IP RTL from user-specified library in IP Packager.
- Supports generation and reconfiguration of IP from centralized IP repository.
- Supports subordinate sbx for design simplification and memory map display.
- Improves customized templates with constraint file included.
- Optimizes warnings and disables modifying Propel IP in Radiant software.
- Supports generation of a file list for scripted build flows.
- Supports IP upgrade through TCL commands.
- Supports switching design output language between Verilog-HDL and VHDL after initial project creation.
- Supports exporting SoC as a set of TCL command and recreating from it.
- Supports DRC for mismatched ID/DATA width in AXI4, AHB-Lite, and APB interfaces.
- Supports TCL in IP Packager.
- Supports GUI color customization options for schematic.
- Supports a new entry to distinguish SoC creation from custom templates or built-in templates.
- Hides glue logics from verification project view.
- Supports DRC of generating default value in top RTL file for AMBA4 dangling optional ports.
- Supports DRC of cacheable address range on SoC including RISC-V RX processor.
- Supports DRC of connection compatibility between RISC-V RX processor and TCM.
- Supports read-only address map for verification projects.
- Supports VHDL for RTL module of glue logic.
- Supports friendlier interface names in IP Packager GUI Display.

IP Support

For IP support, refer to related IP user guides for detailed information.
Template Design and System Simulation

- Provides CertusPro-NX template design, the RISC-V MC SoC Project. Enhanced to support multiple clock domain.
- Provides CrossLink-NX template design, the RISC-V MC SoC Project.
- Provides MachXO2 template design, the RISC-V MC SoC Project.
- Provides MachXO3D template design, the RISC-V MC SoC Project and Lattice Sentry RoT Project (Windows OS only).
- Provides Mach-NX template design (Windows OS only), the Lattice Sentry RoT Project (484), and Lattice Sentry RoT Project (256).
- Provides CertusPro-NX AXI based template design, the RISC-V RX SoC Project.
- Supports functional verification using system-level simulation environment for templates.
- Supports backward-compatible templates, such as Sentry 1.0, Sentry 2.2, Sentry 3.0 projects.
- Provides CertusPro-NX template design, the RISC-V MC Dual Processor Project.
- Provides ECP5 template design, the RISC-V MC SoC Project.
- Provides Lattice Avant template design, the RISC-V MC SoC Project and RISC-V RX SoC Project.
- Supports simulation for design with VHDL.
- Supports simulation for RISC-V RX core templates.
- Supports QuestaSim instead of ModelSim.
- Supports DUT with one-level sub SBX in verification project.

Release Contents

- Propel_2024.1.exe (Windows 10/11 64-bit Operating System)
- Propel_2024.1_lin.run (Red Hat Enterprise Linux 64-bit & Ubuntu LTS Operating System)

Validation Platforms

- CertusPro-NX Evaluation Board (REV A P/N: LFCPNX-EVN)
- Certus-NX Versa Evaluation Board (REV B P/N: LFD2NX-VERSA-EVN)
- CrossLink-NX Evaluation Board (REV B P/N: LIFCL-40-EVN)
- AVANT-AT-E Evaluation Board (REV D P/N: LAV-E70-EVN)
- ECP5 Versa Development Kit (Rev B LFESUM-45F-VERSA-EVN)
- MachXO2 Breakout Board (REV B P/N: LCMXO2-7000HE-B-EVN)

System Requirements

The basic system requirements for Lattice Propel 2024.1 on Microsoft Windows and Linux Operating System (OS):

- Complex instruction set system based on x86 64-bit architecture
- Windows 10/11 64-bit OS
- Red Hat Enterprise Linux 64-bit OS (RHEL7.9/8.8)
- Ubuntu 20.04/22.04 LTS OS
- Free Disk Space: approximately 8 GB
- Network adapter and network connectivity for IP server access
Release Limitations

This release of Lattice Propel 2024.1 has the following limitations:

- You need to regenerate all encrypted IP in Propel 2024.1 if you use Lattice Radiant 2023.2 or previous versions.
- DUT with one-level sub SBX is with limited support in verification project.
- RISC-V RX SoC Project is not yet validated on Lattice Avant G70/X70 board.
- The prerequisite for reproducing projects from TCL commands is that the IP involved already exists at local.
- Encrypted VHDL is only supported in Lattice Radiant flow, but not in Lattice Diamond flow.
- Lattice Diamond flow is not supported in Ubuntu LTS Operating System.
- The MAX_PATH inside Windows file I/O API is restricted to 260 characters, but the usable path is even more constrained. The MAX_PATH must contain the drive letter and the NULL character to terminate the string correctly.
- OpenOCD vexRISC-V cannot read Float Point Unit (FPU) registers, which makes Propel SDK unable to show FPU related register values.
- Lattice Propel 2024.1 software does not support HW-USBN-2A cable.

Known Issues

This release of Lattice Propel 2024.1 has the following known issues:

- There is no QuestaSim waveform output for RISC-V RX template.
- Invalid read error appears at QEMU launching time.

Note

It is recommended to use the same version of Lattice Radiant and Lattice Propel for best compatibility.

Technical Support

- For assistance, submit a technical support case at www.latticesemi.com/techsupport.
- For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/en/Support/AnswerDatabase.
- Previous Lattice Propel software versions are available on Software Archive page on Company Public website: https://www.latticesemi.com/Support/SoftwareArchive
## Revision History

**Revision 1.0, June 2024**

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