



# 8N1 UART Transceiver Demo

## User Guide

FPGA-UG-02118-1.0

October 2020

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## Acronyms in This Document

A list of acronyms used in this document.

| Acronym | Definition                                  |
|---------|---|
| FIFO    | First In, First Out                         |
| FTDI    | Future Technology Devices International     |
| PC      | Personal Computer                           |
| Rx      | Receiver                                    |
| Tx      | Transmitter                                 |
| UART    | Universal Asynchronous Receiver/Transmitter |
| USB     | Universal Serial Bus                        |

## 1. Introduction

This UART (Universal Asynchronous Receiver/Transmitter) demo shows the operation of UART to PC interface using the 8N1 UART Transceiver Reference Design and the Himax HM01B0 UPduino Shield board. The FTDI chip in the Himax HM01B0 UPduino Shield board is utilized for USB-to-UART interface. As such, the board only requires the same micro-USB cable for programming UART interface with the PC. The configuration used is enabled FIFO buffer with 512 address depth, 9600 baudrate, 8-bit data, no parity, and 1 stop bit.

The operation is a simple loopback of serial data where PC/Host Controller transmits serial data. The iCE40 UltraPlus™ device then receives the serial data and transmits back to the PC/Host Controller. This demo is designed to test if the same correct data is received and transmitted by the the iCE40 UltraPlus device.

## 2. Functional Description

The Himax HM01B0 UPduino Shield board's FTDI functions as USB-to-UART interface. Thus, the serial Tx and Rx between the PC/Host controller and the iCE40 UltraPlus device pass through it.

Figure 2.1 shows the diagram of the UART demo. The PC/Host Controller sends 8-bit serial data to the iCE40 UltraPlus device. The iCE40 UltraPlus UART Rx captures the 8-bit serial data, which is then placed on the FIFO buffer, which is turned on for this demo. UART Tx takes the data from the FIFO buffer to be transmitted back to the PC/Host Controller.

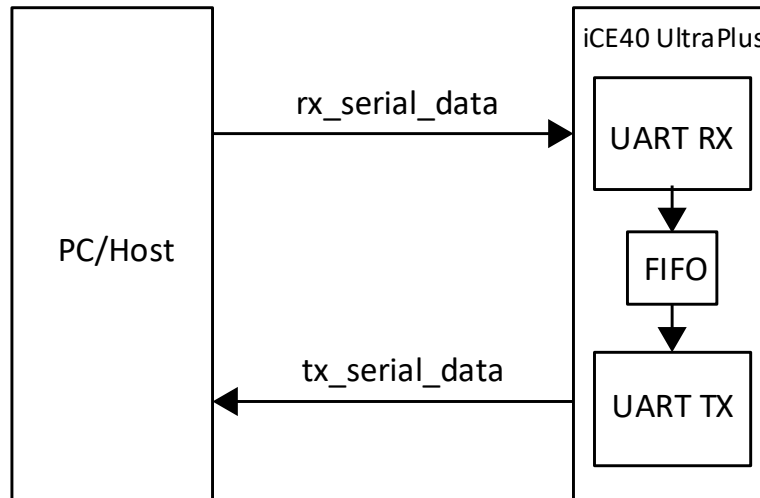


Figure 2.1. Functional Block Diagram

### 3. Demo Setup

To set up the demo:

1. Connect the Himax UPduino board to the PC using the micro USB cable.
2. Launch Diamond® Programmer.
3. Create a new blank project for iCE40 UltraPlus device. In the **Getting Started** dialog box, select **Create a new blank project** and click **OK**. This opens the main interface of Diamond Programmer.

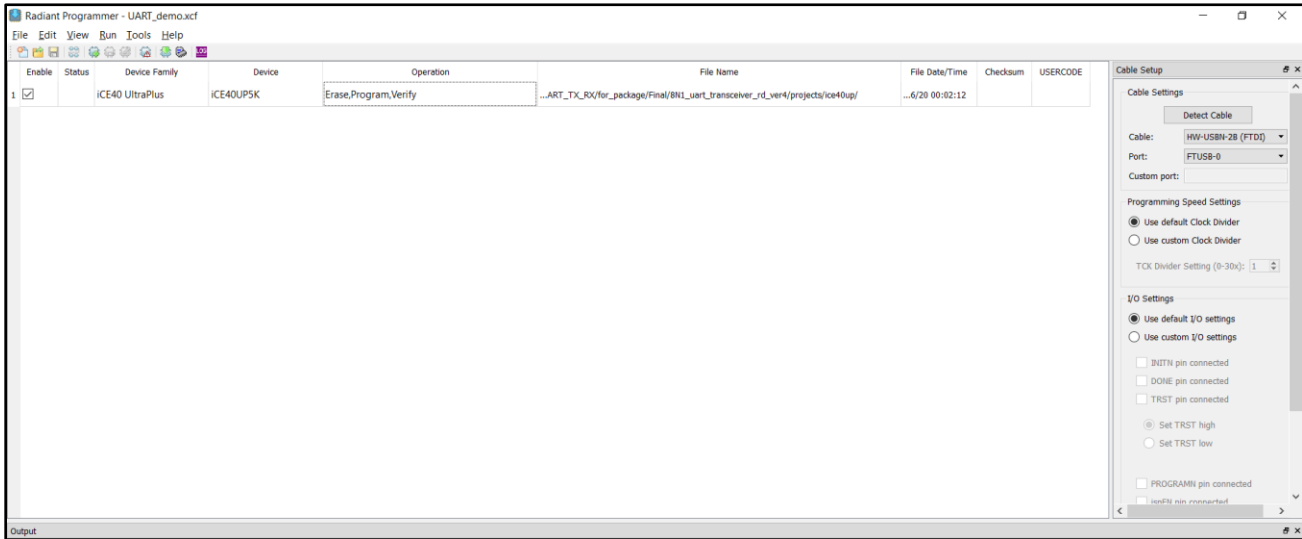


Figure 3.1. Programmer Settings



## 4. Programming the UART Demo

To program the UART demo:

1. Change **Target Memory** to **External SPI Flash Memory**.
2. Select **Erase, Program, Verify**.
3. Under **SPI Flash Options**, select the options below:
  - Family – SPI Serial Flash
  - Vendor – Winbond
  - Device – W25Q32
  - Package – 16-pin SOIC
4. To program the bitstream file, under the **Programming Options**, select the **UART\_demo\_bitstream.bin** in **Programming file**.

## 5. Running the UART Demo

To run the demo using UART Demo:

1. After programming the board, reset power(power cycle) the board by removing and re-inserting the micro USB cable.
2. Open the UART Demo Windows application.
3. Select detected port.
4. Select **9600** baudrate.
5. Click **Open Port**.
6. Enter a character or a string in the **Write box**.
7. Click the **Write** button.

The received character or string is reflected in the **Read box**.

**Note:** Serial 8-bit data transmitted and received is represented as UTF-8 in the application.

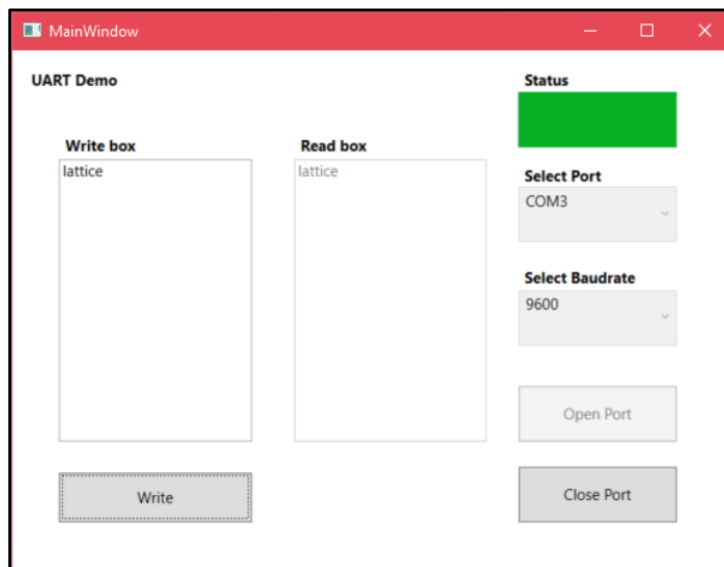
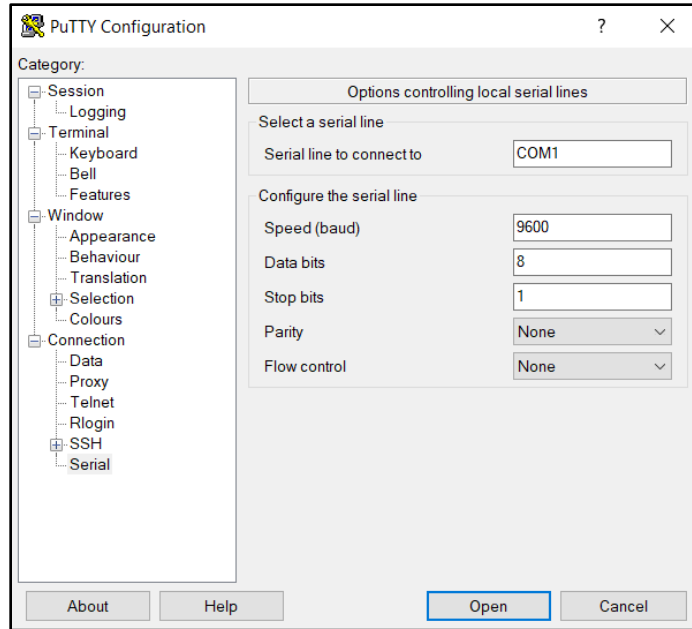


Figure 5.1. UART Windows Application

To run the demo using PuTTY:

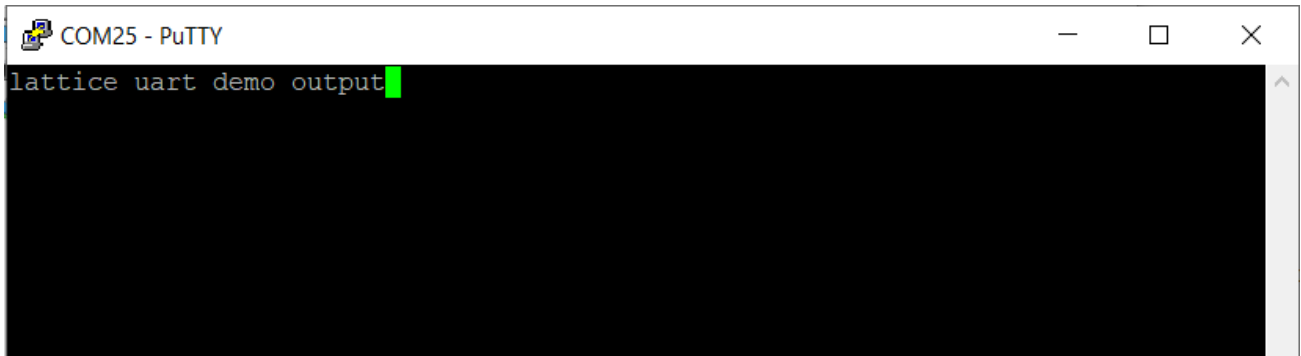
1. Download PuTTY from <https://www.putty.org/>.
2. Open PuTTY and set the configurations below.
  - Connection type – Serial
  - Speed(baud) – 9600
  - Data bits – 8
  - Stop bits – 1
  - Parity – None
  - Flow Control – None



**Figure 5.2. PuTTY Configuration**

3. Click **Open**.

Any pressed character is reflected in the terminal.



**Figure 5.3. PuTTY Terminal**

## 6. Packaged Demo Design

The demo ice40up folder contains five subfolders:

- demo\_project\_file – contains the Lattice Radiant® project file (.rdf), project strategy file (.sty), and IP instantiation file (.ipx) and source files used for demo;
- bitstream – contains the bitstream file (.bit) used for demo.
- docs – contains the demo user guide.
- Uart\_demo\_app – contains the Windows application for UART demo.

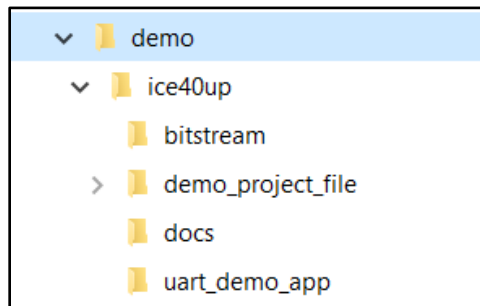


Figure 6.1. Demo Design Directory Structure

## References

For more information, refer to the following documents:

- [iCE40 UltraPlus Family Data Sheet \(FPGA-DS-02008\)](#)
- [Memory Usage Guide for iCE40 Devices \(FPGA-TN-02002\)](#)

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## Technical Support Assistance

Submit a technical support case through [www.latticesemi.com/techsupport](http://www.latticesemi.com/techsupport).

## Revision History

### Revision 1.0, October 2020

| Section | Change Summary   |
|---------|------------------|
| All     | Initial release. |



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