SLVS EC to MIPI CSI-2 with CertusPro-NX

Reference Design

FPGA-RD-02251-1.0

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CRC	Cyclic Redundancy Check
CSI-2	Camera Serial Interface 2
D-PHY	Physical Layer
DSI	Display Serial Interface
DT	Data Type
EBR	Embedded Block RAM
ECC	Error Correction Code
GPLL	General Purpose PLL
HS	High Speed
IP	Intellectual Property
LP	Low Power
LUT	Look Up Table
MIPI	Mobile Industry Processor Interface
MSB	Most Significant Bit
PLL	Phase Locked Loop
P2B	Pixel2Byte
RX	Receiver
SLVS-EC	Scalable Low Voltage Signaling with Embedded Clock
TX	Transmitter
VC	Virtual Channel
WC	Word Count

Supported Device and IP

This reference design supports the following devices with IP versions.

Device Family	Part Number	Compatible IP
CertusPro-NX	LFCPNX-100-7LFG672I	SLVS-EC Receiver IP version 1.2.0 Pixel-to-Byte Converter IP version 1.4.0 D-PHY Transmitter IP version 1.4.0

The IPs above are supported by Lattice Radiant™ software version 3.0.0.24.1 or later.

1. Introduction

The Mobile Industry Processor Interface (MIPI®) D-PHY is developed primarily to support camera and display interconnections in mobile devices, and it has become the industry's primary high-speed PHY solution for these applications in smartphones. It is used in conjunction with MIPI Camera Serial Interface-2 (CSI-2) and MIPI Display Serial Interface (DSI) protocol specifications. It meets the demanding requirements of low power, low noise generation, and high noise immunity that mobile phone designs demand.

MIPI D-PHY is a practical PHY for the typical camera, display applications and designed to replace traditional parallel buses based on LVCMOS or LVDS. However, many processors and displays/cameras still use RGB, CMOS, or MIPI Display Pixel Interface (DPI) as an interface.

The SLVS-EC to MIPI reference design allows the quick interface to receive serial data from CMOS Image Sensors and convert the incoming serial data to MIPI CSI-2 data format. The Lattice Semiconductor SLVS-EC to MIPI D-PHY Interface reference design provides this conversion for Lattice Semiconductor CertusPro™-NX devices. This is useful for wearable, tablet, human-machine interfacing, medical equipment, and many other applications.

1.1. Features List

The key features of the SLVS-EC to MIPI Reference Design are:

- Compliant with SLVS-EC Protocol specification v2.0
- Back compatibility with SLVS-EC Protocol specification v1.2
- Compliant with MIPI D-PHY v1.2, and MIPI CSI-2 v1.2 Specifications
- Supports MIPI CSI-2 interfacing up to 5 Gb/s for SLVS-EC and 6 Gb/s for Soft TX D-PHY
- Supports 1, 2, 4, 6, or 8 RX data lanes
- Supports 1, 2, or 4 MIPI TX D-PHY data lanes
- Supports low-power (LP) mode during the vertical and horizontal blanking
- Supports common MIPI CSI-2 compatible video formats (RAW8, RAW10, RAW12, RAW14, RAW16)

1.2. Block Diagram

Figure 1.1 shows the block level diagram of the SLVS-EC to MIPI Reference Design.

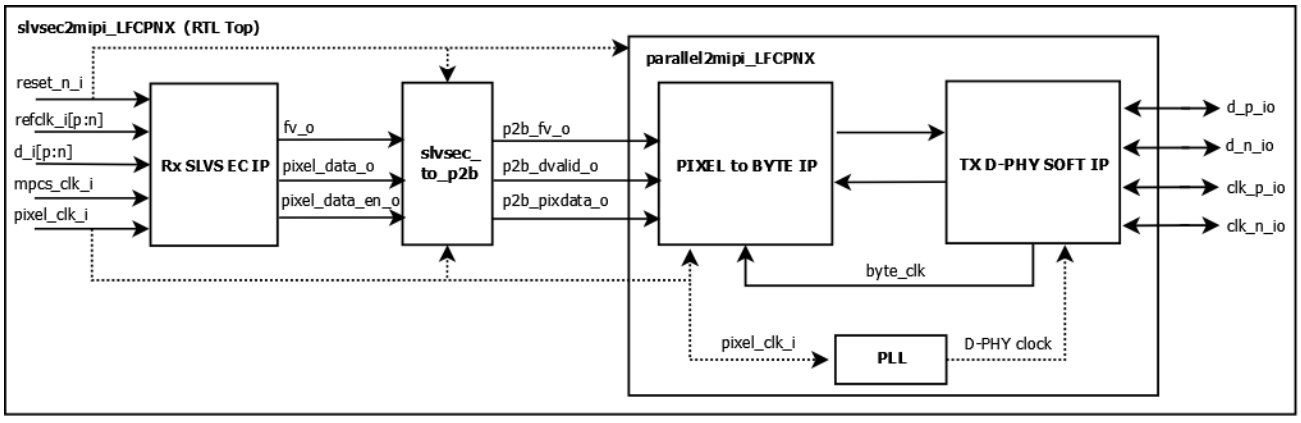

Figure 1.1. SLVS-EC to MIPI Reference Design Block Diagram

As shown in Figure 1.1, the block level diagram of the SLVS-EC to MIPI reference design mainly consists of the SLVS-EC IP, Pixel to Byte IP, and TX D-PHY IP. The pixel data output from SLVS EC IP given is to slvsec_to_p2b module that provides support to feed pixel data to Pixel to Byte IP as per its Byte data output extraction format. TX D-PHY IP requires input reference clock frequency between 24 MHz and 200 MHz, and GPLL used is to create an appropriate TX D-PHY clock frequency.

1.3. Functional Description

The SLVS-EC to MIPI D-PHY Reference Design converts incoming serial video data from the CMOS image sensor back into MIPI CSI-2 serial data format. The SLVS-EC receiver interface consists of two clock lanes and a configurable number of data lanes and as per the configured data type RAW10, provides frame valid, line valid, and parallel pixel data. The design converts this parallel output further from Pixel to byte and transmits the serial data over MIPI D-PHY lanes using TX-DPHY IP.

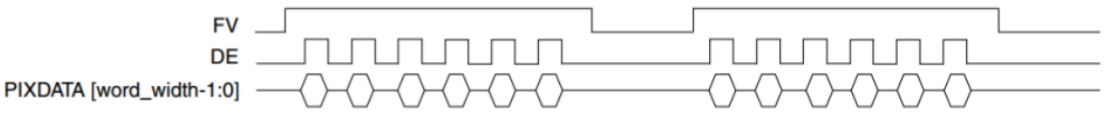

Figure 1.2. Camera Sensor Parallel Input Bus Waveform

This serial bus in Figure 1.2 is converted to the appropriate CSI-2 output format. The CSI-2 output serializes HS (High Speed) data, controls LP (Low Power) data, and transfers them through MIPI D-PHY IP. MIPI D-PHY also has a maximum of 5 lanes per channel. It consists of one clock lane and up to 4 data lanes. The maximum D-PHY data rate per lane is 1.5 Gb/s by TX Soft D-PHY IP.

1.4. Conventions

1.4.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL. This includes radix indications and logical operators.

1.4.2. Data Ordering and Data Types

The highest bit within a data bus is the most significant bit. 10-bit parallel data is serialized to a 1-bit data stream on each MIPI D-PHY data lane where bit 0 is the first transmitted bit.

Table 1.1 lists pixel data order coming from core module.

Table 1.1. Pixel Data Order

Data Type	Format
RAW	RAW [MSB: 0]

1.4.3. Signal Names

Signal names that end with:

- _n are active low
- _i are input signals
- Some signals are declared as bidirectional (I/O) but are only used as input. Hence, _i identifier is used.
- _o are output signals
- Some signals are declared as bidirectional (I/O) but are only used as output. Hence, _o identifier is used.
- _io are bidirectional signals

2. Parameters and Port List

There are two directive files for this reference design:

- synthesis_directives.v – used for design synthesis by Lattice Radiant software and simulation
- simulation_directives.v – used for simulation

These directives can be modified according to the required configuration. The settings in these files must match SLVS-EC IP, Pixel to Byte IP, and TX D-PHY IP settings created by Lattice Radiant.

2.1. Synthesis Directives

Table 2.1 shows the synthesis directives that affect this reference design. They are used for both synthesis and simulation. Some restricted parameter selections are by other parameter settings as shown in Table 2.1 and Table 2.2.

Table 2.1. Synthesis Directives

Category	Directive	Remarks
Number of RX Lane	NUM_RX_LANE_1	Only one of these directives must be selected as per SLVS-EC lanes configuration
	NUM_RX_LANE_2	
	NUM_RX_LANE_4	
Number of Bits per Pixel lane	BIT_PER_PIXEL {value}	Number of Bits per Pixel lane for SLVS EC, Set value {n} for Raw{n} data type.
Pixel count per line	LINE_LENGTH {value}	Number of pixels count in SLVS-EC, Set to 1920.
Baud Grade	BAUD_GRADE_1	Only one of these directives must be selected as per SLVS-EC baud grade configuration
	BAUD_GRADE_3	
	BAUD_GRADE_3	
D-PHY Type	TX_CSI2	SLVS-EC supports only CSI-2. Hence, always CSI-2 is used for transmission.
Video Data Type	RAW8	Type of video data to convert from Serial to Pixel for SLVS –EC and from pixel format to byte format for Pixel to Byte converter, always RAW8 used.
Number of TX Lane	NUM_TX_LANE_1	Only one of these directives must be selected as per TX DPHY lanes configuration
	NUM_TX_LANE_2	
	NUM_TX_LANE_4	
Number of Pixels Per Pixel Clock	NUM_PIX_LANE_1	Only one of these four directives must be defined, Number of pixels per pixel clock used for the input to the Pixel to Byte converter
	NUM_PIX_LANE_2	
	NUM_PIX_LANE_4	
	NUM_PIX_LANE_6	
TX D-PHY Clock Gear	TX_GEAR_8	TX D-PHY Clock Gear always will be Gear 8
Miscellaneous	TX_CSI2	Enables internal signals monitored by test-bench. Always will be ON
Number of Pixels	NUM_PIXELS {value}	Number of active Pixels per Line, set to 1920
Clock Mode	TX_CLK_MODE_HS_ONLY	TX D-PHY Clock mode, only one of these two directives must be defined
	TX_CLK_MODE_HS_LP	
Use GPLL	USE_GPLL	Always defined to generate D-PHY clock frequency for TX D-PHY

Note: HS_LP mode means *non-continuous clock mode* and HS_ONLY means *continuous clock mode* for the TX D-PHY.

2.2. Simulation Directives

Table 2.2 shows the simulation directives for this reference design.

Table 2.2. Simulation Directives

Category	Directive	Remarks
Pixel clock period	PIX_CLK {value}	Pixel clock period in ns
Number of video frames	NUM_FRAMES {value}	Number of video frames to be transmitted
Number of lines per frame	NUM_LINES {value}	Number of active lines per frame
Horizontal Front Porch	HFRONT {value}	Number of blanking cycles before HSYNC signal is asserted
Horizontal Back Porch	HBACK {value}	Number of blanking cycles after HSYNC signal is de-asserted
Vertical Front Porch	VFRONT {value}	Number of blanking lines before VSYNC signal is asserted
Vertical Back Porch	VBACK {value}	Number of blanking lines after VSYNC signal is de-asserted

2.3. Top-Level I/O

Table 2.3 shows the top-level I/O of this reference design. Actual I/O depends on the customer's configurations and compiler directives automatically declare all necessary I/O ports.

Table 2.3. SLVS-EC to MIPI Top Level I/O

Port Name	Direction	Description
Clocks and Reset		
pixel_clk_i[1]	I	Pixel clock input
reset_n_i	I	Active low asynchronous reset
refclk_p_i	I	Differential Reference Clock, CLK+
refclk_n_i	I	Differential Reference Clock, CLK-
mpcs_clkin_i	I	Clock source for PMA in SLVS-EC IP, Use 125 MHz
mpcs_pwrdn_i	I	PHY power down 2'b00: Operational 2'b10: Low-power state. Rx CDRPLL is powered-down. The PHY starts in this low-power mode to perform calibration. 2'b11: Deep low-power state. TX driver is in electrical Idle II (static low). All PLLs are powered down and clock shutdown.
Primary IO		
d_p_i	I	Differential Reference Clock, CLK+
d_n_i	I	Differential Reference Clock, CLK-
setup_i	I	Active high setup signal from Client-side interface to commence start-up for SLVS-EC
APB Interface		
apb_pclk_i	I	APB clock, Use 125 MHz
apb_preset_n_i	I	APB active low reset
apb_paddr_i	I	Address signal
apb_psel_i	I	Select signal. This indicates that the slave device is selected and a data transfer is required.
apb_penable_i	I	Enable signal. Indicates the second and subsequent cycles of an APB transfer
apb_pwdata_i	I	Write data signal
apb_pwrite_i	I	Direction signal, Write = 1, Read = 0
apb_pready_o	O	Ready signal shows transfer completion. Slave uses this signal to extend an APB transfer.
apb_prdata_o	O	Read data signal

Port Name	Direction	Description
MIPI DPHY TX Interface		
d_p_io[NUM_TX_LANE -1:0][2]	I/O	Positive differential TX D-PHY data lanes
d_n_io[NUM_TX_LANE -1:0][2]	I/O	Negative differential TX D-PHY data lanes
clk_p_io	I/O	Positive differential TX D-PHY clock lane
clk_n_io	I/O	Negative differential TX D-PHY clock lane
Miscellaneous		
pll_lock_o	O	GPLL lock output

Notes:

1. Available only if Native interface is enabled in SLVS-EC IP
2. NUM_TX_LANE = Number of TX D-PHY Lanes: 1, 2, 4 (available on user interface)

3. Design and Module Description

The top-level design (slvsec2mipi_LFCPNX.v) consists of the following modules:

- rx_slvs_ec
- slvsec_to_p2b
- p2b
- tx_dphy
- int_pll

The design uses external PLL support on defining USE_GPLL according to Soft TX D-PHY configuration.

Figure 3.1 shows the timing diagram for the D-PHY TX Input Bus for Long Packet Transmission in CSI-2 Interface.

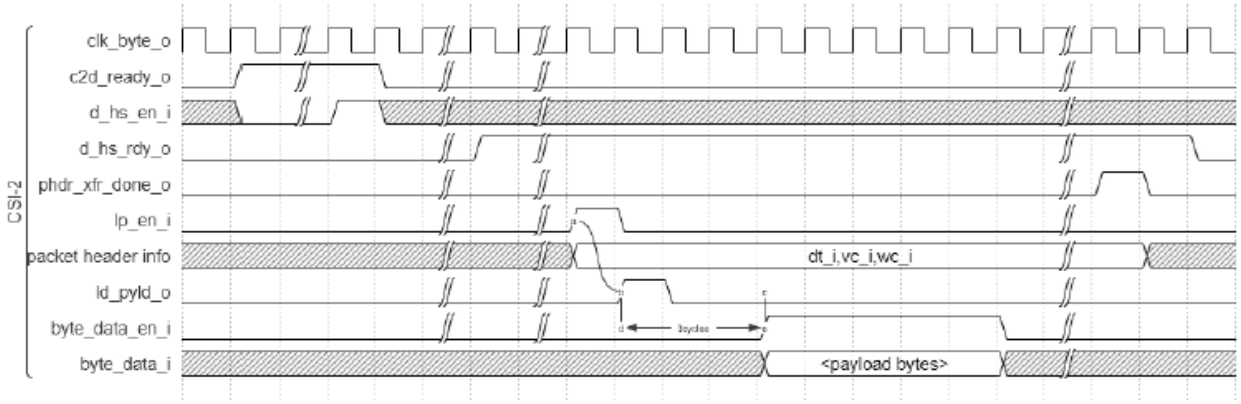

Figure 3.1. D-PHY Tx Input Bus for Long Packet Transmission in CSI-2 Interface

When the protocol type 'CSI-2' selected, there is no internal buffer to save the incoming payload data before the creation of the header packet. Because of this, the D-PHY TX IP requires 3 cycles from the assertion of the ld_pyld_o to the arrival of the valid payload data. The ld_pyld_o asserts the next cycle after the detection of the lp_en_i. Hence, little glue logic is added in the top-level design to take care of this timing requirement for the required signals for the D-PHY TX IP as shown in Figure 3.1.

3.1. rx_slvs_ec

Create this module to receive serial data from the CMOS image sensor and convert it into parallel pixel data output according to configurations, such as RX lanes, Data Type, Baud grade, and others. Figure 3.2 shows an example of IP GUI interface settings in Lattice Radiant for the RX SLVS-EC IP. Refer to SLVS-EC Receiver IP Core User Guide (FPGA-IPUG-53090) for details.

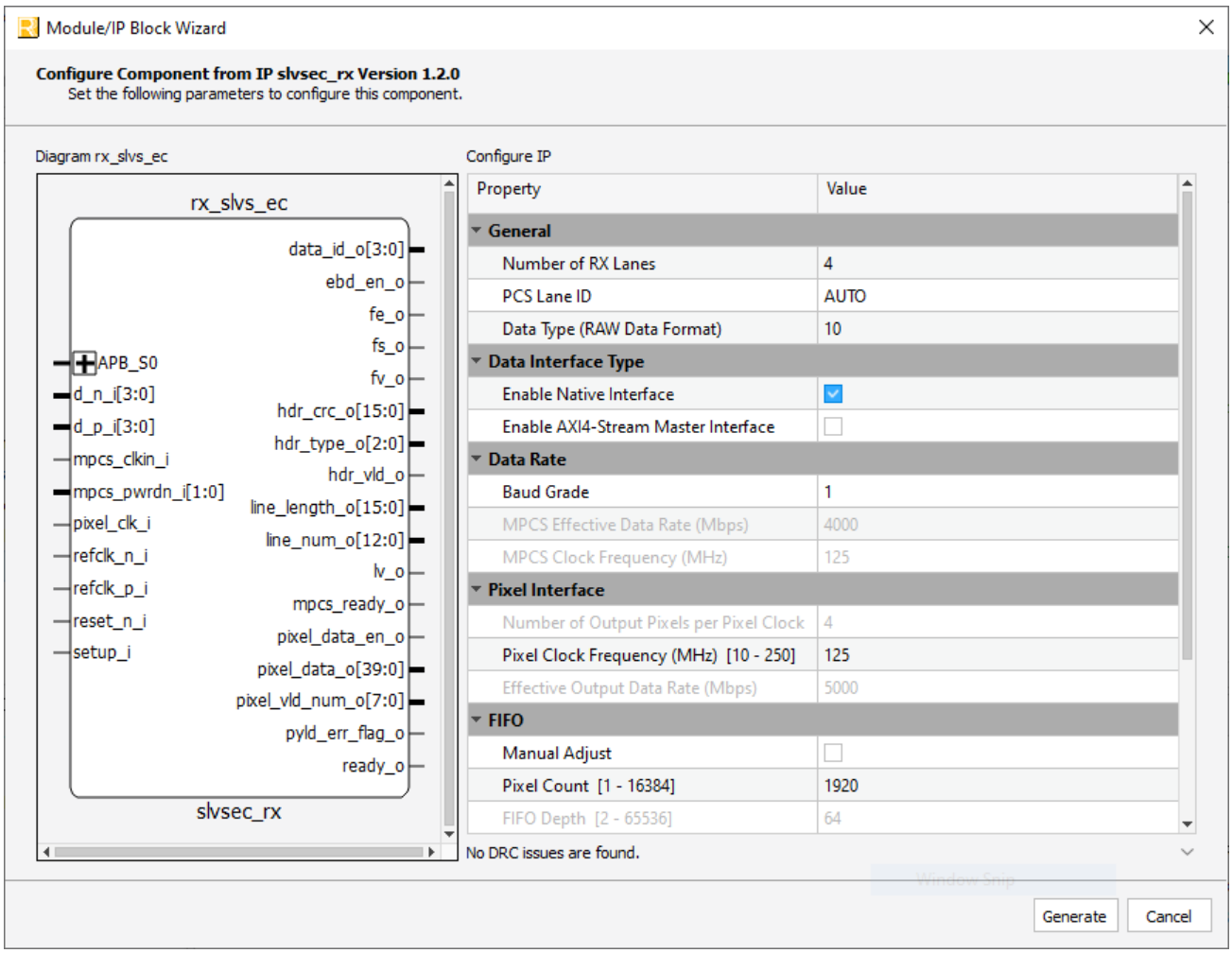

Figure 3.2. rx_slvs_ec IP Creation in Lattice Radiant

The following shows the guidelines and the required parameter settings for this reference design:

- Number of RX Lanes – Select 1,2,4,6 or 8 as per configuration
- PCS Lane ID – Always use AUTO
- Data Type – Select as 8,10,12,14 or 16 as per configuration. These indicate RAW data types.
- Enable Native Interface – Always enabled (checked)
- Enable AXI4-Stream Master Interface – Always disabled (unchecked)
- Baud grade – Select as 1,2 or 3 as per configuration
- Pixel Clock Frequency – Recommended by IP is always 125 MHz. Value changes as per Baud grade selection.
- Pixel count – Set as 1920
- Enable Header Analysis – Always enabled (checked)
- Enable Miscellaneous signals – Always disabled (unchecked)

Note: RXSLVS-EC IP supports only MIPI CSI-2 DPHY type data transfer. Hence, the D-PHY interface type in Pixel to Byte and TX D-PHY IPs also should be always set as CSI-2 only.

The .ipx file is included in the projects (rx_slvs_ec/rx_slvs_ec.ipx) to reconfigure the IP as per the user configuration requirements. If this IP is required to create from scratch, recommended is to set the design name to *rx_slvs_ec* so that it is not required to modify the instance name of this IP in the top-level design as well in the simulation setup file.

3.2. p2b

Create this module to convert Pixel data into Byte data output according to configurations, such as TX Interface, Data Type, number of TX Lanes, and others. Figure 3.3 shows an example of IP GUI interface settings in Lattice Radiant for the Pixel to Byte IP. Refer to Pixel-to-Byte Converter IP Core User Guide (FPGA-IPUG-02094) for details.

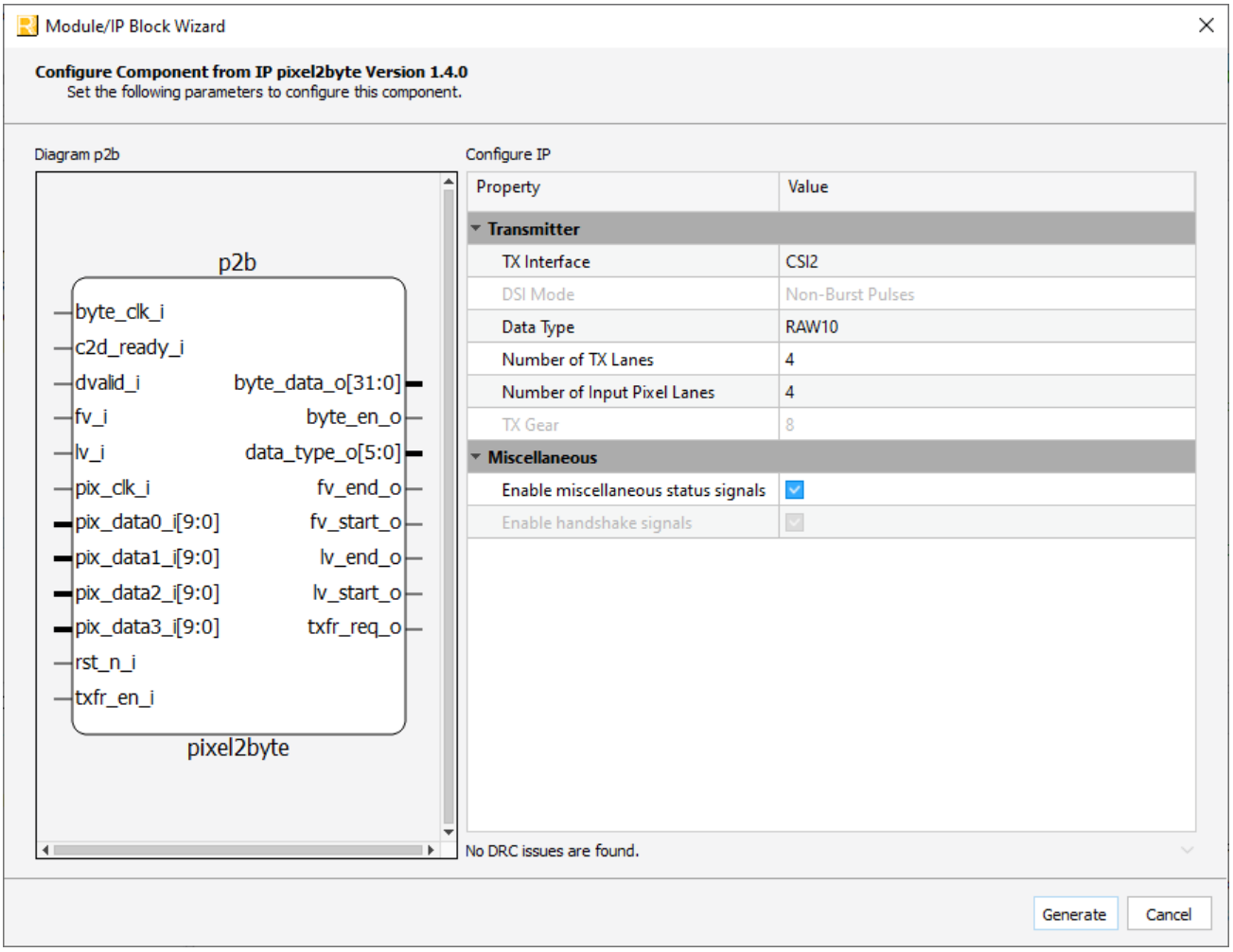

Figure 3.3. p2b IP Creation in Lattice Radiant

The following shows the guidelines and the required parameter settings for this reference design:

- TX Interface – Always select CSI-2.
- Data Type – Select RAW8, RAW10, RAW12, RAW14, or RAW16 for CSI-2, others are not supported in this reference design
- Number of TX Lanes – Select 1, 2, or 4. Set the same value as TX D-PHY IP.
- Number of Input Pixel Lanes – Select 1, 2, 4, and 6 for input Pixel per clock. Number of Input Pixel Per Clock 6 is only supported for CSI-2, RAW10, and RAW12.
- TX Gear – Always select 8
- Enable miscellaneous status signals – Select the checkbox to enable (checked).

The Pixel-to-Byte Converter IP converts the standard pixel data format to the D-PHY CSI-2 standard-based byte data stream. The .ipx file is included in the projects (p2b/p2b.ipx) to reconfigure the IP as per the user configuration requirements. If this IP is required to create from scratch, recommended is to set the design name to *p2b* so that it is not required to modify the instance name of this IP in the top-level design as well as in the simulation setup file.

3.3. slvsec_to_p2b

This module works as a bridge between SLVS EC IP and Pixel to Byte IP to avoid any data mismatch in the design. It receives Pixel data output from SLVS EC IP, re-arranges the pixel data as per configured RX and TX Lanes, and this new pixel data is sent to Pixel to Byte IP. For example, consider RAW10 based one lane SLVS EC to one lane TX D-PHY design for which the 10 Bits sequential pixel data output and its equivalent binary conversion is shown below using pixel naming for a better understanding.

Pixel Naming	SLVS EC Pixel data output	Equivalent Binary format
[9:0]Pixel0	10'h242	10'b1001000010
[9:0]Pixel1	10'h13B	10'b0100111011
[9:0]Pixel2	10'h171	10'b0101110001
[9:0]Pixel3	10'h284	10'b1010000100

The slvsec_to_p2b module receives and stores this incoming sequential pixel data. It then generates new Pixel data by using LSB Bits from bottom to top pixels and re-arranging them as shown below.

New Pixel	New re-arranged Pixel data	Equivalent Binary format
[9:0]P0	{[9:2]Pixel0,[1:0]Pixel3} = 10'h240	10'b1001000000
[9:0]P1	{[9:2]Pixel1,[1:0]Pixel2} = 10'h139	10'b0100111001
[9:0]P2	{[9:2]Pixel2,[1:0]Pixel1} = 10'h173	10'b0101110011
[9:0]P3	{[9:2]Pixel3,[1:0]Pixel0} = 10'h286	10'b1010000110

This re-arrangement logic supports Pixel to Byte IP as per its Byte data output generation format and obtain valid byte data in output to avoid data mismatch. This module takes care of Pixel generation for all supported combinations of this reference design as shown in the Known Limitations section.

3.4. tx_dphy

Create this module according to the channel conditions, such as the number of lanes, bandwidth, and others. Figure 3.4 and Figure 3.5 show an example IP GUI interface setting in Lattice Radiant for the CSI-2 D-PHY Transmitter IP. Refer to CSI-2/DSI D-PHY Tx IP Core User Guide (FPGA-IPUG-02080) for details.

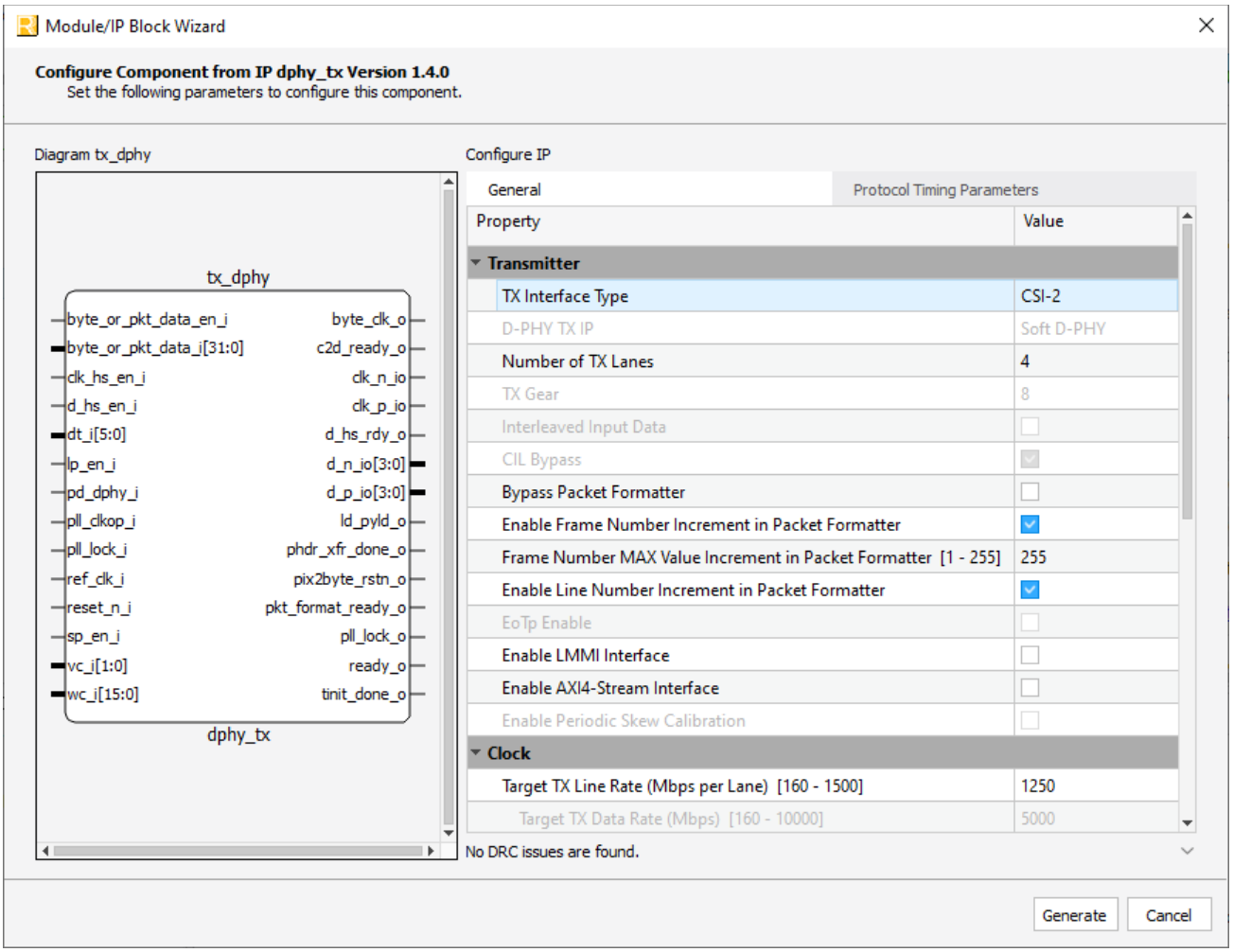

Figure 3.4. tx_dphy IP Creation in Lattice Radiant (1/2)

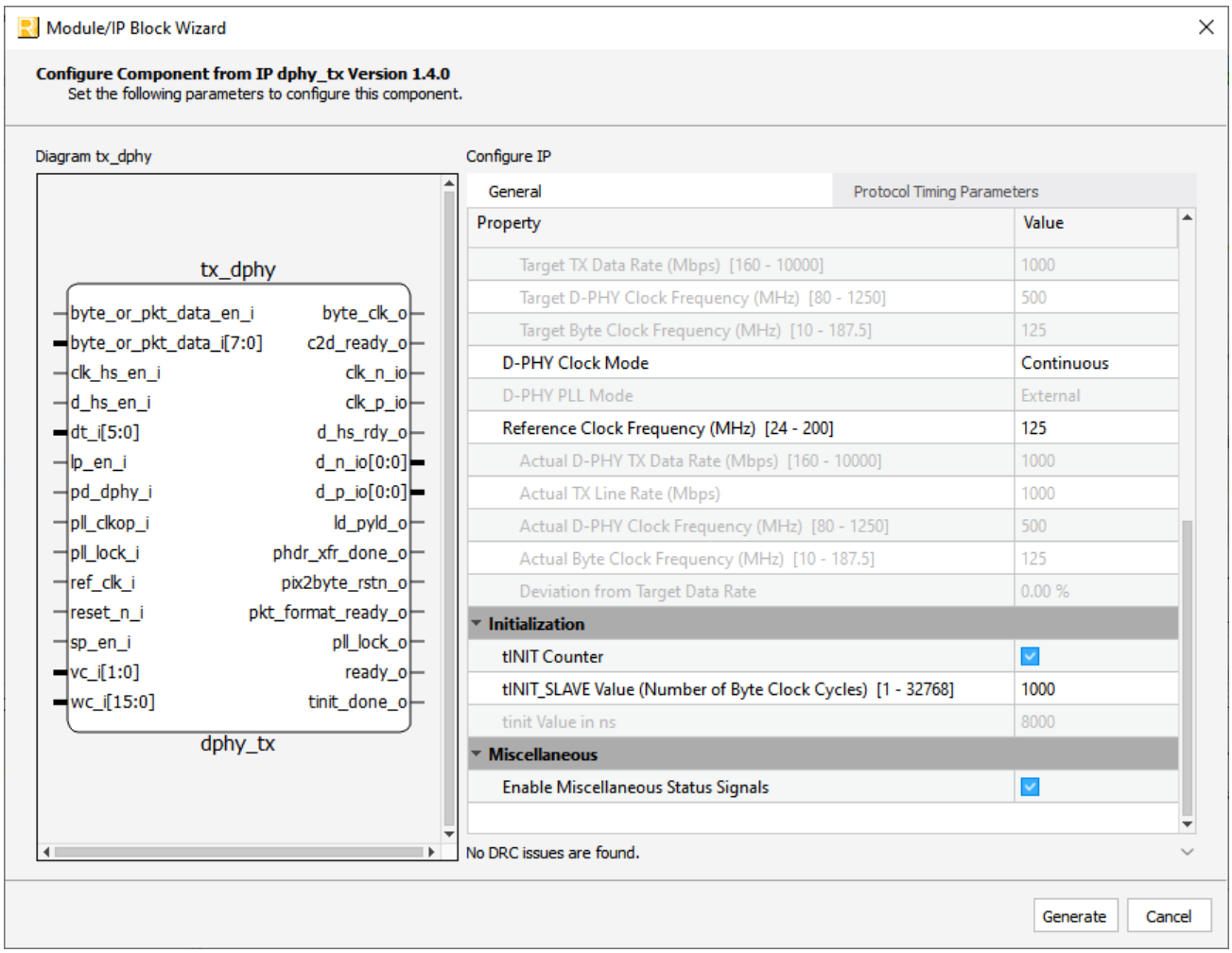

Figure 3.5. tx_dphy IP Creation in Lattice Radiant (2/2)

The following shows the guidelines and required parameter settings for this reference design:

- TX Interface Type – Always select CSI-2
- D-PHY TX IP – CertusPro-NX by default supports only Soft DPHY type.
- Number of TX Lanes – Select 1, 2, or 4 according to the required configuration
- TX Gear – Always 8, since the D-PHY type supported by the device is Soft D-PHY only. Lattice Radiant automatically selects TX Gear 8 when the lane bandwidth is less than 1500 Mbps, which means the TX byte clock could be ~187.5 MHz.
- Bypass Packet Formatter – Always disabled (unchecked)
- Enable Frame Number Increment in Packet Formatter – Select checkbox to enable (checked), only for CSI-2
- Frame Number MAX Value Increment in Packet Formatter [1 - 255] – Numerical value between 1 to 255, only for CSI-2
- Enable Line Number Increment in Packet Formatter – Select checkbox to enable (checked), only for CSI-2
- Enable LMMI Interface – Always disabled (unchecked)
- Enable AXI4-Stream Interface – Always disabled (unchecked)
- TX Line Rate per Lane (Mbps) [160 – 1500] (Soft D-PHY) – Set according to the required configuration
- D-PHY Clock Mode – Set Continuous or Non-continuous according to the required configuration
- Reference Clock Frequency (MHz) [24 – 200] – Set the same value as pixel clock frequency
- tINIT Counter – Always enabled (checked) and use tINIT_SLAVE VALUE always 1000.
- Enable Miscellaneous Status Signals – Always enable (checked)

The default values are recommended in the Protocol Timing Parameters window of this IP. This module takes the byte data and outputs CSI-2 data after serialization in CSI-2 High-Speed mode. The .ipx file is included in the project (tx_dphy/tx_dphy.ipx) to reconfigure the IP as per the user configuration requirements. If this IP is required to create from scratch, it recommended is to set the design name to *tx_dphy* so that it is not required to modify the instance name of this IP in the top-level design as well as a simulation setup file.

3.5. int_pll

Create this module to generate the required TX D-PHY clock frequency (clkop_o) for Soft TX D-PHY IP as per the equation mentioned below. Figure 3.6 shows an example IP GUI interface setting in Lattice Radiant for the PLL IP. Refer to PLL Module User Guide (FPGA-IPUG-02063) for details.

TX D-PHY clock frequency = (TX D-PHY Line rate / 2) MHz

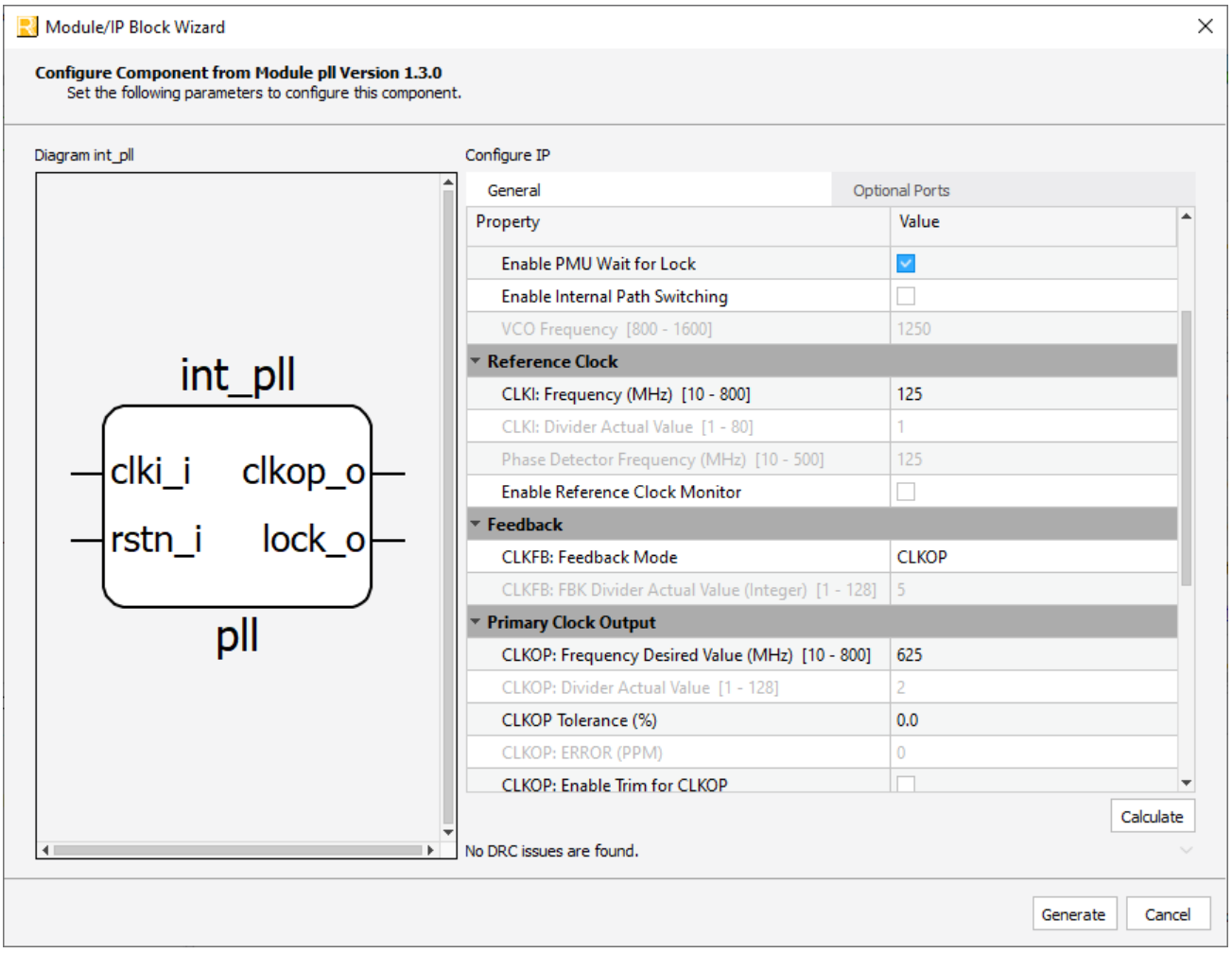

Figure 3.6. int_pll IP Creation in Lattice Radiant

Modify the reference clock frequency and the clkop_o frequency as per the required configurations. The .ipx file is included in this project (int_pll/int_pll.ipx) to reconfigure the IP as per the user configuration requirements. If this IP is required to create from scratch, recommended is to set the design name to int_pll so that it is not required to modify the instance names of IPs in the top-design file.

4. Design and File Modifications

This reference design uses version 1.2.0 of the SLVS EC IP, version 1.4.0 of the Pixel2Byte IP, and version 1.4.0 of the TX D-PHY IP. Some modifications are required depending on user configuration in addition to two directive files (synthesis_directives.v and simulation_directives.v).

4.1. Top level RTL

The current top-level file (slvsec2mipi_LFCPNX.v) integrates all the above-mentioned design IPs required for this reference design. The GPLL setting in the current sub-level file (parallel2mipi_LFCPNX.v) corresponds to the configuration selected for this reference design. According to the configuration, modify the GPLL instantiation as described in Section 3.5. In addition, modify the instance names of RX SLVS-EC (rx_slvs_ec), Pixel to Byte (p2b), TX D-PHY (tx_dphy) and internal GPLL (int_pll) if this IP(s) is created with different name(s).

5. Design Simulation

The script file (slvsec_to_mipi_LFCPNX_msim.do) and testbench folder are provided to run the functional simulation using ModelSim. Follow the naming recommendations regarding design name and instance name when the required IPs are created by Lattice Radiant, the following are the only changes required in the script file:

- User project directory

```
### Set Customer's project/simulation directory ###

set project_dir ~/Desktop/rd_SLVS_EC_to_MIPI_CSI2_LFCPNX
set sim_dir     $project_dir/simulation/lfcpnx
```

Own project directory

Figure 5.1. Script Modification #1

```
### Compiling modules ###
vlog -mfcu -suppress 2388 \
+incdir+"$project_dir/rx_slvs_ec/rtl/" \
+incdir+"$project_dir/p2b/rtl/" \
+incdir+"$project_dir/tx_dphy/rtl/" \
+incdir+"$project_dir/int_pll/rtl/" \
+incdir+"$project_dir/source/verilog/lfcpnx/" \
+incdir+"$project_dir/testbench/verilog/" \
$project_dir/source/verilog/lfcpnx/synthesis_directives.v \
$project_dir/testbench/verilog/simulation_directives.v \
$project_dir/rx_slvs_ec/rtl/rx_slvs_ec.v \
$project_dir/p2b/rtl/p2b.v \
$project_dir/tx_dphy/rtl/tx_dphy.v \
$project_dir/int_pll/rtl/int_pll.v \
$project_dir/source/verilog/lfcpnx/slvsec2mipi_LFCPNX.v \
$project_dir/source/verilog/lfcpnx/slvsec_to_p2b.v \
$project_dir/source/verilog/lfcpnx/parallel2mipi_LFCPNX.v \
$project_dir/testbench/verilog/slvsecrx_test.v \
$project_dir/testbench/verilog/slvsec_model.v \
$project_dir/testbench/verilog/slvsec_driver.v \
$project_dir/testbench/verilog/dphy_checker.v \
$project_dir/testbench/verilog/slvsec_to_mipi_LFCPNX_tb.v \

vsim -voptargs=+acc=ap work.slvsec2mipi_LFCPNX_tb -L pmi_work -L ovi_lfcpnx \
-c -do "add wave -r slvsec2mipi_LFCPNX_tb/* ;run -all; quit" -t fs -suppress 2685,3015,3085,3722
```

Figure 5.2. Script Modification #2

Modify the simulation_directives.v according to the required configuration (refer to Simulation Directives for details). By executing the script in ModelSim, compilation and simulation execute automatically. The test-bench slvsec2mipi_LFCPNX_tb.v instantiates the top-level design module, generates the stimulus video data, and does the data comparison between the expected data and output data from the RD, including Frame Number, EoT Packet check, CRC check, EoTp (Long Packet and Short Packet), ECC, and timing parameters of TX D-PHY. Figure 5.3 shows the following statements when the simulation is completed.

```
#    Time: 659982 ns  Iteration: 0  Instance: /slvsec2mipi_LFCPNX_tb
#               659982   ---------------------------------------------
#               659982   ##### DATA COMPARING IS STARTED #####
#               659982   ---------------------------------------------
#               659982   ***PASS : EOT PACKET CHECK***
#               659982   ***PASS : SYNC CHECK
#               659982   ***PASS : ECC
#               659982   ***PASS : FRAME NO
#               659982   ***PASS : CRC***
#               659982   Test fail count : 0
#
#               659982  -------------------------------------------------------
#               659982  ----------------- SIMULATION PASSED -------------------
#               659982  -------------------------------------------------------
#               664982   TEST END
#
#
# ========================================
# Simulation Done
# ========================================
```

Figure 5.3. Simulation Done Statement

The test-bench generates other debug files during simulation like *input_data.log*, *output_data.log,* and *dphy_checker_timing.log* for debugging purposes. The *input_data.log* file stores the data transmitted by the test-bench to RX SLVS-EC. The *output_data.log* file stores the data received to the test bench from TX D-PHY. The testbench compares both of these files. The *dphy_checker_timing.log* file stores all the timing parameters (such as LP-11, TLPX, HS-prepare, HS-0, and HS-Trail) and gives an error if any timing parameter fails. The same file also saves timing of Header Packet received and Header Packet values like DT, VC, WC, and ECC

Figure 5.4 shows the SLVS EC simulation waveform of the full view of two lines and two frames for the CSI-2 interface. Figure 5.5 shows the zoom view of the simulation waveform shown in Figure 5.4 for the CSI-2 interface.

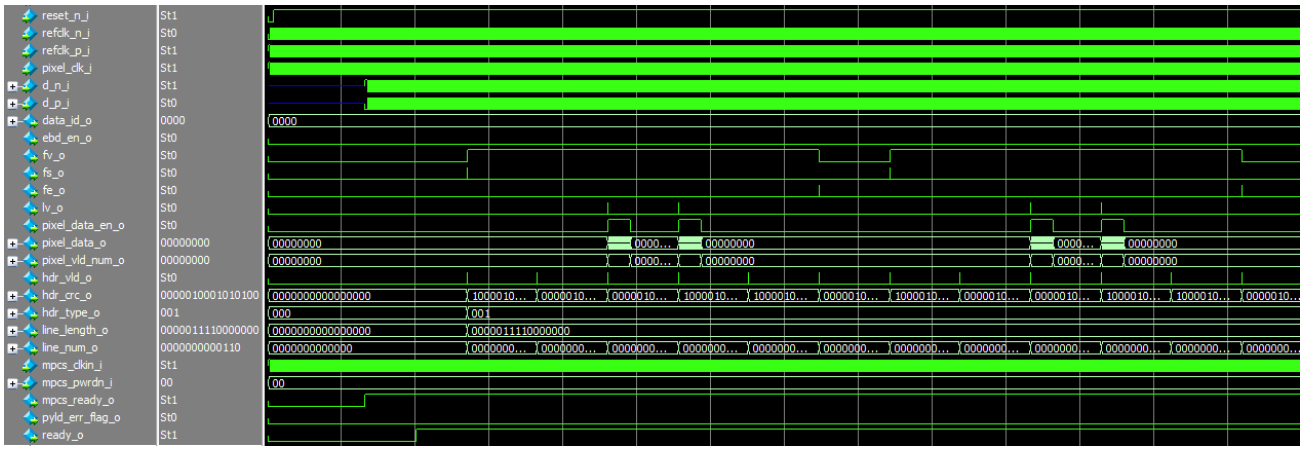

Figure 5.4. Simulation Waveform for CSI-2 (1/2)

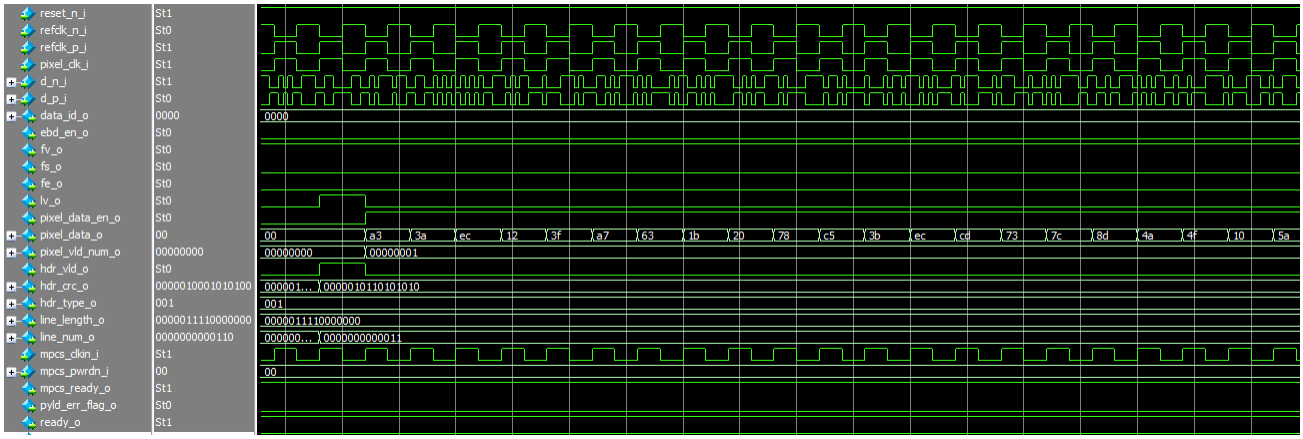

Figure 5.5. Simulation Waveform for CSI-2 (2/2)

The simulation waveform can be by opening the vsim.wlf file in the ModelSim from the simulation directory. More signals can be added from different modules to the waveform as required.

6. Known Limitations

The following are the limitations of this reference design:

- RX SLVS-EC supports only the MIPI CSI-2 D-PHY interface.

Table 6.1 shows the combinations of RX SLVS-EC Data type, Lanes, and Baud grade currently supported by the design.

Table 6.1. Combinations of RX SLVS EC Type

Data type	Number of RX SLVS-EC Lanes	Baud Grade	Number of TX Lanes in P2M and TX D-PHY
RAW8	1	1	1
			2
			4
	1	2	2
			4
	2	1	4
RAW10	1	1	1
			2
			4
	1	2	2
		2	4
		3	4
	2	1	2
		1	4
		2	4
	4	1	4
RAW12	1	1	1

7. Design Package and Project Setup

The SLVS-EC to MIPI with CertusPro-NX Reference Design is available on www.latticesemi.com. Figure 7.1 shows the directory structure. The targeted design is for LFCPNX-100-7LFG672I. synthesis_directives.v and simulation_directives.v are set to configure the design with the following configuration:

- RX : CSI-2, 4-lane, RAW10 with 4 pixel/clock
- TX: CSI-2, 4-lane, Gear 8 with Soft D-PHY in continuous clock mode

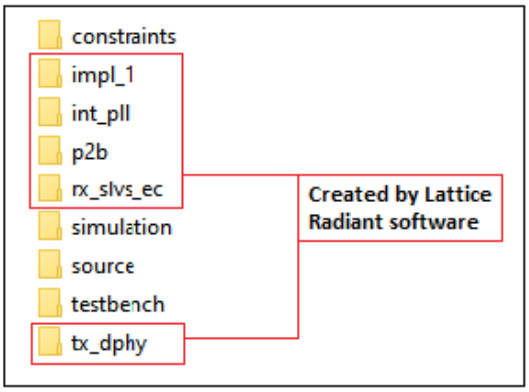

Figure 7.1. Directory Structure

Figure 7.2 shows the design files used in the Lattice Radiant project. Including PLL, Lattice Radiant creates four .ipx files. By specifying slvsec2mipi_LFCPNX as a top-level design, the tool ignores all unnecessary files. Constraint file (slvsec_to_mipi_LFCPNX.pdc) is also included in the project for reference.

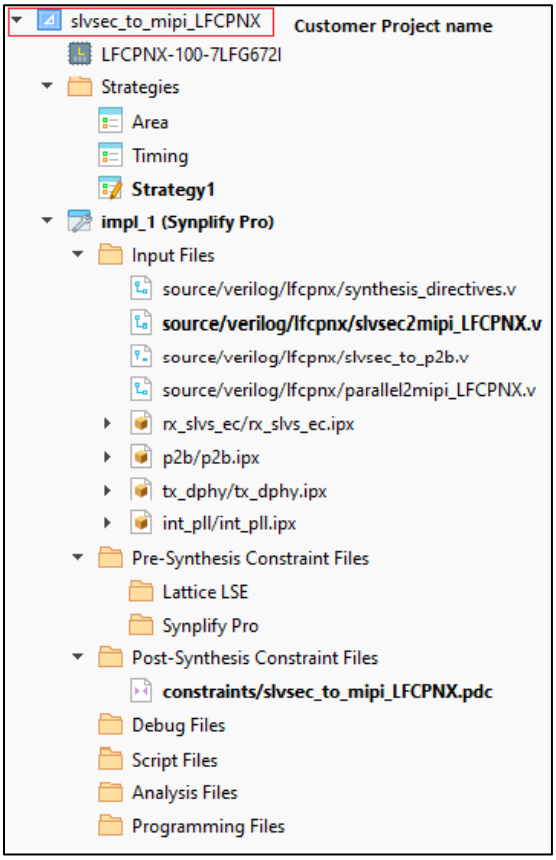

Figure 7.2. Project Files

8. Resource Utilization

Resource utilization depends on the configuration used. Table 8.1 shows resource utilization examples under certain configurations targeting LFCPNX-100. This is just a reference and actual usage varies.

Table 8.1. Resource Utilization Examples

Configuration	LUT (Utilization/Total)	FF (Utilization/Total)	EBR (Utilization/Total)	I/O (Utilization/Total)
CSI-2, RAW10,4-Rx lane, 4 Pixel/clock, Baud grade 1, 4-Tx lane, Gear 8, Soft D-PHY	9488/79872	4710/80769	11/208	119/299
CSI-2, RAW10,1-Rx lane, 1 Pixel/clock, Baud grade 1, 1-Tx lane, Gear 8, Soft D-PHY	3926/79872	2275/80769	3/208	113/299
CSI-2, RAW8,1-Rx lane, 1 Pixel/clock, Baud grade 1, 1-Tx lane, Gear 8, Soft D-PHY	3859/79872	2167/80769	3/208	113/299
CSI-2, RAW8,1-Rx lane, 1 Pixel/clock, Baud grade 1, 2-Tx lane, Gear 8, Soft D-PHY	3930/79872	2253/80769	3/208	115/299
CSI-2, RAW8,1-Rx lane, 1 Pixel/clock, Baud grade 2, 1-Tx lane, Gear 8, Soft D-PHY	5295/79872	2602/80769	3/208	115/299
CSI-2, RAW8,1-Rx lane, 1 Pixel/clock, Baud grade 2, 2-Tx lane, Gear 8, Soft D-PHY	5355/79872	2671/80769	3/208	115/299

References

- MIPI Alliance Specification for D-PHY Version 1.2
- MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2) Version 1.2
- SLVS-EC Receiver IP Core User Guide (FPGA-IPUG-02125)
- Pixel-to-Byte Converter IP Core User Guide (FPGA-IPUG-02094)
- CSI-2/DSI D-PHY Tx IP Core User Guide (FPGA-IPUG-02080)
- PLL Module User Guide (FPGA-IPUG-02063)

For more information on the CertusPro-NX FPGA device, visit https://www.latticesemi.com/Products/FPGAandCPLD/CertusPro-NX

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow, Tasks, and Simulation Flow, see the Lattice Radiant User Guide.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, March 2022.

Section	Change Summary
All	Initial release.

www.latticesemi.com