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1. Introduction

Sony introduced the IMX036 and IMX136 sensors to support resolutions up to 1080P60 and 1080p120 respectively. A traditional CMOS parallel interface could no longer handle the bandwidth requirements of these sensors. To support the higher resolutions and frame rates, Sony utilizes a parallel DDR sub-LVDS interface. This 10/12-bit parallel sub-LVDS DDR interface can operate up to 1080p60 at 148.5 Mbps on the IMX036 and 1080p120 at 297 Mbps on the IMX136. The Lattice Sub-LVDS-to-Parallel Sensor Bridge converts the low voltage sub-LVDS DDR output of the IMX036 and IMX136 to a standard CMOS parallel interface.

The IMX036 is capable of outputting a 3.27 megapixel image. The IMX136 is capable of 2.3 megapixel image. For more technical details regarding the image sensor, please contact Sony. This reference design does the following:

1. Converts parallel data from the LVDS DDR input to SDR data (LVCMOS interface) and generates the output clock (phase adjustable) at twice the frequency of the input clock with a PLL.
2. Extracts EAV and SAV from the SDR data and generates xhs and xvs. All valid and invalid SAV/EAV sync codes are detected and used to generate these active video control lines.

Figure 1.1 shows the block diagram for this design.

The decoder contains the function of the second item listed above and is compiled to the NGO. The device selected can be a MachXO2™, LatticeXP2™, LatticeECP3™, or ECP5™ device.

The phase of the output clock can be adjusted for the next device to sample the data correctly.

The width of input data can be 10 bits or 12 bits, data_in[11:2] is valid in 10-bit mode.

The drive mode can be configured to the following modes: QXGA, WUXGA, 1080p-HD, 720p-HD, 2x2 addition and 3x3 addition. This will affect the number of blank lines after the falling edge of XVS, the number of total horizontal pixels and total vertical lines (see Table 1.1 and Table 1.2). If the parameter sim is set to ‘1’, the number is decreased for reducing the time of simulation. Users have the option of creating additional modes with modification to the generics and source at the top level which drive the NGO.
### Table 1.1. Drive Modes for the Sony IMX036

<table>
<thead>
<tr>
<th>Drive Mode (2 Bits)</th>
<th>Analog-to-Digital Conversion</th>
<th>Number of Pre-blanking Lines</th>
<th>Frame Rate (Frame/s)</th>
<th>Data Rate (Mpix/s)</th>
<th>Number of Recording Pixels</th>
<th>Number of Output Vertical Lines and Horizontal Pixels</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (QXGA)</td>
<td>10</td>
<td>10</td>
<td>12</td>
<td>60.18</td>
<td>216</td>
<td>2048</td>
</tr>
<tr>
<td></td>
<td>12</td>
<td></td>
<td>12</td>
<td>15.05</td>
<td>54</td>
<td></td>
</tr>
<tr>
<td>1 (1080p-HD)</td>
<td>10</td>
<td>10</td>
<td>12</td>
<td>60.00</td>
<td>148.5</td>
<td>2048</td>
</tr>
<tr>
<td></td>
<td>12</td>
<td></td>
<td>12</td>
<td>30.00</td>
<td>74.25</td>
<td></td>
</tr>
<tr>
<td>2 (2x2 addition)</td>
<td>10</td>
<td>6</td>
<td>12</td>
<td>60.18</td>
<td>54</td>
<td>1024</td>
</tr>
<tr>
<td>3 (3x3 addition)</td>
<td>10</td>
<td>4</td>
<td>12</td>
<td>60.18</td>
<td>24</td>
<td>682</td>
</tr>
</tbody>
</table>

### Table 1.2. Drive Modes for the Sony IMX136

<table>
<thead>
<tr>
<th>Drive Mode (2 Bits)</th>
<th>Analog-to-Digital Conversion</th>
<th>Number of Pre-blanking Lines</th>
<th>Frame Rate (Frame/s)</th>
<th>Data Rate (Mpix/s)</th>
<th>Number of Recording Pixels</th>
<th>Number of Output Vertical Lines and Horizontal Pixels</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 (1080p-HD)</td>
<td>10/12</td>
<td>8</td>
<td>8</td>
<td>30</td>
<td>74.25</td>
<td>1920</td>
</tr>
<tr>
<td></td>
<td>10/12</td>
<td>8</td>
<td>60</td>
<td>148.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>8</td>
<td>120</td>
<td>297</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 (WUXGA 37.125 MHz INCK)</td>
<td>10/12</td>
<td>8</td>
<td>27</td>
<td>37.125</td>
<td>1920</td>
<td>1200</td>
</tr>
<tr>
<td></td>
<td>10/12</td>
<td>8</td>
<td>54</td>
<td>74.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>8</td>
<td>108</td>
<td>148.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6 (WUXGA 27 MHz INCK)</td>
<td>10/12</td>
<td>8</td>
<td>20</td>
<td>27</td>
<td>1920</td>
<td>1200</td>
</tr>
<tr>
<td></td>
<td>10/12</td>
<td>8</td>
<td>40</td>
<td>54</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>8</td>
<td>80</td>
<td>108</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7 (720p-HD)</td>
<td>10/12</td>
<td>8</td>
<td>30</td>
<td>37.125</td>
<td>1280</td>
<td>720</td>
</tr>
<tr>
<td></td>
<td>10/12</td>
<td>8</td>
<td>60</td>
<td>74.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>8</td>
<td>120</td>
<td>148.5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:**
1. This may require the removal of the 24-bit to 12-bit parallel bus mux to meet Place and Route I/O timing. The result is a 24-bit parallel bus output at 148.5 MHz. Other options may be available depending on the application. Please consult Lattice Technical Support before attempting to use this mode.

### Table 1.3. Sensor Bridge Port Descriptions

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>rstn</td>
<td>Reset, active low</td>
<td>Input</td>
</tr>
<tr>
<td>clk</td>
<td>Pixel clock</td>
<td>Input</td>
</tr>
<tr>
<td>data_in</td>
<td>LVDS DDR input data (10 or 12 bits)</td>
<td>Input</td>
</tr>
<tr>
<td>clk_out</td>
<td>Double rate of input clock with phase adjusted</td>
<td>Output</td>
</tr>
<tr>
<td>data_out</td>
<td>LVCMOS SDR output data, synchronous with clk_out</td>
<td>Output</td>
</tr>
<tr>
<td>xhs</td>
<td>Horizontal sync pulse, active low</td>
<td>Output</td>
</tr>
<tr>
<td>xvs</td>
<td>Vertical sync pulse, active low</td>
<td>Output</td>
</tr>
</tbody>
</table>
2. Implementation

Table 2.1. Performance and Resource Utilization

<table>
<thead>
<tr>
<th>Device Family</th>
<th>Speed Grade</th>
<th>Utilization (LUTs)</th>
<th>( f_{\text{MAX}} ) (MHz)</th>
<th>I/Os</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>clk</td>
<td>clkx2</td>
<td></td>
</tr>
<tr>
<td>ECP5(^5)</td>
<td>–8</td>
<td>246 (LSE)</td>
<td>&gt;108</td>
<td>&gt;216</td>
</tr>
<tr>
<td></td>
<td>–8</td>
<td>247 (Syn)</td>
<td>&gt;108</td>
<td>&gt;216</td>
</tr>
<tr>
<td>LatticeECP3(^2)</td>
<td>–6</td>
<td>215</td>
<td>&gt;108</td>
<td>&gt;216</td>
</tr>
<tr>
<td>LatticeXP2(^3)</td>
<td>–5</td>
<td>262</td>
<td>&gt;108</td>
<td>&gt;216</td>
</tr>
<tr>
<td></td>
<td>–5</td>
<td>267 (Syn)</td>
<td>&gt;108</td>
<td>&gt;216</td>
</tr>
<tr>
<td>MachXO2(^4)</td>
<td>–6</td>
<td>268 (LSE)</td>
<td>&gt;108</td>
<td>&gt;180</td>
</tr>
<tr>
<td></td>
<td>–6</td>
<td>268 (Syn)</td>
<td>&gt;108</td>
<td>&gt;180</td>
</tr>
</tbody>
</table>

Notes:
1. \( \text{drive_mode} = 0, \text{ad_conv_width} = 12 \).
2. Performance and utilization characteristics are generated using LAE3-17EA-6MG328E, with Lattice Diamond\(^\circledR\) 3.3 design software. When using this design in a different device, density, speed or grade, performance and utilization may vary.
3. Performance and utilization characteristics are generated using LFXP2-5E-5M132C, with Lattice Diamond 3.3 design software. When using this design in a different device, density, speed or grade, performance and utilization may vary. LSE is not supported in this device.
4. Performance and utilization characteristics are generated using LCMX02-1200HC-6MG132C, with Lattice Diamond 3.3 design software with LSE (Lattice Synthesis Engine). When using this design in a different device, density, speed or grade, performance and utilization may vary. LSE is not supported in this device.
5. Performance and utilization characteristics are generated using LFE5UM-8SF_8MG756C, with the Lattice Diamond 3.3 design software with LSE. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Table 2.2. I/O Timing Analysis of Sub-LVDS Parallel Input Bus\(^1,\;2\)

<table>
<thead>
<tr>
<th></th>
<th>Setup</th>
<th>Hold</th>
<th>Setup</th>
<th>Hold</th>
<th>Setup</th>
<th>Hold</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECP5</td>
<td>Speed Grade 6</td>
<td>0.169</td>
<td>-0.062</td>
<td>Speed Grade 7</td>
<td>0.165</td>
<td>-0.062</td>
</tr>
<tr>
<td>LatticeECP3</td>
<td>Speed Grade 7</td>
<td>0.480/0.359</td>
<td>0.351/0.457</td>
<td>Speed Grade 8</td>
<td>0.379/0.480</td>
<td>0.463/0.379</td>
</tr>
<tr>
<td>LatticeXP2</td>
<td>Speed Grade 5</td>
<td>-0.765</td>
<td>0.992</td>
<td>Speed Grade 6</td>
<td>-0.666</td>
<td>0.836</td>
</tr>
<tr>
<td>MachXO2</td>
<td>Speed Grade 4</td>
<td>0.194/0.375</td>
<td>1.097/0.923</td>
<td>Speed Grade 5</td>
<td>0.167/0.348</td>
<td>0.946/0.772</td>
</tr>
<tr>
<td></td>
<td>Speed Grade 6</td>
<td>0.132/0.313</td>
<td>0.796/0.622</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. Multiple setup/hold numbers indicate that not all I/O timing windows had the same delay across the sub-LVDS parallel bus. The delay primitive can be used to adjust this on a pin-by-pin basis to optimize performance, if needed.
2. I/O numbers to be re-run after pinout is added to constraint file.
### Table 2.3. Pinout

<table>
<thead>
<tr>
<th>Signal</th>
<th>MachXO2 Same Bank 132-Ball csBGA</th>
<th>MachXO2 Multi-Bank 132-Ball csBGA</th>
<th>LatticeXP2 Multi-Bank 132-Ball csBGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>rstn</td>
<td>M1</td>
<td>M1</td>
<td>L2</td>
</tr>
<tr>
<td>clk_p</td>
<td>N6</td>
<td>N6</td>
<td>H1</td>
</tr>
<tr>
<td>clk_n</td>
<td>P6</td>
<td>P6</td>
<td>H3</td>
</tr>
<tr>
<td>Data_in_0_p</td>
<td>M4</td>
<td>B14</td>
<td>F1</td>
</tr>
<tr>
<td>Data_in_0_n</td>
<td>N4</td>
<td>C13</td>
<td>G1</td>
</tr>
<tr>
<td>Data_in_1_p</td>
<td>M7</td>
<td>G12</td>
<td>H2</td>
</tr>
<tr>
<td>Data_in_1_n</td>
<td>N8</td>
<td>G14</td>
<td>G3</td>
</tr>
<tr>
<td>Data_in_2_p</td>
<td>P9</td>
<td>K13</td>
<td>D1</td>
</tr>
<tr>
<td>Data_in_2_n</td>
<td>N9</td>
<td>K14</td>
<td>E1</td>
</tr>
<tr>
<td>Data_in_3_p</td>
<td>M10</td>
<td>M10</td>
<td>F3</td>
</tr>
<tr>
<td>Data_in_3_n</td>
<td>P11</td>
<td>P11</td>
<td>G2</td>
</tr>
<tr>
<td>Data_in_4_p</td>
<td>M11</td>
<td>N13</td>
<td>D2</td>
</tr>
<tr>
<td>Data_in_4_n</td>
<td>P12</td>
<td>N14</td>
<td>E3</td>
</tr>
<tr>
<td>Data_in_5_p</td>
<td>N3</td>
<td>E12</td>
<td>C2</td>
</tr>
<tr>
<td>Data_in_5_n</td>
<td>P4</td>
<td>E14</td>
<td>D3</td>
</tr>
<tr>
<td>Data_in_6_p</td>
<td>N5</td>
<td>N5</td>
<td>B1</td>
</tr>
<tr>
<td>Data_in_6_n</td>
<td>M5</td>
<td>M5</td>
<td>B2</td>
</tr>
<tr>
<td>Data_in_7_p</td>
<td>P8</td>
<td>P8</td>
<td>A1</td>
</tr>
<tr>
<td>Data_in_7_n</td>
<td>M8</td>
<td>M8</td>
<td>B3</td>
</tr>
<tr>
<td>Data_in_8_p</td>
<td>N12</td>
<td>N12</td>
<td>A2</td>
</tr>
<tr>
<td>Data_in_8_n</td>
<td>P13</td>
<td>P13</td>
<td>A3</td>
</tr>
<tr>
<td>Data_in_9_p</td>
<td>P2</td>
<td>P2</td>
<td>C5</td>
</tr>
<tr>
<td>Data_in_9_n</td>
<td>N2</td>
<td>N2</td>
<td>A5</td>
</tr>
<tr>
<td>Data_in_10_p</td>
<td>P3</td>
<td>N3</td>
<td>A6</td>
</tr>
<tr>
<td>Data_in_10_n</td>
<td>M3</td>
<td>P4</td>
<td>A7</td>
</tr>
<tr>
<td>Data_in_11_p</td>
<td>P7</td>
<td>F13</td>
<td>B6</td>
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<tr>
<td>Data_in_11_n</td>
<td>N7</td>
<td>F14</td>
<td>C7</td>
</tr>
<tr>
<td>clk_out</td>
<td>K1</td>
<td>K1</td>
<td>P2</td>
</tr>
<tr>
<td>xvs</td>
<td>A12</td>
<td>A12</td>
<td>P14</td>
</tr>
<tr>
<td>xhs</td>
<td>A13</td>
<td>A13</td>
<td>P13</td>
</tr>
<tr>
<td>data_out_0</td>
<td>J1</td>
<td>J1</td>
<td>N8</td>
</tr>
<tr>
<td>data_out_1</td>
<td>H1</td>
<td>H1</td>
<td>M6</td>
</tr>
<tr>
<td>data_out_2</td>
<td>F1</td>
<td>F1</td>
<td>M5</td>
</tr>
<tr>
<td>data_out_3</td>
<td>E1</td>
<td>E1</td>
<td>M7</td>
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<tr>
<td>data_out_4</td>
<td>C1</td>
<td>C1</td>
<td>N12</td>
</tr>
<tr>
<td>data_out_5</td>
<td>B1</td>
<td>B1</td>
<td>N7</td>
</tr>
<tr>
<td>data_out_6</td>
<td>A2</td>
<td>A2</td>
<td>P12</td>
</tr>
<tr>
<td>data_out_7</td>
<td>A3</td>
<td>A3</td>
<td>P5</td>
</tr>
<tr>
<td>data_out_8</td>
<td>A7</td>
<td>A7</td>
<td>P6</td>
</tr>
<tr>
<td>data_out_9</td>
<td>A9</td>
<td>A9</td>
<td>N2</td>
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<tr>
<td>data_out_10</td>
<td>A10</td>
<td>A10</td>
<td>P7</td>
</tr>
<tr>
<td>data_out_11</td>
<td>A11</td>
<td>A11</td>
<td>N4</td>
</tr>
</tbody>
</table>

**Note:**

1. The MachXO2 same bank pinout is preferred as this pinout has built-in termination resistors for the sub-LVDS Data_in bus.
3. Timing Specifications

The timing of the data_out and xhs is shown in Figure 3.1.

![Figure 3.1. data_out and xhs Timing](image)

The timing of xhs and xvs is shown in Figure 3.2.

![Figure 3.2. XHS and XVS Timing](image)

The pixel number and line number can be configured with the parameters. The simulation is supported by Active-HDL simulators. Set the working directory to the location of the .do script and then execute the .do script. The directory should also be updated on line 14 in the script file sim_active_functional_timing.do.

Figure 3.3 shows the relationship of the signal timing to each other at the horizontal blank and vertical blank.

![Figure 3.3. Simulation Screen Shot Showing Signal Timing](image)

Figure 3.4. Simulation Screen Shot for drive_mode=0 and ad_conv_width=12

The waveform, as shown in Figure 3.4, is for drive_mode = 0 and ad_conv_width=12. The waveform shows that data_out follows data_in after 9 clk_out delay.
Tested Reference Design
The Sony IMX036 bridge has been utilized on the TI/Appropho Network Camera. The design utilizes the MachXO2-1200 device.
Technical Support Assistance
Submit a technical support case through www.latticesemi.com/techsupport.
# Revision History

## Revision 1.8, January 2020

<table>
<thead>
<tr>
<th>Section</th>
<th>Change Summary</th>
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</table>
| All     | • Changed document number from RD1122 to FPGA-RD-02147.  
          | • Updated document template. |
| Disclaimers | Added this section. |

## Revision 1.7, January 2015

<table>
<thead>
<tr>
<th>Section</th>
<th>Change Summary</th>
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</table>
| Implementation | Updated Implementation section. Updated Table 2.1, Performance and Resource Utilization.  
                    | • Added support for Lattice Diamond 3.3 design software.  
                    | • Added support for LSE and Synplify Pro. |

## Revision 1.6, March 2014

<table>
<thead>
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<th>Change Summary</th>
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</table>
| Implementation | • Added support for ECP5 device family.  
                    | • Updated Table 2.1, Performance and Resource Utilization.  
                    | • Updated to support Lattice Diamond 3.1 design software. |

## Revision 1.5, October 2012

<table>
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## Revision 1.4, October 2012

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<th>Change Summary</th>
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<tbody>
<tr>
<td>Implementation</td>
<td>Updated data in the Pinout table, LatticeXP2 Multi-Bank 132-Ball csBGA column.</td>
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</tbody>
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## Revision 1.3, August 2012

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<th>Section</th>
<th>Change Summary</th>
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<tbody>
<tr>
<td>All</td>
<td>Updated to include support of the built in WDR capability of the Sony IMX136/104.</td>
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## Revision 1.2, March 2012

<table>
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<tr>
<th>Section</th>
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| All     | • Document updated with new corporate logo.  
          | • Document updated for IMX136. |

## Revision 1.1, January 2012

<table>
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<td>Document updated for MachXO2 device support.</td>
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## Revision 1.0, May 2011

<table>
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<td>All</td>
<td>Initial release.</td>
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