LPC Bus Controller

April 2011 Reference Design RD1049

Introduction

The Low Pin Count (LPC) interface is a low bandwidth bus with up to 33 MHz performance. It is used to connect peripherals around the CPU and to replace the Industry Standard Architecture (ISA) bus which can only run up to 8 MHz. The primary benefit is that signals can be transmitted across a minimum of seven traces for an LPC bus versus 52 traces for an ISA bus. This relieves the pressure of routing on the often-congested motherboard and at the same time improves the overall system integrity.

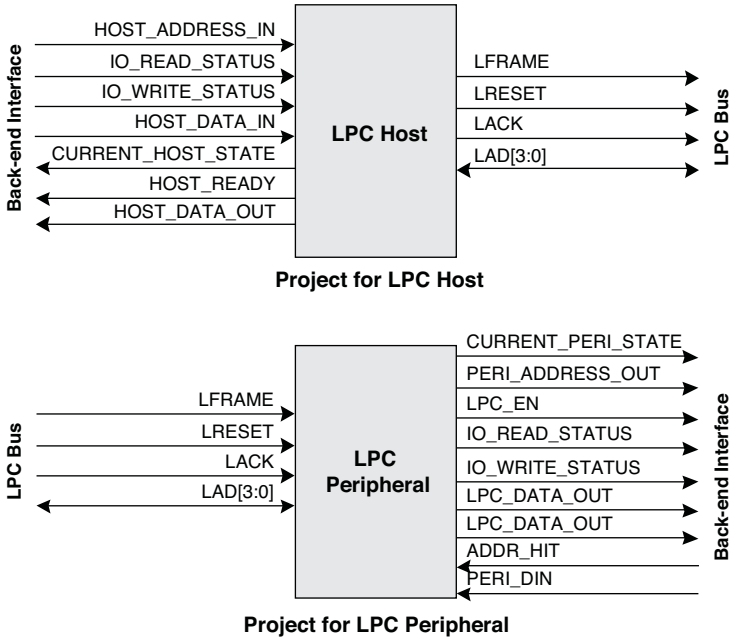
The Lattice LPC Bus Controller Reference Design implements a LPC host and a LPC peripheral that support the seven required LPC control signals. The design is implemented in Verilog as well as VHDL, and Lattice design tools are used for synthesis, place and route, and simulation. The design can be targeted to multiple Lattice device families, and its small size makes it portable across different FPGA/CPLD architectures.

This reference design is based on the Low Pin Count Interface Specification (version 1.1) that is available from the Intel website. It is assumed the reader is familiar with the LPC Specification prior to evaluating and implementing this reference design.

Features and Limitations

This reference design includes two projects, one for the LPC host and the other for the LPC peripheral. This implementation supports I/O read and write. It is not a fully spec-compliant implementation because the LPC host lacks DMA read and DMA write ability. Also, the state machines implemented for I/O read and write do not make full use of the available commands. For example, the read sync does not distinguish between short idle and long idle. There is also no timeout for sync.

Figure 1. Reference Design Block Diagram



Functional Description

LPC Host Module

The LPC host is the initiator of commands. Supported commands are I/O read and write. If the write flag is high, the LPC host transmits the contents of the data and address provided via the back-end interface across the LPC interface to the peripheral. The host then waits for the sync indicator from the peripheral to terminate the write. Read operations behave like the write cycle.

Figure 2. State Machine for the LPC Host Module

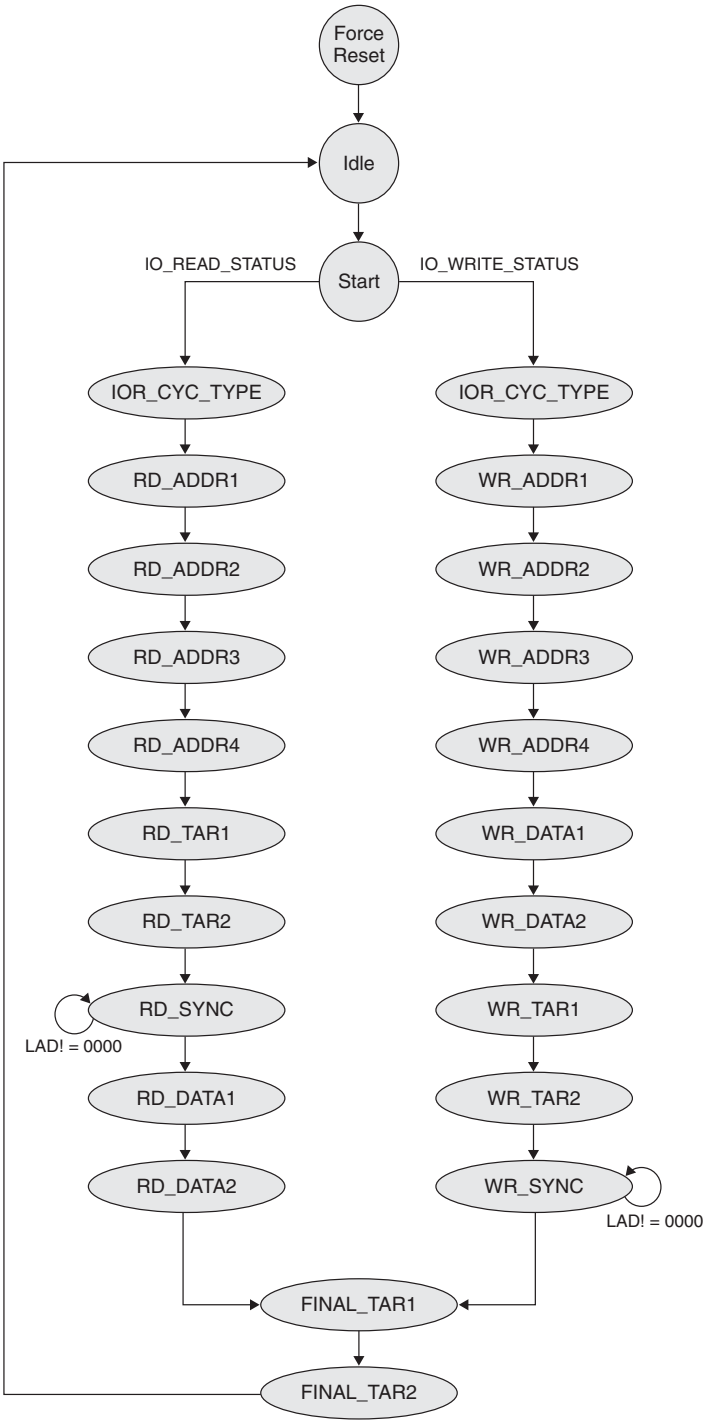


Table 1. LPC Host Signal Descriptions

Name	Direction	Description
LPC Interface		
LAD	Bi-directional	Multiplexed command, Address, and Data
LFRAME	Input	Active-low frame signal
LRESET	Input	Active-low reset signal
LCLK	Input	Clock
Back-end Interface		
Host_Address_In	Input	Address used for reads and writes
IO_Read_Status	Input	Active-high read request
IO_Write_Status	Input	Active-high write request
HOST_DATA_IN	Input	Data sent from host to peripheral
Current_Host_State	Output	Current host state
Host_Ready	Output	Active-high status that host is ready for next operation
HOST_DATA_OUT	Output	Data received from peripheral to host

LPC Peripheral Module

The LPC peripheral is primarily a passive recipient and reactor to commands initiated by the host. Supported commands are I/O read and write.

Figure 3. State Machine for the LPC Peripheral Module

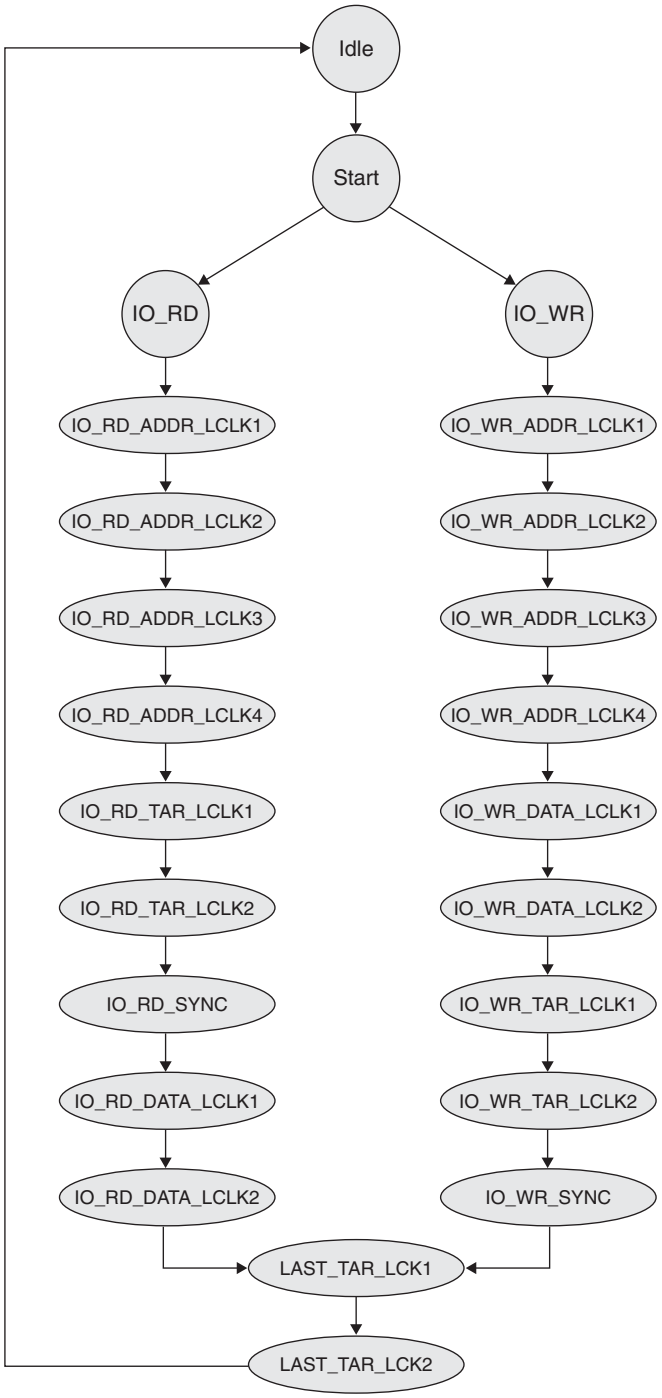


Table 2. LPC Peripheral Signal Descriptions

Name	Direction	Description
LPC Interface		
LAD	Bi-directional	Multiplexed Command, Address and Data
LFRAME	Input	Active-low frame signal
LRESET	Input	Active-low reset signal
LCLK	Input	Clock
Back-end Interface		
Addr_Hit	Input	
Peri_Din	Input	Data sent when host requests a read
IO_Read_Status	Output	Active-high read status
IO_Write_Status	Output	Active-high write status
Current_Peri_State	Output	Current peripheral state
Lpc_En	Output	Active-high status signal indicating the peripheral is ready for next operation.
Lpc_Data_In	Output	Data received by peripheral for writing
Lpc_Data_Out	Output	Data sent to host when a read is requested

The CPU must provide external control, address and data inputs to the LPC host in order to perform a read or write operation to the peripheral. When the host requests a read operation, the peripheral must supply the data to be returned on the Peri_Data_In bus. When the host performs a write operation, the peripheral receives the data from the host on the Peri_Write_Out bus.

Testbench Description
The testbench for this design includes the following modules:

- LPC_Host
- LPC_Peripheral

An I/O write and then an I/O read are performed to demonstrate functionality of the design.

Timing Specifications

The following diagrams show the major milestones in the LPC Reference Design.

Figure 4 shows a CPU writing to a LPC peripheral device. The host is writing address 0xF0F0 with data 0x5A.

Figure 4. LPC Host Write Cycle

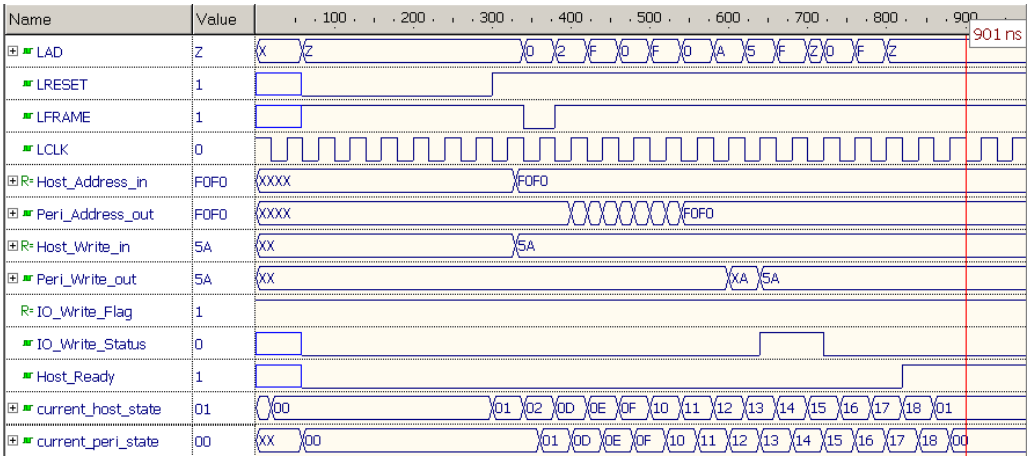
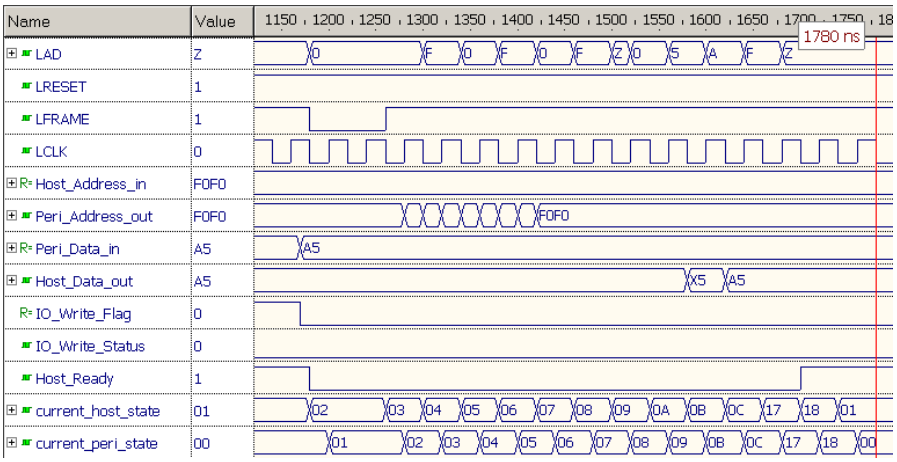


Figure 5 shows a CPU reading from a LPC peripheral device. The host is reading address 0xF0F0 and gets 0xA5. The testbench throws any write data away, and only provides a constant 0xA5 to the host for read cycles. It is the designer's responsibility to connect the back-end to a storage medium.

Figure 5. LPC Host Read Cycle



Implementation

This design is implemented in Verilog and VHDL. When using this design in a different device, density, speed, or grade, performance and utilization may vary. Default settings are used during the fitting of the design.

Table 3. Performance and Resource Utilization

Project	Device Family	Language	Speed Grade	Utilization	f_{MAX} (MHz)	I/Os	Architecture Resources
LPC Peripheral	MachXO2™ [1]	VHDL	-5	73 LUTs	>33	52	N/A
		Verilog	-5	73 LUTs	>33	52	N/A
	MachXO™ [2]	VHDL	-3	73 LUTs	>33	52	N/A
		Verilog	-3	73 LUTs	>33	52	N/A
	LatticeECP3™ [3]	VHDL	-7	97 LUTs	>33	52	N/A
		Verilog	-7	96 LUTs	>33	52	N/A
	LatticeXP2™ [4]	VHDL	-5	95 LUTs	>33	52	N/A
		Verilog	-5	90 LUTs	>33	52	N/A
	ispMACH® 4000ZE[5]	VHDL	-5 (ns)	66 Macrocells	>33	52	N/A
		Verilog	-5 (ns)	66 Macrocells	>33	52	N/A
LPC Host	MachXO2[1]	VHDL	-5	92 LUTs	>33	50	N/A
		Verilog	-5	84 LUTs	>33	50	N/A
	MachXO[2]	VHDL	-3	89 LUTs	>33	50	N/A
		Verilog	-3	84 LUTs	>33	50	N/A
	LatticeECP3™ [3]	VHDL	-7	109 LUTs	>33	52	N/A
		Verilog	-7	107 LUTs	>33	52	N/A
	LatticeXP2[4]	VHDL	-5	119 LUTs	>33	50	N/A
		Verilog	-5	119 LUTs	>33	50	N/A
	ispMACH 4000ZE[5]	VHDL	-5 (ns)	26 Macrocells	>33	50	N/A
		Verilog	-5 (ns)	26 Macrocells	>33	50	N/A

1. Performance and utilization characteristics are generated using LCMXO2-1200HC-5MG132C with Lattice Diamond™ 1.2 design software.
2. Performance and utilization characteristics are generated using LCMXO256C-3T100C with Lattice Diamond 1.2 design software.
3. Performance and utilization characteristics are generated using LFE3-95EA-7FN1156C with Lattice Diamond 1.2 design software.
4. Performance and utilization characteristics are generated using LFXP2-5E-5M132C with Lattice Diamond 1.2 design software.
5. Performance and utilization characteristics are generated using LC4256ZE-5TN100C, with Lattice ispLEVER® Classic 1.4 software software.

References

- Low Pin Count Interface Specification, Intel Corporation

Technical Support Assistance

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Revision History

Date	Version	Change Summary
February 2009	01.0	Initial release.
July 2009	01.1	Added support for ispMACH 4000ZE CPLD family.
		Design separated into LPC host and LPC peripheral projects.
October 2009	01.2	Added VHDL support.
January 2010	01.3	Added support for LatticeXP2 device family.
April 2010	01.4	Updated code and includes standardized VHDL syntax.
November 2010	01.5	Added support for MachXO2 device family and Lattice Diamond design software.
April 2011	01.6	Updated signal names in Reference Design Block Diagram, LPC Host Signal Descriptions table and LPC Peripheral Signal Descriptions table.
		Added support for LatticeECP3 device family and Lattice Diamond 1.2 design software.