

October 2012

Reference Design RD1135

Introduction

The Infrared Data Association (IrDA) maintains an interoperable, low cost, low power, half-duplex serial data interconnection standard that supports a walk-up, point-to-point user model that is adaptable to a wide range of appliances and devices. Infrared (IR) technologies are best suited for short distance, low-to-medium data throughput and wireless communication channels.

This document provides a brief description of an IrDA Fast Transmitter and its implementation.

This reference design is implemented in VHDL. The Lattice iCEcube2[™] Place and Route tool integrated with the Synplify Pro synthesis tool is used for implementation of the design. The design uses an iCE40[™] ultra low density FPGA and can be targeted to other iCE40 family members.

Features

- 4 Mbps baud rate
- · Complete 4PPM packet support Preamble, STA, Data, STO fields
- · Synchronous parallel processor interface
- · 32x32-bit read and write data FIFOs
- · Interrupt on completion of data receipt
- IEEE 802 32-bit Cyclic Redundancy Check (CRC-32) generation and detection

Features not supported:

- Configurable baud rate
- Host UART interface
- Not hardware tested

Functional Description

Figure 1. Block Diagram



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Signal Descriptions

Table 1. Signal Description

Signal	Width	Direction	Description	
cs_n	1	Input	Active low chip select	
oe_n	1	Input	Active low output enable	
we_n	1	Input	Active low write enable	
register_addr	2	Input	Register selection bus to select registers from – control register, status register	
intr	1	Output	IrDA Transmitter interrupt	
data_bus	32	Input	Processor data bus (bi-directional)	
irda_tx	1	Input	IR device data input	
rst_n	1	Input	Asynchronous active low reset – This signal is used to initialize the internal state machine to a known state	
clk_sys	1	Input	System clock	

Module Descriptions

Figure 2. Functional Block Diagram



The IrDA defines a set of specifications, or protocol stack, that provides for the establishment and maintenance of a link so that error-free communication is possible.

The IrDA standards include three mandatory specifications: the Physical Layer, Link Access Protocol (IrLAP), and Link Management Protocol (IrLMP). Beginning with version 1.1 of the IrDA Physical Layer specification, a 4 Mbps data rate is supported.

The Fast Infrared (FIR, 4 Mbps) scheme uses the four pulse position modulation (4PPM) scheme, where one complete symbol is represented by four equal-time slices called "chips". In FIR, every chip has 125 ns duration, and every symbol represents two bits of data. Because there are four unique chip positions within each symbol in 4PPM, four independent symbols exist in which only one chip is a logic '1' while all other chips are a logic '0'. These four unique symbols are the only legal data symbols (DD) allowed in 4PPM. Each DD represents two bits of payload data, or a single data bit pair (DBP), so that a byte of payload data can be represented by four DDs in sequence.

In IrDA FIR mode, a special packet format is used for data transfer. The packet format is divided into four blocks as shown in Table 2.



Table 2. IrDA Data Format

PA	STA	DD along with CRC-32	STO

- PA Preamble consists of exactly 16 repeated transmissions of the following symbols: 1000 0000 1010 1000.
- **STA** Start sequence. Occurs only once and includes the following symbols: 0000 0011 0000 0011 0110 0000 0110 0000. After the preamble, the receiver looks for the STA sequence for synchronization.
- DD Actual data encoded in the 4 PPM scheme along with the CRC-32 bit. After the start sequence, the transmitter transmits the data in encoded form along with CRC-32 to facilitate error detection at the receiver end. CRC(x) = x³² + x²⁶ + x²³ + x²² + x¹⁶ + x¹² + x¹¹ + x¹⁰ + x⁸ + x⁷ + x⁵ + x⁴ + x² + x + 1
- **STO** The stop sequence occurs only once and includes the sequence 0000 0011 0000 0011 0000 0110 0000 0110, indicating the end of a data frame.

Figure 3. FIR (4 PPM) Modulation/Demodulation Schemes



Table 3. Internal Register List

Register	Address	Width (Bits)	Access
Configuration register	0x01	8	R/W
Read (Rx) data FIFO register	0x02	8	R
Status register	0x03	8	R



Table 4. Internal Register Bit Descriptions

Register	Bit Number	Access	Description
	31:13	R/W	Unimplemented
	12	R/W	'1' indicates start of data transaction
	11	R/W	'1' clears the interrupts
Configuration Register (0x01)	10	R/W	'1' enables the interrupts
	9	R/W	'1' clears the read/write FIFO
	8:5	R/W	Unimplemented
	4:0	R/W	Block length of data transaction
Read (Tx) Data FIFO Register (0x02)	31:0	R	Transmitter FIFO read data
	31:4	R	Unimplemented
	3	R	'1' indicates write FIFO Full
Status Register (0x03)	2	R	'1' indicates write FIFO Half Full
	1	R	'1' indicates write FIFO Empty
	0	R	'1' indicates IrDA Transmitter is busy

Operation Sequence

Figure 4. Operational Blocks



- 1. The transmitter is operational when reset = 1° .
- Write the data to be transmitted to the write FIFO by selecting the address = '10'. Sample data : X"0B0B1B0F", X"141BA41E"... (in this case, 16 data words)
- Write to the transmitter configuration register by selecting address = '01'. Making 10th bit = '1' and the 12th bit = '1' implies start of transmission.
 Give the following input: 00000000000000000010100000 to the data bus
- Read the status of the IrDA Transmitter by selecting the address '11' in between data transactions. The irda_busy signal will be high. Content of data bus: "X"00000005"
- 5. Wait until the IrDA Transmitter interrupt goes high, indicating the transmission of data is complete.
- Read the transmitter configuration register by selecting the address = '01' after data transmission. Content of data bus: X"00000410"
- Read the status register of the IrDA Transmitter after data transmission by selecting the address = '11'. The irda_busy signal will go low. Content of data bus: X"00000000".



Timing Diagram



Figure 5. IrDA Transmitter Write/Read Data/Configuration Register Timing Diagram

Simulation Waveforms

Figure 6. Simulation Waveforms

Signal name	Value	· · · · 400 · · · · 800 · · · · 1200 · · · · 1600 · · · · 2000 · · · · 2400 · · · 2800 ·	· · · · · · · · · · · · · · · · · · ·
<pre># rst_n_tb</pre>	1		2 928 797 977 ps
<pre>w cs_n_tb</pre>	0		
⊯ oe_n_tb	1		
# we_n_tb	1		
🖽 🖛 register_addr_tb	3		3
# intr_tb	0		
🖽 🕶 data_bus_tb	77777777		22222222
🕀 🕊 data_bus_i	00001410	(00001410
# ird_nx_tb	1	ער אין	
# data_bus_en_i	0		
# div_clk_i	U		
🕀 🖛 word	0000		0000
w count_16	F		F
w count_4	3		3
Cursor 1		2 928 79	77 977 ps

Implementation

This design is implemented in VHDL. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Table 5. Performance and Resource Utilization

Family	Language	Utilization (LUTs)	f _{MAX} (MHz)	I/Os	Architectural Resources
iCE40 ¹	VHDL	793	79	40	N/A

1. Performance and resource utilization characteristics are generated using iCE-40LP1K-CM121 with iCEcube2 design software.

References

• iCE40 Family Handbook



Technical Support Assistance

Hotline: 1-800-LATTICE (North America) +1-503-268-8001 (Outside North America) e-mail: techsupport@latticesemi.com

Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
October 2012	01.0	Initial release.