

Introduction

The MIL-STD-1553 is a low-speed serial bus used in avionics systems. This reference design implements Manchester II encoding and decoding required by the 1553 along with synchronization pattern insertion and identification, data serialization and de-serialization and parity checking and insertion functions.

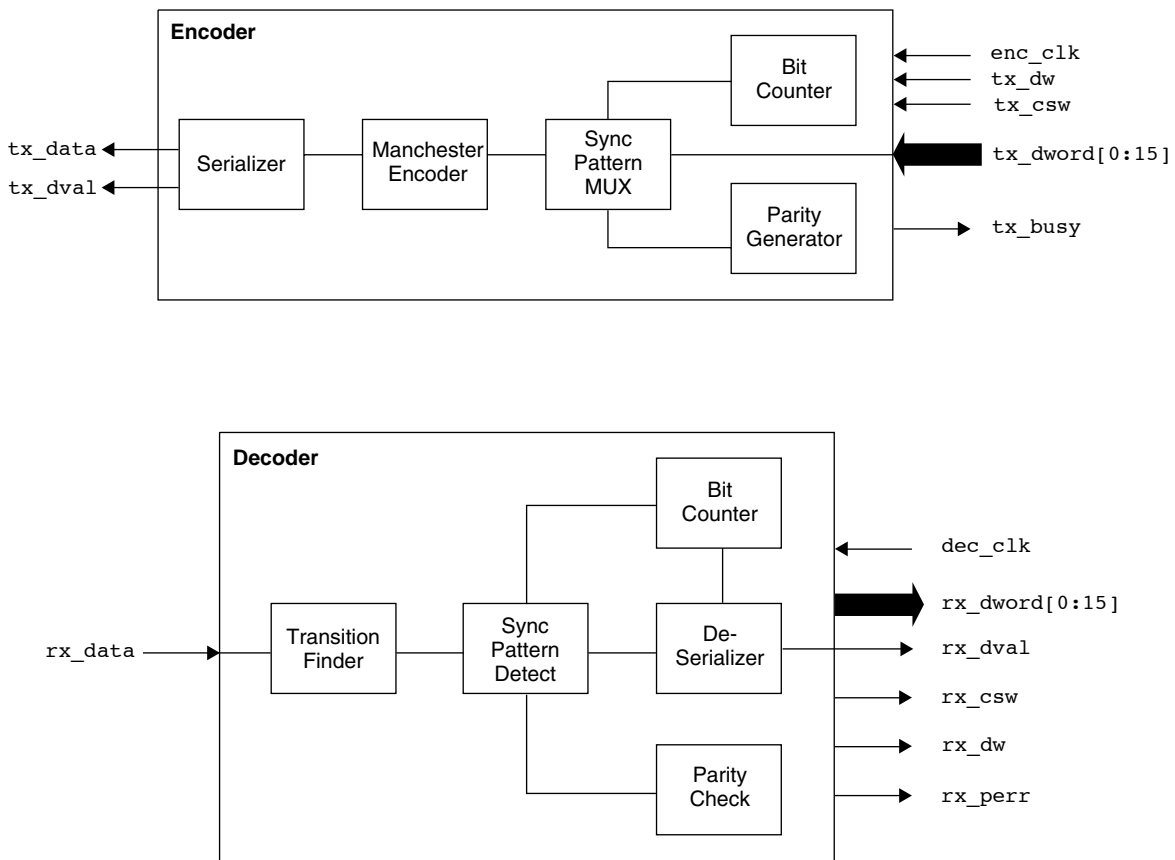
Features

- MIL-STD-1553 Compatible
- 1 Mbps Data Rate
- Sync Pattern Identification and Insertion
- Manchester II Encoding/Decoding
- Parity Checking and Insertion
- Serialization and De-serialization

Functional Description

The following figure shows a block diagram of the different functions implemented in this 1553 Encoder/Decoder along with the input/output signals.

Figure 1. 1553 Encoder/Decoder Block Diagram



Encoder Operation

The encoder requires a single clock with a frequency (2 MHz) of twice the desired data rate (1 Mbps) for `enc_clk`. The encoder cycle begins with either `tx_csw` or `tx_dw` pulse along with the command-status or data word to be transmitted. Then the encoder asserts `tx_busy` until it transmits this word serially through all the encoder functions and then de-asserts `tx_busy` to accept the next word.

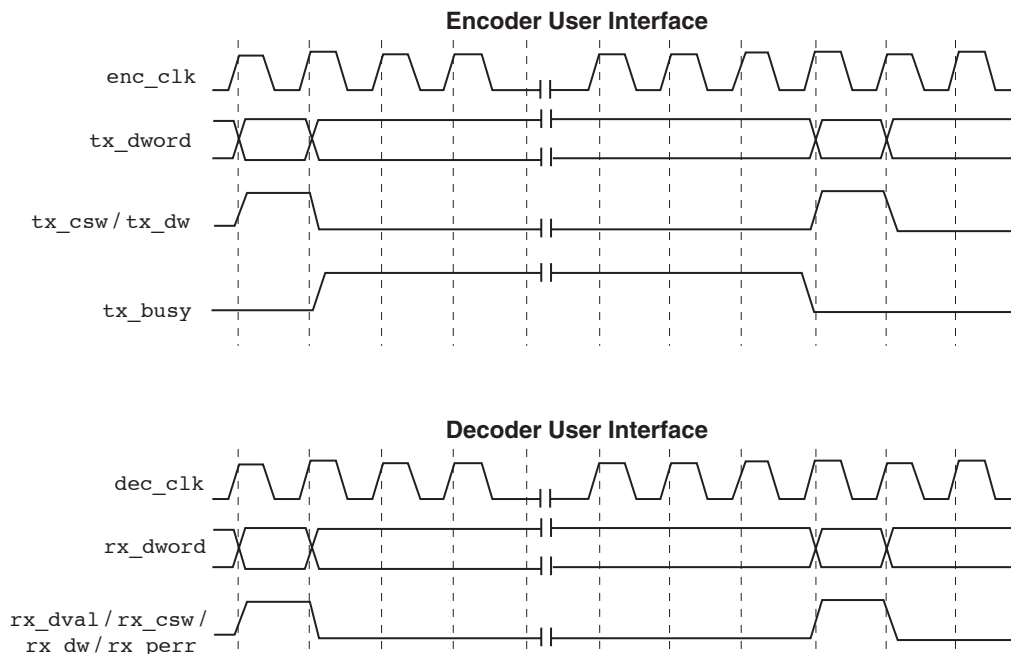
Decoder Operation

The decoder requires a single clock with a frequency (8 MHz) of 8 times the desired data rate (1 Mbps) for `dec_clk`. The decoder is free running and continuously hunting for the synchronization pattern on the serial input. When a valid synchronization pattern is detected, it identifies the boundary of the word and determines it as either a command-status word or a data word. Then the serial bits are passed through shift registers, and a parallel word is presented to the user interface along with the type of word and when it is valid. Also, the word is checked for parity errors.

Pin Descriptions

Port Name	Active State	I/O	Signal Description
Decoder			
<code>dec_clk</code>	—	In	Decoder clock of 8 MHz
<code>rst_n</code>	Low	In	Asynchronous reset
<code>rx_data</code>	—	In	Serial data Input
<code>rx_dword[0:15]</code>	—	Out	Received output data word to user
<code>rx_dval</code>	High	Out	Data valid indication for <code>rx_dword</code>
<code>rx_csw</code>	High	Out	Indicates <code>rx_dword</code> has command or status word
<code>rx_dw</code>	High	Out	Indicates <code>rx_dword</code> has data word
<code>rx_perr</code>	High	Out	Indicates parity error in <code>rx_dword</code>
Encoder			
<code>enc_clk</code>	—	In	Encoder clock of 2 MHz
<code>rst_n</code>	Low	In	Asynchronous reset
<code>tx_dword[0:15]</code>	—	In	Data word from user for transmission
<code>tx_csw</code>	High	In	Indicates <code>tx_dword</code> has command or status word
<code>tx_dw</code>	High	In	Indicates <code>tx_dword</code> has data word
<code>tx_data</code>	—	Out	Serial data output
<code>tx_dval</code>	High	Out	Data valid indication for <code>tx_data</code>
<code>tx_busy</code>	High	Out	Indicates Encoder is not ready to accept the next word

Timing Diagrams



Implementation Results

The design software used for this implementation is Lattice ispLEVER[®] version 4.2 and the Synplcity Synplify synthesis tool. The device utilization and performance summary for LatticeEC[™] and LatticeXP[™] devices (-4 speed grade) is shown below.

Device	Size	Reported Frequency
Decoder		
LFEC20E-4	53 SLICES	8 MHz
LFXP10E-4	53 SLICES	8 MHz
Encoder		
LFEC20E-4	39 SLICES	2 MHz
LFXP10E-4	33 SLICES	2 MHz

File List

The files provided in this LatticeEC reference design package are:

1. /1553_enc_dec/docs/1553_enc_dec.doc	Design document
2. /1553_enc_dec/docs/readme.txt	Read me file
3. /1553_enc_dec/source/decoder_1553.v	Decoder source verilog file
4. /1553_enc_dec/source/encoder_1553.v	Encoder source verilog file
5. /1553_enc_dec/par/EC/decoder_1553.prf	Decoder Constraint file for place and route
6. /1553_enc_dec/par/EC/encoder_1553.prf	Encoder Constraint file for place and route
7. /1553_enc_dec/par/EC/decoder_1553.syn	Decoder Project file for place and route
8. /1553_enc_dec/par/EC/encoder_1553.syn	Encoder Project file for place and route
9. /1553_enc_dec/simulation/EC/scripts/runsim_1553.do	Scripts for RTL simulation
10. /1553_enc_dec/synthesis/EC/synplify/decoder_1553.prj	Decoder Project file for synthesis using Synplify
11. /1553_enc_dec/synthesis/EC/synplify/encoder_1553.prj	Encoder Project file for synthesis using Synplify
12. /1553_enc_dec/synthesis/EC/synplify/decoder_1553.sdc	Decoder Constraint file for synthesis using Synplify
13. /1553_enc_dec/synthesis/EC/synplify/encoder_1553.sdc	Encoder Constraint file for synthesis using Synplify
14. /1553_enc_dec/testbench/test_1553.v	Testbench for simulation

The files provided in this LatticeXP reference design package are:

1. /1553_enc_dec/docs/1553_enc_dec.doc	Design document
2. /1553_enc_dec/docs/readme.txt	Read me file
3. /1553_enc_dec/source/decoder_1553.v	Decoder source verilog file
4. /1553_enc_dec/source/encoder_1553.v	Encoder source verilog file
5. /1553_enc_dec/par/xp/decoder_1553.prj	Decoder Constraint file for place and route
6. /1553_enc_dec/par/xp/encoder_1553.prj	Encoder Constraint file for place and route
7. /1553_enc_dec/par/xp/decoder_1553.syn	Decoder Project file for place and route
8. /1553_enc_dec/par/xp/encoder_1553.syn	Encoder Project file for place and route
9. /1553_enc_dec/simulation/xp/scripts/runsim_1553.do	Scripts for RTL simulation
10. /1553_enc_dec/synthesis/xp/synplify/decoder_1553.prj	Decoder Project file for synthesis using Synplify
11. /1553_enc_dec/synthesis/xp/synplify/encoder_1553.prj	Encoder Project file for synthesis using Synplify
12. /1553_enc_dec/synthesis/xp/synplify/decoder_1553.sdc	Decoder Constraint file for synthesis using Synplify
13. /1553_enc_dec/synthesis/xp/synplify/encoder_1553.sdc	Encoder Constraint file for synthesis using Synplify
14. /1553_enc_dec/testbench/test_1553.v	Testbench for simulation

Technical Support Assistance

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