Color Space Converter

March 2009 Reference Design RD1047

Introduction

Color Space Converters (CSC) are used in video and image display systems including televisions, computer monitors, color printers, video telephony and surveillance systems. CSCs are also used in many video/image compression and processing applications, and in the implementation of NTSC/PAL/SECAM television standards, JPEG and MPEG systems.

A CSC converts signals from one color space to another color space. Color space conversion is often required to ensure compatibility with display devices or to make the image data amenable for compression or transmission.

The CSC Reference Design is widely parameterizable and can support any custom color space conversion requirement. Furthermore, several commonly used color space conversion methods are provided as ready-to-use configurations.

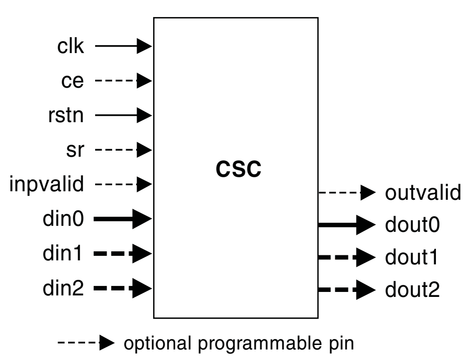
Features

- Input data width of 8, 10, 12, and 16 bits
- Signed or unsigned input data
- Supports standard configurations as well as custom configurations
- Parameterized coefficients precision from 9 to 18 bits
- Full precision as well as limited precision output
- Programmable precision and rounding options for the output
- Option for sequential or parallel architecture for area or throughput optimization
- Configurable DSP block based or look-up-table (LUT) based multiplier implementations
- Registered input option available for input set up time improvement.

Block Diagram

The top-level interface diagram for the CSC Reference Design is given in Figure 1.

Figure 1. Top-Level Interface Diagram for the CSC Reference Design



Functional Description

Color Spaces

A color space is a three dimensional representation of the color and intensity of an image's pixel. An example of a color space is a RGB color space where each pixel's color is represented by the constituent red, green and blue components. This color space is a natural choice for computer displays where the CRT uses these colors to display a multi-colored pixel. However, a RGB color space may not be the ideal one for image processing or efficient image transmission or human interpretation of color information. A color space that represents a color pixel using the characteristics of hue, saturation and brightness is more akin to the way humans interpret color information. HIS and HSV are examples of such color spaces.

It is known that human vision is more sensitive to brightness than color. In an image, green color carries more of the brightness information than the red and blue components. Therefore some of the information from the red and blue color components can be reduced in order to compress the signal for more efficient processing. It is useful to deploy a color space representing brightness (luminance) and color components (chrominance) for processing applications. Common examples of such color spaces are YUV, YIQ and YCbCr, which are part of many video standards.

The following are some commonly used color spaces:

- **RGB:** Red, Green, Blue. This color space is used in computer displays.
- **YIQ,YUV,YCbCr:** Luminance, Chrominance. These color spaces are used in television systems. YIQ is used in NTSC systems, YUV is used in PAL systems and YCbCr is used in digital television systems.
- **CMY(K):** Cyan, Magenta, Yellow, (Black). This color space is used in printing applications. The fourth component, black, is used to improve both the density range and color range. This removes the need to generate a good black color from CMY components.

Color Space Conversion

Color space conversion is required when transferring data between devices that use different color space models. For example, RGB to YCbCr color space conversion is required when displaying a computer image on a television. Similarly YCbCr to RGB color space conversion is required when displaying television movies on the computer monitor. As a color can be represented completely using three dimensions, a color space is a three dimensional space. Color space conversion is a one-to-one mapping from one color space to another color space.

R'G'B' to Y'CbCr color space conversion is given by the following equations. The prime notations are used to denote gamma corrected values.

$$Y' = 0.257 * R' + 0.504 * G' + 0.098 * B' + 16$$
$$Cb = -0.148 * R' - 0.291 * G' + 0.439 * B' + 128$$
$$Cr = 0.439 * R' - 0.368 * G' - 0.071 * B' + 128$$

Y'CbCr to computer R'G'B' conversion is given by the following equations.

$$R' = 1.164 * Y' + 0.0 * Cb + 1.596 * Cr - 222.912$$
$$G' = 1.164 * Y' - 0.392 * Cb - 0.813 * Cr + 135.616$$
$$B' = 1.164 * Y' + 2.017 * Cb + 0.0 * Cr - 276.8$$

Example applications that use CSC for R'G'B' to Y'CbCr Conversion and Y'CbCr to R'G'B' conversion are shown in the following figures.

Figure 2. JPEG Encoding Application

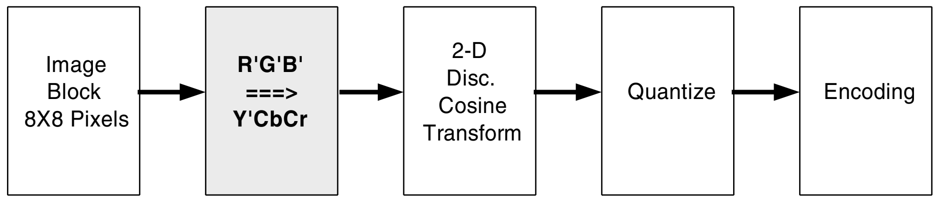
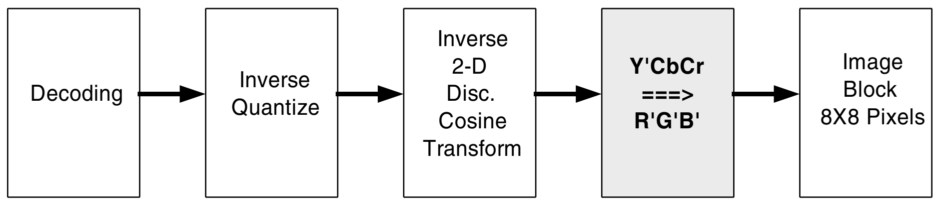


Figure 3. JPEG Decoding Application



CSC Implementation

The color space converter is implemented using multipliers and adders operating on input pixel data and a set of coefficients defined for that conversion. The general color space conversion equations can be expressed by the following matrix multiplication.

$$\begin{bmatrix} dout0 \\ dout1 \\ dout2 \end{bmatrix} = \begin{bmatrix} cMH & cMI & cMJ & cMK \\ cNH & cNI & cNJ & cNK \\ cPH & cPI & cPJ & cPK \end{bmatrix} = \begin{bmatrix} din0 \\ din1 \\ din2 \\ 1 \end{bmatrix}$$

The pixel values of the input color space, din0, din1 and din2 are read through the input ports. The constants denoted by cMH,cMI, ..., cPK, are the coefficients used for the color space conversion. These coefficients are either provided by the user or automatically determined by the reference design GUI for standard conversions. The values of the pixel components in the converted color space are available through the output ports: dout0, dout1 and dout2.

The CSC Reference Design offers a choice of two different architectures: parallel and sequential. In the parallel architecture, all three color plane data are applied at the same time. The output data for all the color planes are also available at the same time after a latency of few clock cycles. In the sequential architecture, the input data for the three color planes is applied in sequence, one after the other, using the same input port din0. The output data for the color planes is given out sequentially using the same output port dout0 after a latency of few clock cycles.

Parameter Descriptions

Table 1 describes the user-configurable parameters entered directly by the user through the IPexpress GUI for the CSC Reference Design. The GUI tabs for default configuration are shown in Figures 4 and 5.

Figure 4. Inputs/Coefficients GUI Tab for CSC Reference Design

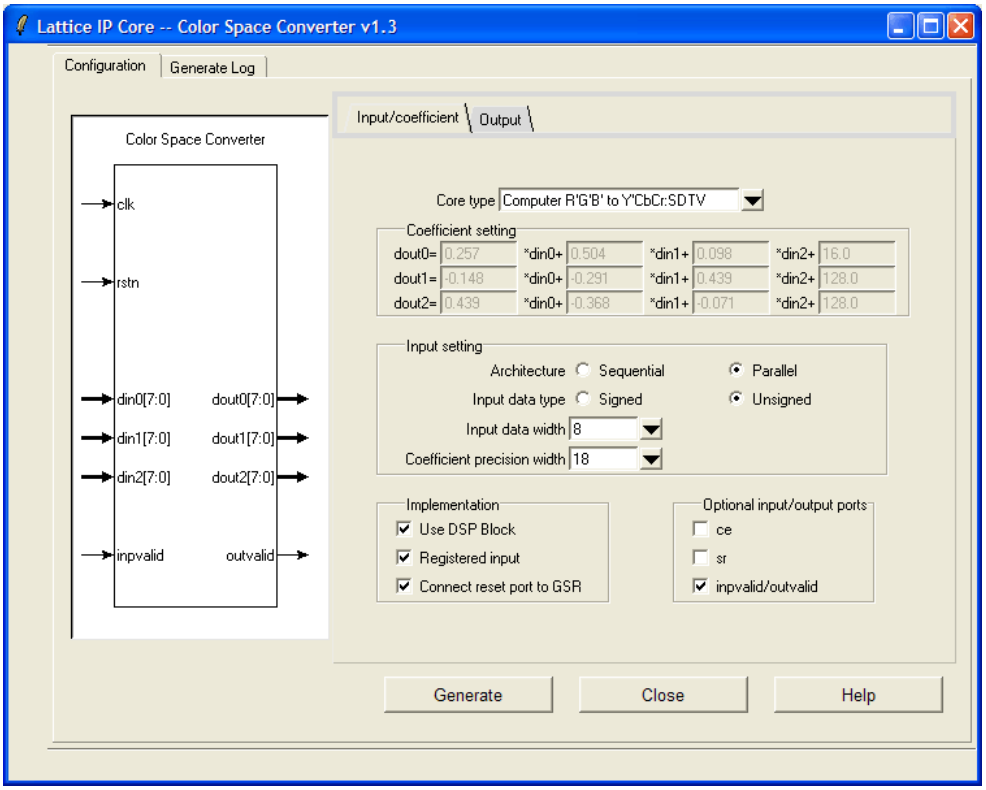


Figure 5. Output GUI Tab for CSC Reference Design

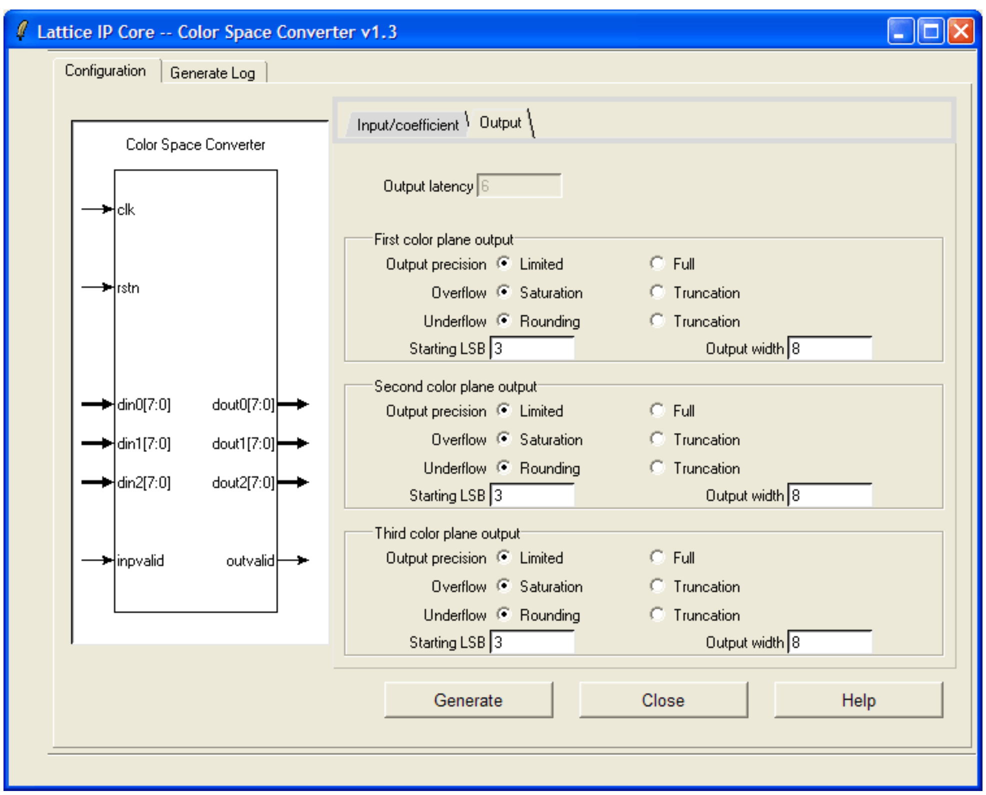


Table 1. User-Configurable Parameters

Name	Description	Range	Default
Core Type			
Core type	Selects between custom and pre-defined standard configurations.	{Custom, Computer R2G2B2 to Y2CbCr:SDTV, Computer R2G2B2 to Y2CbCr:HDTV, Studio R2G2B2 to Y2CbCr:SDTV, Studio R2G2B2 to Y2CbCr:HDTV, Y2CbCr:SDTV to Computer R2G2B2, Y2CbCr:HDTV to Computer R2G2B2, Y2CbCr:SDTV to Studio R2G2B2, Y2CbCr:HDTV to Studio R2G2B2, Y2UV to Computer R2G2B2, Computer R2G2B2 to Y2UV, Y2IQ to Computer R2G2B2, Computer R2G2B2 to Y2IQ, Y2IQ to Y2UV}	Computer R_G_B__to Y_CbCr:SDTV
Architecture			
Architecture	Selects between parallel and sequential implementation architectures.	{Sequential, Parallel}	Sequential
Input Data Width			
Input data width	The bit width for the input color planes.	{8, 10, 12, 16}	8
Input Data Type			
Input data type	Signed or unsigned input data type	{Signed, Unsigned}	Unsigned
Registered Input			
Registered input	The inputs are registered, if this option is selected. The core inputs' set-up times will improve by registering the inputs. This option is useful when the input data is provided on the device pins.	{Yes, No}	Yes
Coefficient Precision Width			
Coefficient precision width	Number of bits used to convert floating point coefficients into fixed point.	9-18	18
Color Plane Output Options			
Output precision	Selects between full precision and limited precision for the output data.	{Full, Limited}	Full
Output width	Output width. This selection is available for limited precision outputs.	5-35	Not Applicable
Overflow	This parameter is available when some MSBs have to be removed from the result for the limited precision output. If the overflow option is "Truncation", the excess MSBs are removed and the remaining LSBs are not changed. If saturation option is selected, the output is saturated based on the removed MSBs.	{Saturation, Truncation}	Truncation

Table 1. User-Configurable Parameters (Continued)

Name	Description	Range	Default
Underflow	This parameter is available when some LSBs have to be removed from the result for the limited precision output. If the underflow option is "Truncation", the excess LSBs are removed and the remaining output is not affected by the removed LSBs. If rounding option is selected, the output is rounded based on the removed LSBs.	{Rounding, Truncation}	Truncation
Starting LSB	This parameter defines the starting Least Significant Bit of the full precision output that becomes LSB of the limited precision output. This parameter gets enabled only when Output precision is selected as Limited.	0-30	3
Optional Input Ports			
ce	Input port ce is added to the core when checked.	Yes or No	No
sr	Input port sr is added to the core when checked.	Yes or No	No
inpvalid/outvalid	If architecture is selected as Sequential, then this is always checked. If architecture is selected as Parallel, then this is optional. If checked this option will add inpvalid and outvalid ports to the core.	Yes or No	No
Output Latency			
Output latency	This provides the output latency for the selected core configuration.	4-9	6
Connect Reset Port to GSR			
Connect reset port to GSR	If this option is checked, the GSR is instantiated and used to route the CSC's rstn input. Using GSR improves the utilization and performance of the CSC Reference Design. However, if GSR is used an active input in rstn will reset most of the FPGA components as well. This option must be checked to enable the hardware evaluation capability for this reference design.	Yes or No	Yes

Configuring the CSC

Standard and Custom Core Types

Table 2 lists the standard configurations available in the CSC Reference Design GUI and their coefficient values.

Table 2. Coefficients for Standard Configurations

Core Type		*din0	*din1	*din2	+
Computer R_G_B__to Y_CbCr:SDTV	dout0	0.257	0.504	0.098	16.0
	dout1	-0.148	-0.291	0.439	128.0
	dout2	0.439	-0.368	-0.071	128.0
Computer R_G_B__to Y_CbCr:HDTV	dout0	0.183	0.614	0.062	16.0
	dout1	-0.101	-0.338	0.439	128.0
	dout2	0.439	-0.399	-0.04	128.0
Studio R_G_B__to Y_CbCr:SDTV	dout0	0.299	0.587	0.114	0.0
	dout1	-0.172	-0.339	0.511	128.0
	dout2	0.511	-0.428	-0.083	128.0
Studio R_G_B__to Y_CbCr:HDTV	dout0	0.213	0.715	0.072	0.0
	dout1	-0.117	-0.394	0.511	128.0
	dout2	0.511	-0.464	-0.047	128.0

Table 2. Coefficients for Standard Configurations (Continued)

Core Type		*din0	*din1	*din2	+
Y_CbCr:SDTV to Computer R_G_B_	dout0	1.164	0.0	1.596	-222.912
	dout1	1.164	-0.391	-0.813	135.488
	dout2	1.164	2.018	0.0	-276.928
Y_CbCr:HDTV to Computer R_G_B_	dout0	1.164	0.0	1.793	-248.128
	dout1	1.164	-0.213	-0.534	76.992
	dout2	1.164	2.115	0.0	-289.344
Y_CbCr:SDTV to Studio R_G_B_	dout0	1.0	0.0	1.371	-175.488
	dout1	1.0	-0.336	-0.698	132.352
	dout2	1.0	1.732	0.0	-221.696
Y_CbCr:HDTV to Studio R_G_B_	dout0	1.0	0.0	1.54	-197.12
	dout1	1.0	-0.183	-0.459	82.176
	dout2	1.0	1.816	0.0	-232.448
Y_UV to Computer R_G_B_	dout0	1.0	0.0	1.14	0.0
	dout1	1.0	-0.395	-0.581	0.0
	dout2	1.0	-2.032	0.0	0.0
Computer R_G_B__to Y_UV	dout0	0.299	0.587	0.114	0.0
	dout1	-0.147	-0.289	0.436	0.0
	dout2	0.615	-0.515	-0.1	0.0
Y_IQ to Computer R_G_B__	dout0	1.0	0.956	0.621	0.0
	dout1	1.0	-0.272	-0.647	0.0
	dout2	1.0	-1.107	1.704	0.0
Computer R_G_B__to Y_IQ	dout0	0.299	0.587	0.114	0.0
	dout1	0.596	-0.275	-0.321	0.0
	dout2	0.212	-0.523	0.311	0.0
Y_IQ to Y_UV	dout0	1.0	0.0	0.0	0.0
	dout1	0.0	-0.544639	0.838671	0.0
	dout2	0.0	0.838671	0.544639	0.0

When a Core type is selected as Custom, the user must manually enter the coefficient values in the GUI.

Full Precision Outputs

The full precision output width is given by the following sum.

Full Precision Width = din_width + coeff_width + 1 + addbitval

Where din_width is input data width, coeff_width is coefficient precision width and addbitval = 1 when the Use DSP Block option is unchecked, the Input Data Type is unsigned, and addbit = 0.

The full precision output is a scaled-up version of the actual output value by a factor of 2^x. The value of x is equal to the maximum integer that satisfies the following equations:

$coeffi*2^x$ ($[-2^{coeff\_widht-1}, 2^{coeff\_width-1}-1]$ for all multiplicative coefficients and
$x \leq coeff\_width + din\_width - y$

where y = ciel($\log_2$ (additive_coefficient_value)) and coeffi is the i^{th} multiplicative coefficient.

Therefore, the true output value is obtained by dividing the full precision output by 2^x.

Limited Precision Outputs

The limited precision output option can be used to limit the width of the outputs to any desired size. The CSC Reference Design GUI provides the option to choose the output width and starting LSB number. If the starting LSB is given as start_lsb, then the output is tapped as full_precision_output[output_width+start_lsb-1:start_lsb]. Limited precision output results in the removal of some LSBs and MSBs from the full precision output.

The underflow options, “truncation” and “rounding” are available when one or more LSBs are removed from the full precision output. If the truncation option is selected, the removed LSBs are simply discarded and the used output bits are not affected by the discarded LSBs. If the rounding option is selected, a ‘1’ is added to the output for positive values, if the most significant discarded bit is a 1.

The overflow options, “truncation” and “saturation” are available when one or more MSBs are removed from the full precision output. If truncation option is selected, the removed MSBs are simply discarded and the used output bits are not affected by the discarded MSBs. If the saturation option is selected, the output is made equal to the maximum positive or negative value based on the sign bit, if the discarded MSBs have any significant bits.

Signal Descriptions

The I/O port definitions are given in Table 3.

Table 3. Interface Signal Description

Port	Bits	I/O	Description
All Configurations			
clk	1	I	Reference clock for input and output data.
rstn	1	I	System wide asynchronous active-low reset signal.
din0	8 - 16	I	Input data. When the sequential architecture is selected then this port is used to give input data for all the three input color planes in sequence. When the parallel architecture is selected then this port is used to give input data for the first input color plane.
dout0	5 - 35	O	Output data. When the sequential architecture is selected then this port is used to give output data for all the three output color planes in sequence. When the parallel architecture is selected then this port is used to give output data for the first output color plane.
When Parallel Architecture is Selected			
din1	8 - 16	I	Input data for second color plane.
din2	8 - 16	I	Input data for third color plane.
dout1	5 - 35	O	Output data for second color plane.
dout2	5 - 35	O	Output data for third color plane. This port is always enabled when the parallel architecture is selected.
Valid Signals			
inpvalid	1	I	Input data valid. Indicates valid data is present on din0 (also on din1 and din2 when present). When the parallel architecture is selected then this port is optional. In this case this port is not used directly in the core but used to generate the outvalid signal after initial core latency. When the sequential architecture is selected then this port is always enabled. In this case this port is used inside the core and also used to generate the outvalid signal after initial core latency. Also when the sequential architecture is selected then this signal should be asserted high for one clock cycle when valid data for the first input color plane is present on the din0 port. For the second and third input color planes data this signal should be low. Input data for all the three input color planes should be applied at successive clock cycles without any gap.
outvalid	1	O	Output data valid. Indicates valid data is present on dout0 (also on dout1 and dout2 when present). When the parallel architecture is selected then this port is optional. When the sequential architecture is selected then this port is always enabled and asserted high when the valid data is present for the first output color plane. During output data of second and third color planes outvalid is low.

Table 3. Interface Signal Description (Continued)

Port	Bits	I/O	Description
Optional I/Os			
ce	1	1	Clock Enable. While this is de-asserted, the core will ignore all other synchronous inputs and maintain its current state.
sr	1	1	Synchronous Reset. Asserted for at least one clock period duration in order to re-initialize the core. After synchronous reset, all internal registers are cleared and outvalid goes low.

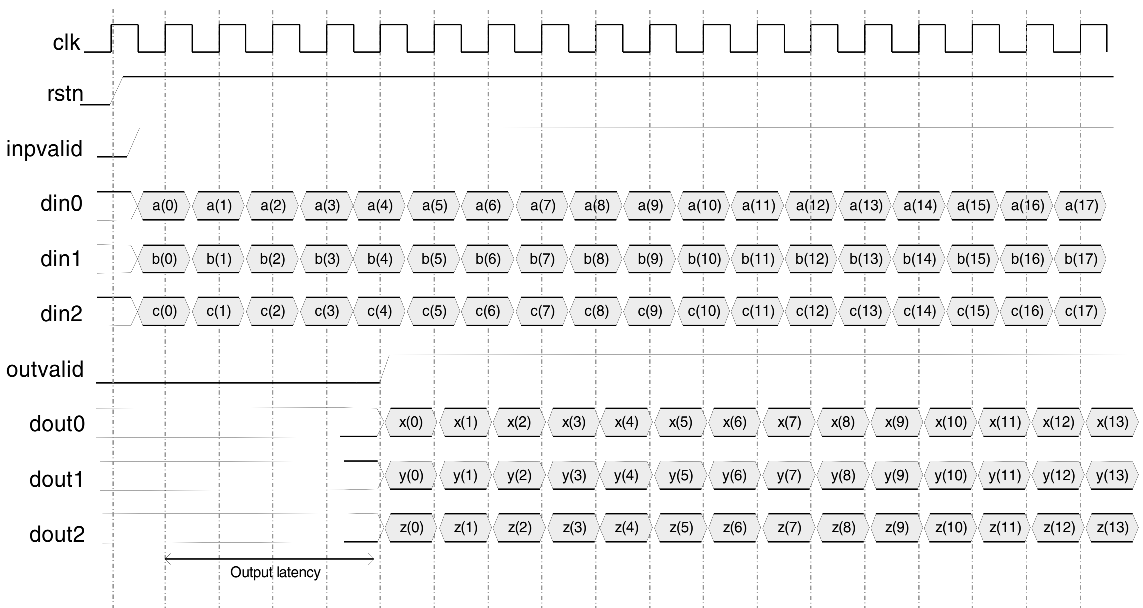
Timing Specifications

Parallel Architecture Timing

Figure 6 shows the input and output signal timing diagram for the parallel architecture. The input data for all the three color planes are applied simultaneously on the input ports din0, din1 and din2.

The signal inpvalid is asserted to indicate a valid input data present on the input ports. After a latency of few cycles, the output data for all the three color planes appear on the output ports dout0, dout1 and dout2. The signal outvalid is asserted to indicate a valid output data present on the output ports.

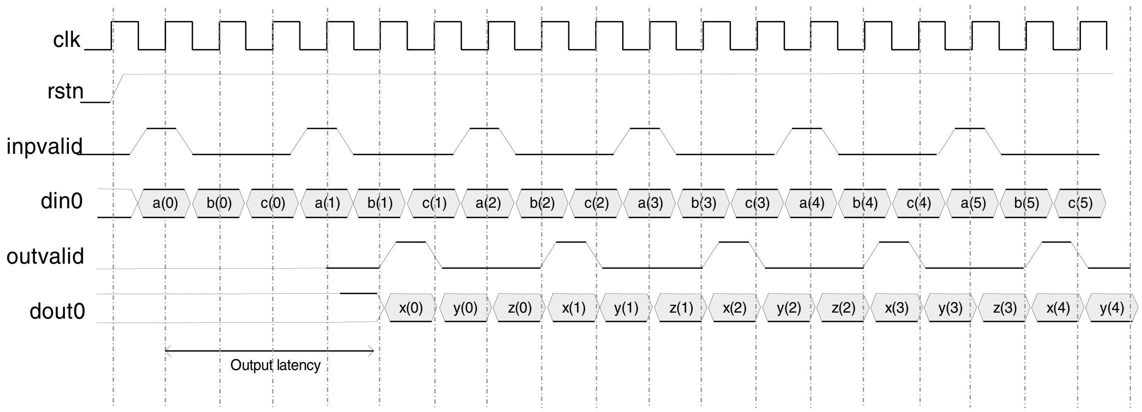
Figure 6. Parallel Architecture



Sequential Architecture Timing

Figure 7 shows the input and output signal timing for the sequential architecture. The input data for all the three color planes is applied in sequence on the input port din0. The signal inpvalid is asserted to indicate the first color plane data on din0. In the following two cycles, the second and third color plane data are applied on din0. After a latency of few cycles the output data for the first color plane appears on the output port dout0. The signal outvalid is asserted to indicate the first color plane data on dout0. In the following two cycles, the second and third color plane data appear on dout0.

Figure 7. Sequential Architecture



IPexpress™ User-Configurable Reference Design

The CSC is an IPexpress user-configurable reference design that allows designers to configure the core and generate netlists as well as simulation files for use in designs.

To download a full version of this reference design, please go to the Lattice IP Server tab in the ispLEVER® IPexpress GUI window. All ispLeverCORE™ cores available for download are visible on this tab.

Example Configurations

Configuration		Config1	Config2	Config3	Config4	Config5
Core Type		Computer R'G'B' to Y'CbCr:SDTV	Computer R'G'B' to Y'CbCr:SDTV	Y'CbCr:HDTV to Computer R'G'B'	Computer R'G'B' to Y'CbCr:SDTV	Y'IQ to Y'UV
Input Setting	Architecture	Parallel	Sequential	Parallel	Parallel	Parallel
	Input data type	Unsigned	Unsigned	Signed	Unsigned	Signed
	Input data width	8	8	16	8	16
	Coefficient precision width	18	18	18	12	18
Implementation	Registered input	Yes	Yes	Yes	Yes	Yes
	Connect reset port to GSR	Yes	Yes	Yes	Yes	Yes
Optional Input/Output Ports	ce	No	No	Yes	No	Yes
	sr	No	No	Yes	No	Yes
	Inpvalid/outvalid	Yes	Yes	Yes	Yes	Yes
Output Latency		6	9	6	6	4
First Color Plane Output	Output precision	Limited	Limited	Limited	Limited	Full
	Overflow	Saturation	Saturation	Saturation	Saturation	Saturation
	Underflow	Rounding	Rounding	Truncation	Rounding	Rounding
	Starting LSB	3	5	2	5	
	Output width	8	8	32	8	35
Second Color Plane Output	Output precision	Limited	Limited	Limited	Limited	Full
	Overflow	Saturation	Saturation	Truncation	Saturation	Saturation
	Underflow	Rounding	Rounding	Rounding	Rounding	Rounding
	Starting LSB	3		5	4	
	Output width	8		29	8	35

Example Configurations (Continued)

Configuration		Config1	Config2	Config3	Config4	Config5
Third Color Plane Output	Output precision	Limited	Limited	Limited	Limited	Full
	Overflow	Saturation	Saturation	Saturation	Saturation	Saturation
	Underflow	Rounding	Rounding	Rounding	Rounding	Rounding
	Starting LSB	3		3	6	
	Output width	8		31	8	35

Implementation

LatticeEC™ Devices

Table 4. Performance and Resource Utilization[1]

IPexpress User-Configurable Mode	Slices	LUTs	Registers	IOB	sysDSP™ Blocks	f_{MAX} (MHz)
Config1	549	1097	611	52	—	123
Config2	473	946	265	20	—	97
Config3	739	1477	714	146	—	99
Config4	384	760	471	52	—	130
Config5	658	1315	475	159	—	86

1. Performance and utilization characteristics are generated using LFEC20E-5F672, with Lattice ispLEVER 7.1 software. When using this reference design in a different density, speed, or grade within the LatticeEC family, performance and utilization may vary

LatticeECP™ Devices

Table 5. Performance and Resource Utilization[1]

IPexpress User-Configurable Mode	Slices	LUTs	Registers	IOB	sysDSP Blocks	f_{MAX} (MHz)
Config1	79	158	156	52	3	114
Config2	53	58	106	20	1	126
Config3	170	334	299	146	3	113
Config4	384	760	471	52	0	137
Config5	27	54	52	159	3	188

1. Performance and utilization characteristics are generated using LFECP20E-5F672, with Lattice ispLEVER 7.1 software. When using this reference design in a different density, speed, or grade within the LatticeECP family, performance and utilization may vary.

LatticeECP2/M Devices

Table 6. Performance and Resource Utilization[1]

IPexpress User-Configurable Mode	Slices	LUTs	Registers	IOB	sysDSP Blocks	f_{MAX} (MHz)
Config1	78	155	153	52	3	199
Config2	53	57	105	20	1	203
Config3	172	338	299	146	3	198
Config4	407	806	471	52	0	230
Config5	27	54	52	159	3	291

1. Performance and utilization characteristics are generated using LFE2-50E-7F672C, with Lattice ispLEVER 7.1 software. When using this reference design in a different density, speed, or grade within the LatticeECP2 family, performance and utilization may vary.

LatticeXP™ Devices

Table 7. Performance and Resource Utilization [1]

IPexpress User-Configurable Mode	Slices	LUTs	Registers	IOB	sysDSP Blocks	f_{MAX} (MHz)
Config1	549	1097	611	52	—	112
Config2	473	946	265	20	—	90
Config3	739	1477	714	146	—	88
Config4	384	760	471	52	—	121
Config5	658	1315	475	159	—	75

1. Performance and utilization characteristics are generated using LFXP20E-5F484C, with Lattice ispLEVER 7.1 software. When using this reference design in a different density, speed, or grade within the LatticeXP family, performance and utilization may vary.

LatticeXP2™ Devices

Table 8. Performance and Resource Utilization [1]

IPexpress User-Configurable Mode	Slices	LUTs	Registers	IOB	sysDSP Blocks	f_{MAX} (MHz)
Config1	78	155	153	52	3	183
Config2	53	57	105	20	1	193
Config3	172	338	299	146	3	188
Config4	407	806	471	52	0	217
Config5	27	54	52	159	3	240

1. Performance and utilization characteristics are generated using LFXP2-17E-7F484C, with Lattice ispLEVER 7.1 software. When using this reference design in a different density, speed, or grade within the LatticeXP2 family, performance and utilization may vary.

LatticeSC/M Devices

Table 9. Performance and Resource Utilization [1]

IPexpress User-Configurable Mode	Slices	LUTs	Registers	IOB	sysDSP Blocks	f_{MAX} (MHz)
Config1	815	1624	623	52	—	211
Config2	454	905	265	20	—	185
Config3	904	1797	718	146	—	238
Config4	486	967	485	52	—	273
Config5	803	1593	484	159	—	188

1. Performance and utilization characteristics are generated using LFSC3GA25E-7F900C, with Lattice ispLEVER 7.1 software. When using this reference design in a different density, speed, or grade within the LatticeSC family, performance and utilization may vary.

You can use the IPexpress software tool to help generate new configurations of this reference design. IPexpress is the Lattice IP configuration utility, and is included as a standard feature of the ispLEVER design tools. Details regarding the usage of IPexpress can be found in the IPexpress and ispLEVER help system. For more information on the ispLEVER design tools, visit the Lattice web site at: www.latticesemi.com/software.

References

- Keith Jack, "Video Demystified", fourth edition, Elsevier, London, 2005.

Technical Support Assistance

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Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
March 2009	01.0	Initial release.