MachXO3L/MachXO3LF Product Family Qualification Summary

Lattice Document # MS – 107213 June 2019

Dear Customer,

Enclosed is Lattice Semiconductor's MachXO3L/MachXO3LF Product Family Qualification Report.

This report was created to assist you in the decision making process of selecting and using our products. The information contained in this report represents the entire qualification effort for this device family.

The information is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC and Automotive Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

Your feedback is valuable to Lattice. If you have suggestions to improve this report, or the data included, we encourage you to contact your Lattice representative.

Sincerely,

James M. Orr
Vice President,
Corporate Quality
Lattice Semiconductor Corporation

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1.0 INTRODUCTION

The MachXO3 device family is an Ultra-Low Density family that supports the most advanced programmable bridging and I/O expansion. It has the breakthrough I/O density and the lowest cost per I/O. The device I/O features have the integrated support for latest industry standard I/O.

The MachXO3L/MachXO3LF family of low power, non-volatile PLDs has five devices with densities ranging from 640 to 9400 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I2C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO3L/MachXO3LF devices are designed on a 65nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO3L provides a low cost migration path to MachXO3LF, which utilizes an innovative non-volatile configuration memory (NVCM) technology that is multi-time (Endurance = 9 program/erase cycles) programmable, while the MachXO3LF devices utilize a low-cost, Flash technology (Endurance = 10K) for maximum flexibility.

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2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Lattice Semiconductor's Reliability Monitor Program Procedure (Doc. #70-101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8D process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITs. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Product families are qualified based upon the requirements outlined in Table 2.2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

The MachXO2, MachXO3L and MachXO3LF families are all 65nm technology-based product offerings that leverage the same silicon design blocks, wafer fabrication design rules, bills of materials, and assembly processes & test sites. Therefore, the MachXO3L and MachXO3LF FPGA product family qualifications are based on a combination of device specific qual data and family generic qual data as per the Lattice Semiconductor Qualification Procedure, doc#70-100164. The MachXO3L and MachXO3LF silicon is qualified by similarity from the MachXO2, while the MachXO3L and MachXO3LF package qualification leverages data from both the Cu-wire quals and MachXO3L package specific qual data.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at Product Reliability Monitor Report.

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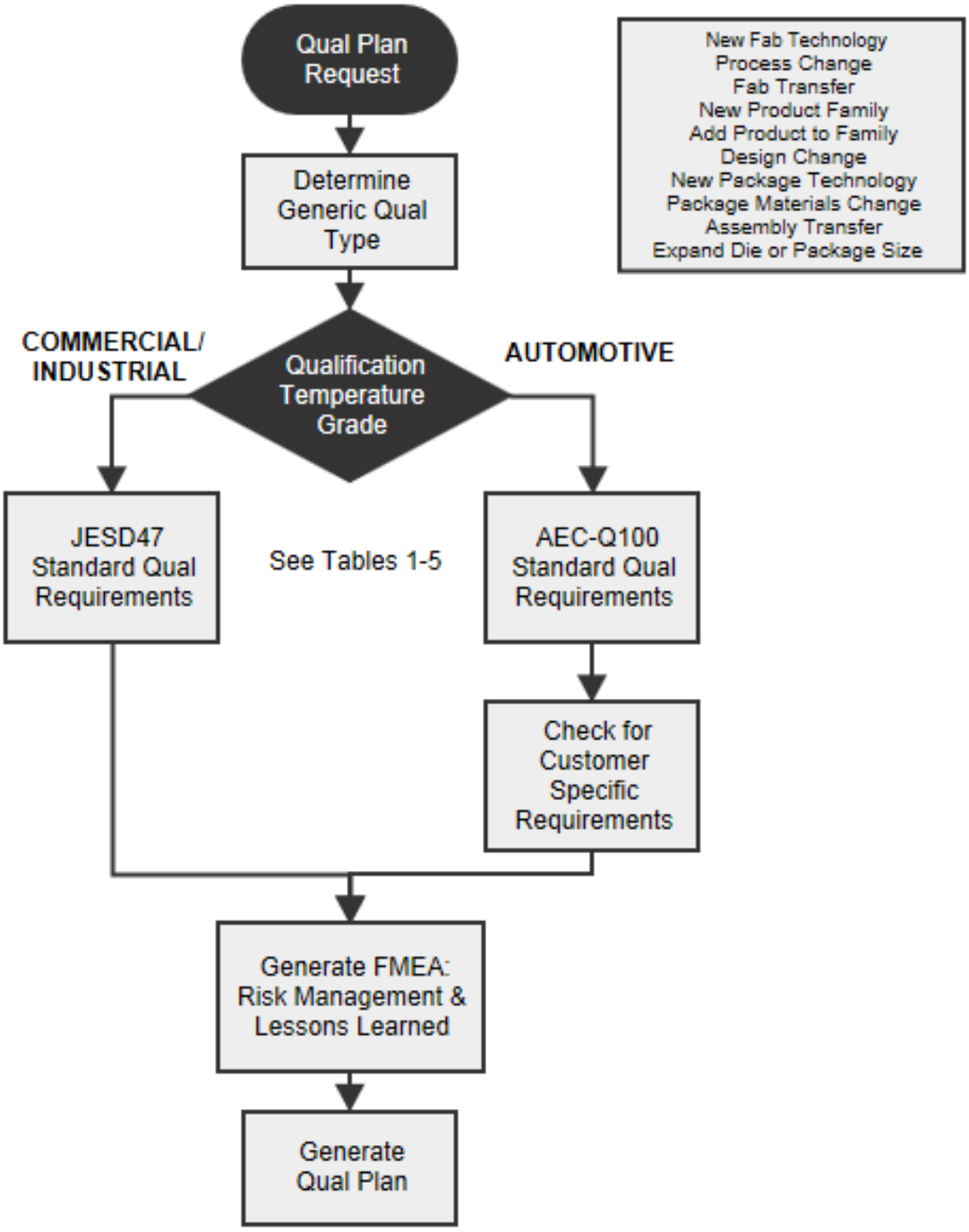
Figure 2.0.1 Lattice Standard Product Qualification Process Flow

This diagram represents the standard qualification flow used by Lattice to qualify new Product Families. The target end market for the Product Family determines which flow options are used. The MachXO3L/MachXO3LF Product Family was qualified using the Commercial / Industrial Qualification Option.



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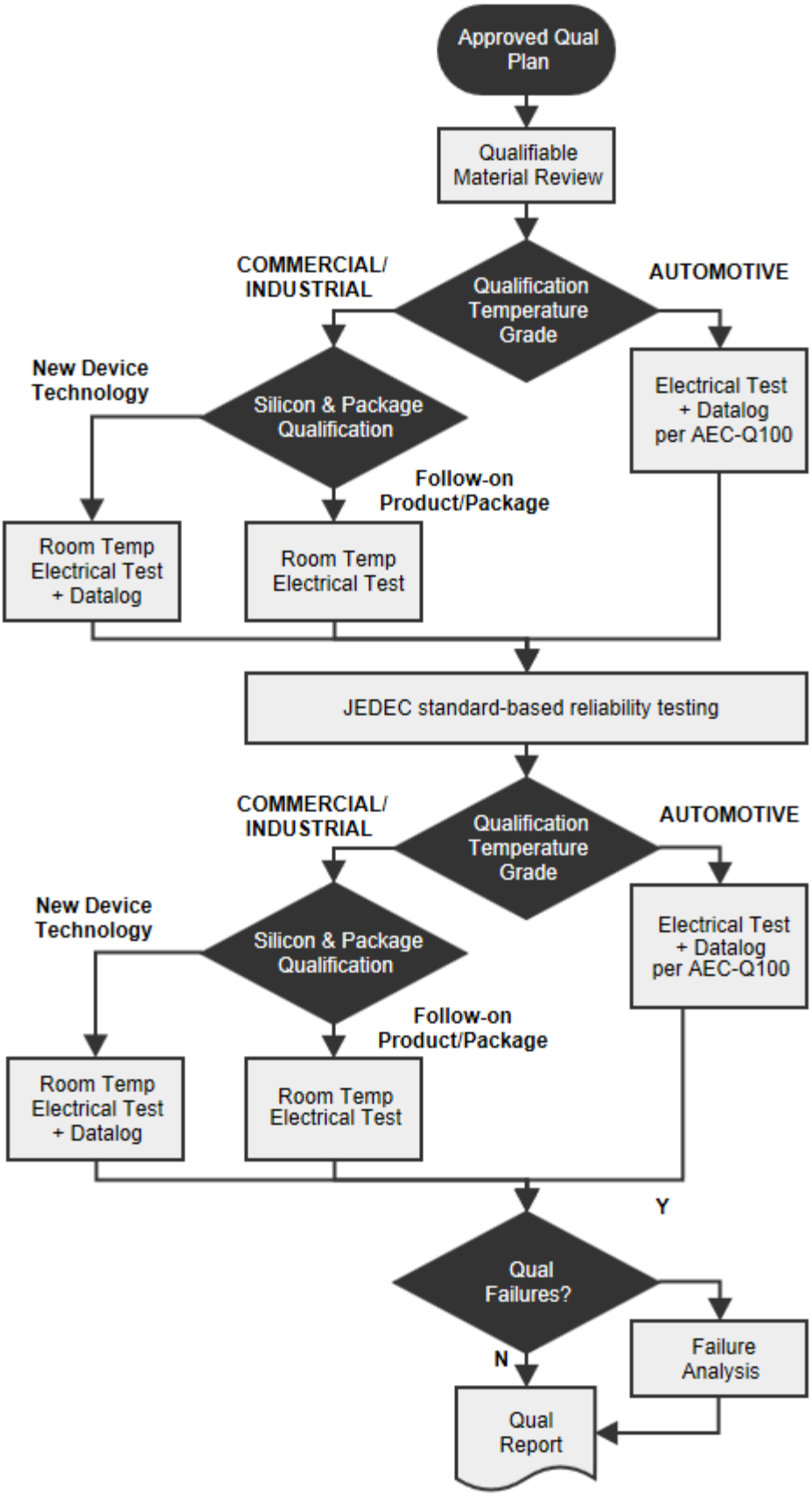

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Table 2.0.2 Standard Qualification Testing

TEST	STANDARD	TEST CONDITIONS
High Temperature Operating Life (HTOL)	JESD22-A108	≥125°C Tj and max operating supplies
Human Body Model ESD (HBM)	JS-001	25°C (Technology/Device dependent Performance Targets)
Charged Device Model ESD (CDM)	JESD22-C101	25°C (Technology/Device dependent Performance Targets)
Latch-Up (LU)	JESD78	Class II, +/-100mA trigger current and 1.5x max operating supplies
Accelerated Soft Error Testing (ASER)	JESD89	25°C, Nominal operating supplies
Surface Mount Pre-conditioning (SMPC)	IPC/JEDEC J-STD-020D JESD-A113	Per appropriate MSL level per J-STD-020
High Temp Storage Life (HTSL)	JESD22-A103	Condition B
Temperature Cycling (TC)	JESD22-A104	Condition B, soak mode 2 (typical)
Temperature Humidity Bias (THB) or Biased Highly Accelerated Stress Test (HAST)	JESD22-A101 JESD22-A110	85°C/85%RH, max operating supplies or 110°C/85%RH, max operating supplies or 130°C/85%RH, max operating supplies
Unbiased Temperature/Humidity (UHAST)	JESD22-A118	110°C/85%RH or 130°C/85%RH

Table 2.0.3 Industry Standard Qualification Testing for WLCSP Packages

STRESS TEST	STANDARD	TEST CONDITIONS
Slow-Temperature Cycling	JEDEC JESD22-A104 IPC-JEDEC9701A	Condition G, soak mode 2 (-40°C to 125°C, 7.5 min soak) 1-2 CPH for 3000 cycles
Bend Qualification	JEDEC JESD22-B113 IPC-JEDEC9702	200,000 bends of test boards at 1 to 3 Hz with maximum cross-head displacement of 4 mm
Drop Qualification Condition B (Handheld apps)	JEDEC JESD22-B111 IPC-JEDEC9703	1500g drops at 0.5 millisecond duration (half-sine pulse)
Drop Qualification Condition H (Shipping)	JEDEC JESD-B104 IPC-JEDEC9703	2900g drops at 0.3 millisecond duration (half-sine pulse)

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3.0 QUALIFICATION DATA MACHXO3L/MACHXO3LF PRODUCT FAMILY

The MachXO3L/MachXO3LF devices are fabricated at Fujitsu on a 65nm non-volatile low power process, then assembled and tested at Advanced Semiconductor Engineering, Malaysia (ASEM), Amkor Technology Philippines (ATP), and Amkor Technology Taiwan (ATT).

Product Family: MachXO3L/MachXO3LF

Package Offered: WLCSP, caBGA and csfBGA

Process Technology Node: 65nm

Table 3.0.1 MachXO3L/MachXO3LF Family Selection Guide

Features		MachXO3L-640/ MachXO3LF-640	MachXO3L-1300/ MachXO3LF-1300	MachXO3L-2100/ MachXO3LF-2100	MachXO3L-4300/ MachXO3LF-4300	MachXO3L-6900/ MachXO3LF-6900	MachXO3L-9400/ MachXO3LF-9400
LUTs		640	1300	2100	4300	6900	9400
Distributed RAM (kbits)		5	10	16	34	54	73
EBR SRAM (kbits)		64	64	74	92	240	432
Number of PLLs		1	1	1	2	2	2
Hardened Functions:	I^2C	2	2	2	2	2	2
	SPI	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1
	Oscillator	1	1	1	1	1	1
MIPI D-PHY Support		Yes	Yes	Yes	Yes	Yes	Yes
Multi Time Programmable NVCM		MachXO3L-640	MachXO3L-1300	MachXO3L-2100	MachXO3L-4300	MachXO3L-6900	MachXO3L-9400
Programmable Flash		MachXO3LF-640	MachXO3LF-1300	MachXO3LF-2100	MachXO3LF-4300	MachXO3LF-6900	MachXO3LF-9400
Packages				**IO**			
36-ball WLCSP[1] (2.5 mm x 2.5 mm, 0.4 mm)			28				
49-ball WLCSP[1] (3.2 mm x 3.2 mm, 0.4 mm)				38			
81-ball WLCSP[1] (3.8 mm x 3.8 mm, 0.4 mm)					63		
121-ball csfBGA[1] (6 mm x 6 mm, 0.5 mm)		100	100	100	100		
256-ball csfBGA[1] (9 mm x 9 mm, 0.5 mm)			206	206	206	206	206
324-ball csfBGA[1] (10 mm x 10 mm, 0.5 mm)				268	268	281	
256-ball caBGA[2] (14 mm x 14 mm, 0.8 mm)			206	206	206	206	206
324-ball caBGA[2] (15 mm x 15 mm, 0.8 mm)				279	279	279	
400-ball caBGA[2] (17 mm x 17 mm, 0.8 mm)					335	335	335
484-ball caBGA[2] (19 mm x 19 mm, 0.8 mm)							384

1. Package is only available for E=1.2 V devices.
2. Package is only available for C=2.5 V/3.3 V devices.

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3.1 MachXO3L/MachXO3LF Product Family Life (HTOL) Data

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JEDEC JESD22-A108D "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

Life Test (HTOL) Conditions:

Devices Stressed: MachXO2

Stress Duration: 168, 500, 1000, 2000 hours

Stress Temperature: $T_{JUNCTION} = \geq 125°C$

Stress Voltage: MachXO2 HTOL Pattern, Vcc=1.26V (ZE/HE), 3.47V (HC), Vccio=3.47V

Stress Method: Lattice Document # 87-101943 and JESD22-A108C/E

Table 3.1.1 MachXO3L/MachXO3LF Product Family Life Results

Product Name	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
LCMXO2-1200ZE	Lot #6	60	0	0	0	N/A	60,000
LCMXO2-1200HC	Lot #6	60	0	0	0	N/A	60,000
LCMXO2-1200ZE	Lot #6	48	0	0	0	N/A	48,000
LCMXO2-1200HC	Lot #6	50	0	0	0	N/A	50,000
LCMXO2-7000ZE	Lot #1	40*	0	0	0	0	80,000
LCMXO2-7000HC	Lot #1	40*	0	0	0	0	80,000
LCMXO2-7000ZE	Lot #1	50	0	0	0	0	100,000
LCMXO2-7000HC	Lot #1	48	0	0	0	0	96,000
LCMXO2-7000ZE	Lot #2	40*	0	0	0	0	80,000
LCMXO2-7000HC	Lot #2	40*	0	0	0	0	80,000
LCMXO2-7000ZE	Lot #2	50	0	0	0	0	100,000
LCMXO2-7000HC	Lot #2	48	0	0	0	0	96,000
LCMXO3-9400HC	Lot#3	80	0	0	0	N/A	80,000
LCMXO3-9400HE	Lot#1	93	0	0	0	N/A	93,000
LCMXO3-9400HE	Lot#2	96	0	0	0	N/A	96,000
LCMXO3-9400HE	Lot#3	118	0	0	0	N/A	118,000

* These units did not receive Flash cell pre-condition cycling prior to stress.

Cumulative Life Testing Device Hours = 1,317,000
Cumulative Result = 0 failures at 1000 & 2000 hours
Long Term Failure Rate = 9 FIT
FIT Assumptions: CL=60%, AE=0.7eV, Tjref=55C

ELFR (168Hrs) Cumulative Result/Sample Size = 0 / 963
HTOL (1000 Hrs) Cumulative Result/Sample Size = 0 / 961
HTOL (2000 Hrs) Cumulative Result/Sample Size = 0 / 356

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3.2 MachXO3L/MachXO3LF Product Family High Temperature Retention (HTRX) Data

High Temperature Data Retention (HTRX)

The High Temperature Data Retention test measures the cell reliability of the non-volatile memories for Flash based, packaged devices. The High Temperature Data Retention test is specifically designed to accelerate charge gain on to or charge loss off of the memory cells in the array. Since the charge on these cells determines the actual pattern and function of the device, this test is a measure of the reliability of the device in retaining programmed information. In High Temperature Data Retention, the memory cell reliability is determined by monitoring the cell margin after biased static operation at 150°C ambient. Memory cells in the arrays are life tested with half the samples programmed with a checkerboard pattern and half with checkerboard-not patterns. Prior to data retention testing all memory cells are pre-conditioned with 10,000 program/erase cycles.

Data Retention (HTRX) Conditions:

Devices Stressed: MachXO2

Stress Duration: 168, 500, 1000 hours.

Temperature: 150°C ambient

Stress Voltage: V_{CC}=1.26V/ V_{CCIO}=3.47V

Method: Lattice Document # 87-101925 and JESD22-A103C / JESD22-A117A/C

Table 3.2.1 MachXO3LF** High Temperature Retention Results

Product Name	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	1500 Hrs Result	Cumulative Hours
LCMXO2-1200ZE	Lot #3	76	0	0	0	NA	76,000
LCMXO2-1200ZE	Lot #4	26*	0	0	0	NA	26,000
LCMXO2-1200ZE	Lot #4	26*	0	0	0	NA	26,000
LCMXO2-1200ZE	Lot #4	26*	0	0	0	NA	26,000
LCMXO2-1200ZE	Lot #5	80	0	0	0	NA	80,000
LCMXO2-1200ZE	Lot #6	80	0	0	0	0	120,000
LCMXO2-1200ZE	Lot #6	80	0	0	0	0	120,000
LCMXO2-7000ZE	Lot #1	80	0	0	0	0	120,000
LCMXO2-7000ZE	Lot #2	80	0	0	0	0	120,000
LCMXO3-9400HC	Lot #1	80	0	0	0	NA	80,000 ***
LCMXO3-9400HC	Lot #2	80	0	0	0	NA	80,000 ***
LCMXO3-9400HC	Lot #3	80	0	0	0	NA	80,000 ***

* Qual lot #4 LCMXO2-1200ZE includes tunnel oxide (TOX) process splits: nominal, thick and thin TOX respectively.
** The MachXO3LF and MachXO2 families uses the exact same 65nm Flash cell on all product densities and speed-power versions. The results above include six separate foundry lots of the same flash cell. A detailed 65nm Flash Data Retention report is available upon request. Lattice Semiconductor Corp. document #25-106925.
*** No program/erase pre-conditioning

Cumulative HTRX Failure Rate = 0 / 794
Cumulative HTRX Device Hours = 954,000

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3.3 MachXO3LF Product Family Flash Endurance Cycling Data

Flash Extended Endurance testing measures the durability of the device through programming and erase cycles. Endurance testing consists of repeatedly programming and erasing all cells in the array at 25°C ambient to simulate programming cycles the user would perform. This test evaluates the integrity of the thin tunnel oxide through which current passes to program the floating gate in each cell of the array.

MachXO3LF Flash Extended Endurance Test Conditions:

Devices Stressed: MachXO2

Stress Duration: 1K, 10K, 20K, 50K, 100K Cycles

Stress Temperature: 25°C ambient

Stress Voltage MachXO2: V_{CC}=1.26V / V_{CCIO}=3.47V

Stress Method: Lattice Document # 70-104633 and JESD22-A117A

Table 3.3.1 MachXO3LF* Flash Extended Endurance Results

Product Name	Lot #	Qty	Cycling Temp	1K CYC	10K CYC	20K CYC	50K CYC	100K CYC
LCMXO2-1200ZE	Lot #6	54	25°C	0	0	0	0	0
LCMXO2-7000ZE	Lot #1	60	25°C	0	0	0	0	0
LCMXO2-7000ZE	Lot #2	60	25°C	0	0	0	0	0
LCMXO2-640ZE	Lot #1	30	25°C	0	0	0	0	0
LCMXO2-2000ZE	Lot #1	30	25°C	0	0	0	0	0
LCMXO2-4000ZE	Lot #1	30	25°C	0	0	0	0	0

* The MachXO3LF and MachXO2 families uses the exact same 65nm Flash cell on all product densities and speed-power versions. The results above includes six separate foundry lots of the same flash cell.

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3.4 MachXO3L/MachXO3LF Product Family – ESD and Latch UP Data

Electrostatic Discharge-Human Body Model:

MachXO3L/MachXO3LF product family was tested per the JESD22-A114 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure and Lattice Procedure # 70-100844. All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.1 MachXO3L/MachXO3LF ESD-HBM Data

Product	36 WLCSP (2.5x2.5mm , 0.4mm pitch)	49 WLCSP (3.2x3.2mm, 0.4mm pitch)	81 WLCSP (3.8x3.8mm, 0.4mm pitch)	121 csfBGA (6x6mm, 0.5mm pitch)	256 csfBGA (9x9mm, 0.5mm pitch)	324 csfBGA (10x10mm, 0.5mm pitch)	256 caBGA (14x14mm, 0.8mm pitch)	324 caBGA (15x15mm, 0.8mm pitch)	400 caBGA (17x17mm, 0.8mm pitch)	484 caBGA (19x19mm, 0.8mm pitch)
LCMXO3L/XO3LF-640				QBS HBM>2KV Class 2						
LCMXO3L/XO3LF-1300*	QBS HBM>2KV Class 2			QBS HBM>2KV Class 2	QBS HBM>2KV Class 2		QBS HBM>2KV Class 2			
LCMXO3L/XO3LF-2100		QBS HBM>2KV Class 2		QBS HBM>2KV Class 2	QBS HBM>2KV Class 2	QBS HBM>2KV Class 2	HBM>2KV Class 2	QBS HBM>2KV Class 2		
LCMXO3L/XO3LF-4300			QBS HBM>2KV Class 2	QBS HBM>2KV Class 2	QBS HBM>2KV Class 2	QBS HBM>2KV Class 2	HBM>2KV Class 2	QBS HBM>2KV Class 2	QBS HBM>2KV Class 2	
LCMXO3L/XO3LF-6900					QBS HBM>2KV Class 2	QBS HBM>2KV Class 2	HBM>2KV Class 2	QBS HBM>2KV Class 2	QBS HBM>2KV Class 2	
LCMXO3L/XO3LF-9400					HBM>2KV Class 2		HBM>2KV Class 2		QBS HBM>2KV Class 2	QBS HBM>2KV Class 2

HBM classification for Commercial/Industrial products, per AEI/JESD22-A114 / JS001-2014.
All HBM levels indicated are dual-polarity (±).
HBM worst-case performance is the package with the smallest RLC parasitics. All other packages for a given product are qualified-by-similarity (QBS).
*LCMXO3L/XO3LF-1300 HBM captured on 132csBGA non-production package.

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Electrostatic Discharge-Charged Device Model:

MachXO3L/MachXO3LF product family was tested per the JESD22-C101C, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure and Lattice Procedure # 70-100844. All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.2 MachXO3L/MachXO3LF ESD-CDM Data

Product	36 WLCSP (2.5x2.5mm , 0.4mm pitch)	49 WLCSP (3.2x3.2mm, 0.4mm pitch)	81 WLCSP (3.8x3.8mm, 0.4mm pitch)	121 csfBGA (6x6mm, 0.5mm pitch)	256 csfBGA (9x9mm, 0.5mm pitch)	324 csfBGA (10x10mm, 0.5mm pitch)	256 caBGA (14x14mm, 0.8mm pitch)	324 caBGA (15x15mm, 0.8mm pitch)	400 caBGA (17x17mm, 0.8mm pitch)	484 caBGA (19x19mm, 0.8mm pitch)
LCMXO3L/XO3LF-640				QBS CDM>1KV Class IV						
LCMXO3L/XO3LF-1300*	QBS CDM>1KV Class IV			QBS CDM>1KV Class IV	QBS CDM>1KV Class IV		QBS CDM>1KV Class IV			
LCMXO3L/XO3LF-2100		QBS CDM>1KV Class IV		QBS CDM>1KV Class IV	QBS CDM>1KV Class IV	QBS CDM>1KV Class IV	CDM>1KV Class IV	QBS CDM>1KV Class IV		
LCMXO3L/XO3LF-4300			QBS CDM>800V Class IV	QBS CDM>800V Class IV	QBS CDM>800V Class IV	QBS CDM>800V Class IV	CDM>800V Class IV	QBS CDM>800V Class IV	QBS CDM>800V Class IV	
LCMXO3L/XO3LF-6900					QBS CDM>1KV Class IV	QBS CDM>1KV Class IV	CDM>1KV Class IV	QBS CDM>1KV Class IV	QBS CDM>1KV Class IV	
LCMXO3L/XO3LF-9400					CDM>1KV Class 2		QBS CDM>1KV Class 2		QBS CDM>1KV Class 2	CDM>1KV Class 2

CDM classification for Commercial/Industrial products, per EIA/JESD22-C101 / JS002-2014.
All CDM levels indicated are dual-polarity (±).
CDM worst-case performance is the package with the largest bulk capacitance. All other packages for a given product are qualified-by-similarity (QBS).
*LCMXO3L/XO3LF-1300 CDM captured on 132csBGA non-production package.

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Latch-Up:

MachXO3L/MachXO3LF product family was tested per the JEDEC EIA/JESD78D IC Latch-up Test procedure and Lattice Procedure # 70-101570. All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.3 MachXO3L/MachXO3LF I/O Latch Up >100mA @ HOT (105°C) Data

Product	36 WLCSP (2.5x2.5mm , 0.4mm pitch)	49 WLCSP (3.2x3.2mm, 0.4mm pitch)	81 WLCSP (3.8x3.8mm, 0.4mm pitch)	121 csfBGA (6x6mm, 0.5mm pitch)	256 csfBGA (9x9mm, 0.5mm pitch)	324 csfBGA (10x10mm, 0.5mm pitch)	256 caBGA (14x14mm, 0.8mm pitch)	324 caBGA (15x15mm, 0.8mm pitch)	400 caBGA (17x17mm, 0.8mm pitch)	484 caBGA (19x19mm, 0.8mm pitch)
LCMXO3L/XO3LF-640				QBS > +/-100mA Class II Level A						
LCMXO3L/XO3LF-1300*	QBS > +/-100mA Class II Level A			QBS > +/-100mA Class II Level A	QBS > +/-100mA Class II Level A		QBS > +/-100mA Class II Level A			
LCMXO3L/XO3LF-2100		QBS > +/-100mA Class II Level A		QBS > +/-100mA Class II Level A	QBS > +/-100mA Class II Level A	QBS > +/-100mA Class II Level A	> +/-100mA Class II Level A	QBS > +/-100mA Class II Level A		
LCMXO3L/XO3LF-4300			QBS > +/-100mA Class II Level A	QBS > +/-100mA Class II Level A	QBS > +/-100mA Class II Level A	QBS > +/-100mA Class II Level A	> +/-100mA Class II Level A	QBS > +/-100mA Class II Level A	QBS > +/-100mA Class II Level A	
LCMXO3L/XO3LF-6900					> +/-100mA Class II Level A		> +/-100mA Class II Level A		QBS > +/-100mA Class II Level A	QBS > +/-100mA Class II Level A

I-Test LU classification for Commercial/Industrial products, per JESD78E.
All IO-LU levels indicated are dual-polarity (±).
IO-LU worst-case performance is the package with access to the most IOs. All other packages for a given product are qualified-by-similarity (QBS).
*LCMXO3L/XO3LF-1300 LU captured on 132csBGA non-production package.

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Table 3.4.4 MachXO3L/MachXO3LF Vcc Latch Up >1.5X @ HOT (105°C) Data

Product	36 WLCSP (2.5x2.5mm, 0.4mm pitch)	49 WLCSP (3.2x3.2mm, 0.4mm pitch)	81 WLCSP (3.8x3.8mm, 0.4mm pitch)	121 csfBGA (6x6mm, 0.5mm pitch)	256 csfBGA (9x9mm, 0.5mm pitch)	324 csfBGA (10x10mm, 0.5mm pitch)	256 caBGA (14x14mm, 0.8mm pitch)	324 caBGA (15x15mm, 0.8mm pitch)	400 caBGA (17x17mm, 0.8mm pitch)	484 caBGA (19x19mm, 0.8mm pitch)
LCMXO3L/XO3LF-640				QBS > 1.5x Vcc Class II						
LCMXO3L/XO3LF-1300*	QBS > 1.5x Vcc Class II			QBS > 1.5x Vcc Class II	QBS > 1.5x Vcc Class II		QBS > 1.5x Vcc Class II			
LCMXO3L/XO3LF-2100		QBS > 1.5x Vcc Class II		QBS > 1.5x Vcc Class II	QBS > 1.5x Vcc Class II	QBS > 1.5x Vcc Class II	> 1.5x Vcc Class II	QBS > 1.5x Vcc Class II		
LCMXO3L/XO3LF-4300			QBS > 1.5x Vcc Class II	QBS > 1.5x Vcc Class II	QBS > 1.5x Vcc Class II	QBS > 1.5x Vcc Class II	> 1.5x Vcc Class II	QBS > 1.5x Vcc Class II	QBS > 1.5x Vcc Class II	
LCMXO3L/XO3LF-6900					QBS > 1.5x Vcc Class II	QBS > 1.5x Vcc Class II	> 1.5x Vcc Class II	QBS > 1.5x Vcc Class II	QBS > 1.5x Vcc Class II	
LCMXO3L/XO3LF-9400					> 1.5x Vcc Class II		> 1.5x Vcc Class II			QBS > 1.5x Vcc Class II

Vsupply Over-voltage Test LU classification for Commercial/Industrial products, per JESD78E.
Vcc-LU worst-case performance is the package with access to the most individual power rails. All other packages for a given product are qualified-by-similarity (QBS).
*LCMXO3L/XO3LF-1300 Vcc-LU captured on 132csBGA non-production package.

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4.0 PACKAGE QUALIFICATION DATA FOR MACHXO3L/MACHXO3LF PRODUCT FAMILY

The MachXO3L/MachXO3LF Wafer Level Chip Scale Package (WLCSP) devices are assembled in Amkor Technology Taiwan (ATT); Saw-singulated Chip Array BGA (caBGA) devices are primarily assembled and tested at Amkor Technology Philippines (ATP), with secondary sourcing at Advanced Semiconductor Engineering, Malaysia (ASEM); while the FlipChip Chip Scale Package (fcCSP or csfBGA) devices are bumped at ATT and assembled in ATP. This report details the package qualification results of the various MachXO3L/MachXO3LF product introductions. Package qualification tests include Surface Mount Pre-Conditioning (SMPC), Temperature Cycling (TC), Unbiased HAST (uHAST), Biased HAST (BHAST) and High Temperature Storage (HTSL). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and visual inspection (VI). SMPC is used prior package stresses on all packages except for HTSL, where SMPC is required, only on wirebonded packages (caBGA).

4.1 Family Qualifications

The generation and use of generic data applied across a family of packages emanating from one base assembly process is a Family Qualification, or Qualification-by-Similarity (QBS). For the package stresses BHAST, UHAST and HTSL, these are considered generic for a given Package Technology. TC is considered generic up to an evaluated die size + package size + 10%, for a given Package Technology. Surface Mount Pre-Conditioning (SMPC) is considered generic up to an evaluated Peak Reflow temperature, for a given Package Technology.

The following table demonstrates the package stresses qualification matrix.

Table 4.1.1 WLCSP Package Qualification-By-Similarity (QBS) Matrix at ATT

The LCMXO3L/XO3LF, WLCSP product/package combinations are Qualified-by-Similarity (QBS) using the qualification vehicles below.	Stress Tests	Amkor Technology Taiwan (ATT) T5 and T1		
		36WLCSP (2.5x2.5mm, 0.4mm pitch)	49WLCSP (3.2x3.1mm, 0.4mm pitch)	81WLCSP (3.7x3.8mm, 0.4mm pitch)
LCMXO3L/XO3LF-4300, 81WLCSP (Lead WLCSP qual vehicle)	SMPC			MSL1
	T/C			700 cycles
	UHAST			264 hours
	HTSL			1000 hours
LCMXO3L/XO3LF-2100, 49WLCSP (Package is qualified-by-similarity from the LCMXO3L/XO3LF-4300, 81WLCSP)	SMPC		QBS	
	T/C			
	UHAST			
	HTSL			
LCMXO3L/XO3LF-1300, 36WLCSP (Package is qualified-by-similarity from the LCMXO3L/XO3LF-4300, 81WLCSP)	SMPC	QBS		
	T/C			
	UHAST			
	HTSL			

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Table 4.1.2 Cu-wire, caBGA Package Qualification-By-Similarity (QBS) Matrix at ASEM

The LCMXO3L/XO3LF, caBGA product/package combinations are Qualified-by-Similarity (QBS) using the qualification vehicles below.	Stress Tests	Advanced Semiconductor Engineering, Malaysia (ASEM)					
		132csBGA (8x8mm, 0.5mm pitch)	256caBGA (14x14mm, 0.8mm pitch)	324caBGA (15x15mm, 0.8mm pitch)	400caBGA (17x17mm, 0.8mm pitch)	256ftBGA (17x17m, 1.0mm pitch)	324ftBGA (19x19mm, 1.0mm pitch)
LFXP2-17, 256ftBGA (Baseline qualification and smallest vertical CUP separation)	SMPC					MSL3	
	T/C						
	BHAST					264 hours	
	UHAST					264 hours	
	HTSL					1000 hours	
LFXP2-30, 256ftBGA (Largest die and smallest vertical CUP separation)	SMPC					MSL3	
	T/C					1000 cycles	
	BHAST						
	UHAST						
	HTSL						
LCMXO2280, 324ftBGA (Largest package)	SMPC						MSL3
	T/C						1000 cycles
	BHAST						
	UHAST						
	HTSL						1000 hours
LCMXO2280, 256ftBGA (Longest wire)	SMPC					MSL3	
	T/C					1000 cycles	
	BHAST					396 hours	
	UHAST						
	HTSL						
LCMXO2-1200, 132csBGA (65nm SRAM + Flash)	SMPC	MSL3					
	T/C						
	85/85	1000 hours					
	UHAST	264 hours					
	HTSL	1000 hours					
LCMXO3L/XO3LF-6900, caBGA (Package is qualified-by-similarity from the above product-package combinations)	SMPC		QBS	QBS	QBS		
	T/C						
	BHAST						
	UHAST						
	HTSL						
LCMXO3L/XO3LF-4300, caBGA (Package is qualified-by-similarity from the above product-package combinations)	SMPC		QBS	QBS	QBS		
	T/C						
	BHAST						
	UHAST						
	HTSL						
LCMXO3L/XO3LF-2100, caBGA (Package is qualified-by-similarity from the above product-package combinations)	SMPC		QBS	QBS			
	T/C						
	BHAST						
	UHAST						
	HTSL						
LCMXO3L/XO3LF-1300, caBGA (Package is qualified-by-similarity from the above product-package combinations)	SMPC		QBS				
	T/C						
	BHAST						
	UHAST						
	HTSL						

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Table 4.1.3 Cu-wire, caBGA Package Qualification-By-Similarity (QBS) Matrix at ATP

The LCMXO3L/XO3LF, caBGA product/package combinations are Qualified-by-Similarity (QBS) using the qualification vehicles below.	Stress Tests	Amkor Technology Philippines (ATP)			
		256caBGA (14x14mm, 0.8mm pitch)	324caBGA (15x15mm, 0.8mm pitch)	400caBGA (17x17mm, 0.8mm pitch)	484caBGA (19x19mm, 0.8mm pitch)
LCMXO3L/XO3LF-9400 (484caBGA is the lead caBGA qual vehicle) (256caBGA is worst-case die/package ratio)	SMPC	MSL3		QBS	MSL3
	T/C	700 cycles			700 cycles
	BHAST	QBS			264 hours
	uHAST				264 hours
	HTSL				1000 hours
LCMXO3L/XO3LF-6900 (400caBGA is the lead caBGA qual vehicle) (256caBGA is worst-case die/package ratio)	SMPC	MSL3	QBS	MSL3	
	T/C	700 cycles		700 cycles	
	BHAST	QBS		264 hours	
	HTSL			1000 hours	
LCMXO3L/XO3LF-4300 (Package is qualified-by-similarity from the LCMXO3L/XO3LF-6900 caBGAs)	SMPC	QBS	QBS	QBS	
	T/C				
	BHAST				
	HTSL				
LCMXO3L/XO3LF-2100 (Package is qualified-by-similarity from the LCMXO3L/XO3LF-6900 caBGAs)	SMPC	QBS	QBS		
	T/C				
	BHAST				
	HTSL				
LCMXO3L/XO3LF-1300 (Package is qualified-by-similarity from the LCMXO3L/XO3LF-6900 caBGAs)	SMPC	QBS			
	T/C				
	BHAST				
	HTSL				

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Table 4.1.4 csfBGA (or fcCSP) Package Qualification-By-Similarity (QBS) Matrix at ATT/ATP

The LCMXO3L/XO3LF, csfBGA product/package combinations are Qualified-by-Similarity (QBS) using the qualification vehicles below.	Stress Tests	Amkor Technology Taiwan (ATT) Amkor Technology Philippines (ATP)		
		121csfBGA (6x6mm, 0.5mm pitch)	256csfBGA (9x9mm, 0.5mm pitch)	324csfBGA (10x10mm, 0.5mm pitch)
LCMXO3L/XO3LF-9400 (256csfBGA is the lead csfBGA qual vehicle – largest package)	SMPC		MSL3	
	T/C		700 cycles	
	BHAST		264 hours	
	uHAST		264 hours	
	HTSL		1000 hours	
LCMXO3L/XO3LF-6900 (324csfBGA is the lead csfBGA qual vehicle – largest package)	SMPC		MSL3	MSL3
	T/C		700 cycles	700 cycles
	BHAST		QBS	264 hours
	uHAST		264 hours	QBS
	HTSL		1000 hours	
LCMXO3L/XO3LF-4300 (121csfBGA is worst-case die/package ratio)	SMPC	MSL3	QBS	QBS
	T/C	700 cycles		
	BHAST	QBS		
	uHAST			
	HTSL			
LCMXO3L/XO3LF-2100 (Package is qualified-by-similarity from the LCMXO3L/XO3LF-6900 csfBGAs)	SMPC	QBS	QBS	QBS
	T/C			
	BHAST			
	uHAST			
	HTSL			
LCMXO3L/XO3LF-1300 (Package is qualified-by-similarity from the LCMXO3L/XO3LF-6900 csfBGAs)	SMPC	QBS	QBS	
	T/C			
	BHAST			
	uHAST			
	HTSL			
LCMXO3L/XO3LF-640 (Package is qualified-by-similarity from the LCMXO3L/XO3LF-6900 csfBGAs)	SMPC	QBS		
	T/C			
	BHAST			
	uHAST			
	HTSL			

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4.2 Surface Mount Preconditioning (SMPC)

The SMPC Test is used to model the surface mount assembly conditions during component solder processing. This preconditioning is consistent with JEDEC JESD22-A113, “Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing”, Moisture Sensitivity Level 3 (MSL3) and Level 1 (MSL1) package moisture sensitivity and dry-pack storage requirements.

Surface Mount Preconditioning (MSL3): 5 Temperature Cycles; 24 hours Bake @ 125°C; 30°C/60% RH soak for 192 hours; 3X passes of reflow simulation performed before all[A] package stresses.
MSL3 Packages: csBGA, caBGA, ftBGA and csfBGA

Surface Mount Preconditioning (MSL1): 5 Temperature Cycles; 24 hours Bake @ 125°C; 85°C/85% RH soak for 168 hours; 3X passes of reflow simulation performed before all package stresses.
MSL1 Packages: WLCSP

Method: J-STD-020D.1/E[B] and JESD22-A113F/G[B]/H

Table 4.2.1 SMPC Data

Product Name	Package	Assembly Site	Lot Number	Moisture Soak Level	3X Reflow Temperature	Quantity	# of Fails
LFXP2-17	256ftBGA	ASEM	Lot #1	MSL3	260°C	231	0
LFXP2-17	256ftBGA	ASEM	Lot #2	MSL3	260°C	231	0
LFXP2-17	256ftBGA	ASEM	Lot #3	MSL3	260°C	231	0
LFXP2-17	256ftBGA	ASEM	Lot #4[C]	MSL3	260°C	77	0
LFXP2-30	256ftBGA	ASEM	Lot #1	MSL3	260°C	77	0
LFXP2-30	256ftBGA	ASEM	Lot #2	MSL3	260°C	77	0
LFXP2-30	256ftBGA	ASEM	Lot #3	MSL3	260°C	77	0
LFXP2-30	256ftBGA	ASEM	Lot #4[C]	MSL3	260°C	77	0
LCMXO2280	256ftBGA	ASEM	Lot #1	MSL3	260°C	154	0
LCMXO2280	256ftBGA	ASEM	Lot #2	MSL3	260°C	154	0
LCMXO2280	256ftBGA	ASEM	Lot #3	MSL3	260°C	154	0
LCMXO2280	256ftBGA	ASEM	Lot #4	MSL3	260°C	77	0
LCMXO2280	256ftBGA	ASEM	Lot #5	MSL3	260°C	77	0
LCMXO2280	256ftBGA	ASEM	Lot #6	MSL3	260°C	77	0
LCMXO2280	324ftBGA	ASEM	Lot #1	MSL3	260°C	154	0
LCMXO2280	324ftBGA	ASEM	Lot #2	MSL3	260°C	154	0
LCMXO2280	324ftBGA	ASEM	Lot #3	MSL3	260°C	154	0
LCMXO2-1200	132csBGA	ASEM	Lot #1	MSL3	260°C	184	0
LCMXO2-1200	132csBGA	ASEM	Lot #2	MSL3	260°C	184	0
LCMXO2-1200	132csBGA	ASEM	Lot #3	MSL3	260°C	184	0
LCMXO3L/XO3LF-4300E	81WLCSP	ATT	Lot #1	MSL1	260°C	164	0
LCMXO3L/XO3LF-4300E	81WLCSP	ATT	Lot #2	MSL1	260°C	164	0
LCMXO3L/XO3LF-4300E	81WLCSP	ATT	Lot #3	MSL1	260°C	163	0
LCMXO3L/XO3LF-6900C	256caBGA	ATP	Lot #1	MSL3	260°C	266	0
LCMXO3L/XO3LF-6900C	256caBGA	ATP	Lot #2	MSL3	260°C	258	0
LCMXO3L/XO3LF-6900C	256caBGA	ATP	Lot #3	MSL3	260°C	307	0
LCMXO3L/XO3LF-6900C	400caBGA	ATP	Lot #1	MSL3	260°C	83	0
LCMXO3L/XO3LF-6900C	400caBGA	ATP	Lot #2	MSL3	260°C	84	0
LCMXO3L/XO3LF-6900C	400caBGA	ATP	Lot #3	MSL3	260°C	84	0

Product Name	Package	Assembly Site	Lot Number	Moisture Soak Level	3X Reflow Temperature	Quantity	# of Fails
LCMXO3L/XO3LF-6900E	324csfBGA	ATT/ATP	Lot #1	MSL3	260°C	170	0
LCMXO3L/XO3LF-6900E	324csfBGA	ATT/ATP	Lot #2	MSL3	260°C	170	0
LCMXO3L/XO3LF-6900E	324csfBGA	ATT/ATP	Lot #3	MSL3	260°C	170	0
LCMXO3L/XO3LF-6900E	256csfBGA	ATT/ATP	Lot #1	MSL3	260°C	160	0
LCMXO3L/XO3LF-6900E	256csfBGA	ATT/ATP	Lot #2	MSL3	260°C	160	0
LCMXO3L/XO3LF-6900E	256csfBGA	ATT/ATP	Lot #3	MSL3	260°C	160	0
LCMXO3L/XO3LF-4300E	121csfBGA	ATT/ATP	Lot #1	MSL3	260°C	85	0
LCMXO3L/XO3LF-4300E	121csfBGA	ATT/ATP	Lot #2	MSL3	260°C	85	0
LCMXO3L/XO3LF-4300E	121csfBGA	ATT/ATP	Lot #3	MSL3	260°C	85	0
LCMXO3L/XO3LF-9400C	484caBGA	ATP	Lot #1	MSL3	260°C	399	0
LCMXO3L/XO3LF-9400C	484caBGA	ATP	Lot #2	MSL3	260°C	400	0
LCMXO3L/XO3LF-9400C	484caBGA	ATP	Lot #3	MSL3	260°C	400	0
LCMXO3L/XO3LF-9400C	256caBGA	ATP	Lot #1	MSL3	260°C	160	0
LCMXO3L/XO3LF-9400C	256caBGA	ATP	Lot #2	MSL3	260°C	160	0
LCMXO3L/XO3LF-9400C	256caBGA	ATP	Lot #3	MSL3	260°C	160	0
LCMXO3L/XO3LF-9400E	256csfBGA	ATP	Lot #1	MSL3	260°C	399	0
LCMXO3L/XO3LF-9400E	256csfBGA	ATP	Lot #2	MSL3	260°C	400	0
LCMXO3L/XO3LF-9400E	256csfBGA	ATP	Lot #3	MSL3	260°C	400	0
LCMXO3L/XO3LF-9400C[D]	484caBGA	ATP	Lot #2	MSL3	260°C	240	0
LCMXO3L/XO3LF-9400C[D]	484caBGA	ATP	Lot #3	MSL3	260°C	240	0
LCMXO3L/XO3LF-9400C[D]	256caBGA	ATP	Lot #1	MSL3	260°C	80	0
LCMXO3L/XO3LF-9400C[D]	256caBGA	ATP	Lot #2	MSL3	260°C	80	0
LCMXO3L/XO3LF-9400C[D]	256caBGA	ATP	Lot #3	MSL3	260°C	80	0
LCMXO3L/XO3LF-2100E[E]	49WLCSP	ATT	Lot #1	MSL1	260°C	250	0
LCMXO3L/XO3LF-2100E[E]	49WLCSP	ATT	Lot #2	MSL1	260°C	248	0
LCMXO3L/XO3LF-2100E[E]	49WLCSP	ATT	Lot #3	MSL1	260°C	250	0
LCMXO3L/XO3LF-9400C[D]	484caBGA	ATP	Lot #1	MSL3	260°C	250	0
LCMXO3L/XO3LF-9400C[D]	484caBGA	ATP	Lot #2	MSL3	260°C	250	0
LCMXO3L/XO3LF-9400E[D]	484caBGA	ATP	Lot #3	MSL3	260°C	250	0

[A]Except for HTSL where it's only required for wirebonded packages (caBGA)
[B]Intercepts csfBGA package qualification
[C]These lots were built using the worst-case wire bond DOE parameters to ensure a robust process
[D]Hi-Thermal QMI529HT-LV Die Attach + SAC305 Solderball (PCN#06A-17)
[E]Site transfer from ATT5 (Hsinchu) + ATT1 (Taouyuan)

Cumulative SMPC Failure Rate = 0 / 10,699

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4.3 Temperature Cycling (TC)

The TC test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104 “Temperature Cycling”, Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csBGA, caBGA, ftBGA and csfBGA

MSL1 Packages: WLCSP

Stress Duration: 700 cycles

Stress Conditions: Temperature cycling between -55°C to 125°C

Method: JESD22-A104D/E[A], Condition B

Table 4.3.1 TC Data

Product Name	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Quantity	# of Fails
LFXP2-30	256ftBGA	ASEM	Lot #1	-55°C to 125°C	1000 cycles	77	0
LFXP2-30	256ftBGA	ASEM	Lot #2	-55°C to 125°C	1000 cycles	77	0
LFXP2-30	256ftBGA	ASEM	Lot #3	-55°C to 125°C	1000 cycles	77	0
LFXP2-30	256ftBGA	ASEM	Lot #4[B]	-55°C to 125°C	1000 cycles	77	0
LCMXO2280	256ftBGA	ASEM	Lot #1	-55°C to 125°C	1000 cycles	77	0
LCMXO2280	256ftBGA	ASEM	Lot #2	-55°C to 125°C	1000 cycles	77	1[C]
LCMXO2280	256ftBGA	ASEM	Lot #3	-55°C to 125°C	1000 cycles	77	0
LCMXO2280	324ftBGA	ASEM	Lot #1	-55°C to 125°C	1000 cycles	77	0
LCMXO2280	324ftBGA	ASEM	Lot #2	-55°C to 125°C	1000 cycles	77	0
LCMXO2280	324ftBGA	ASEM	Lot #3	-55°C to 125°C	1000 cycles	77	0
LCMXO3L/XO3LF-4300E	81WLCSP	ATT	Lot #1	-55°C to 125°C	700 cycles	77	0
LCMXO3L/XO3LF-4300E	81WLCSP	ATT	Lot #2	-55°C to 125°C	700 cycles	77	0
LCMXO3L/XO3LF-4300E	81WLCSP	ATT	Lot #3	-55°C to 125°C	700 cycles	77	0
LCMXO3L/XO3LF-6900C	256caBGA	ATP	Lot #1	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-6900C	256caBGA	ATP	Lot #2	-55°C to 125°C	700 cycles	77	0
LCMXO3L/XO3LF-6900C	256caBGA	ATP	Lot #3	-55°C to 125°C	700 cycles	77	0
LCMXO3L/XO3LF-6900C	400caBGA	ATP	Lot #1	-55°C to 125°C	700 cycles	92	0
LCMXO3L/XO3LF-6900C	400caBGA	ATP	Lot #2	-55°C to 125°C	700 cycles	86	0
LCMXO3L/XO3LF-6900C	400caBGA	ATP	Lot #3	-55°C to 125°C	700 cycles	101	0
LCMXO3L/XO3LF-6900E	324csfBGA	ATT/ATP	Lot #1	-55°C to 125°C	700 cycles	85	0
LCMXO3L/XO3LF-6900E	324csfBGA	ATT/ATP	Lot #2	-55°C to 125°C	700 cycles	85	0
LCMXO3L/XO3LF-6900E	324csfBGA	ATT/ATP	Lot #3	-55°C to 125°C	700 cycles	85	0

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Product Name	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Quantity	# of Fails
LCMXO3L/XO3LF-6900E	256csfBGA	ATT/ATP	Lot #1	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-6900E	256csfBGA	ATT/ATP	Lot #2	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-6900E	256csfBGA	ATT/ATP	Lot #3	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-4300E	121csfBGA	ATT/ATP	Lot #1	-55°C to 125°C	700 cycles	85	0
LCMXO3L/XO3LF-4300E	121csfBGA	ATT/ATP	Lot #2	-55°C to 125°C	700 cycles	85	0
LCMXO3L/XO3LF-4300E	121csfBGA	ATT/ATP	Lot #3	-55°C to 125°C	700 cycles	85	0
LCMXO3L/XO3LF-9400C	256caBGA	ATP	Lot #1	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-9400C	256caBGA	ATP	Lot #2	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-9400C	256caBGA	ATP	Lot #3	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-9400C	484caBGA	ATP	Lot #1	-55°C to 125°C	700 cycles	79	0
LCMXO3L/XO3LF-9400C	484caBGA	ATP	Lot #2	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-9400C	484caBGA	ATP	Lot #3	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-9400E	256csfBGA	ATP	Lot #1	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-9400E	256csfBGA	ATP	Lot #2	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-9400E	256csfBGA	ATP	Lot #3	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-9400C[D]	256caBGA	ATP	Lot #1	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-9400C[D]	256caBGA	ATP	Lot #2	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-9400C[D]	256caBGA	ATP	Lot #3	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-9400C[D]	484caBGA	ATP	Lot #1	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-9400C[D]	484caBGA	ATP	Lot #2	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-9400C[D]	484caBGA	ATP	Lot #3	-55°C to 125°C	700 cycles	80	0
LCMXO3L/XO3LF-2100E[E]	49WLCSP	ATT	Lot #1	-55°C to 125°C	700 cycles	82	0
LCMXO3L/XO3LF-2100E[E]	49WLCSP	ATT	Lot #2	-55°C to 125°C	700 cycles	82	0
LCMXO3L/XO3LF-2100E[E]	49WLCSP	ATT	Lot #3	-55°C to 125°C	700 cycles	82	0

[A]Intercepts csfBGA package qualification.
[B]These lots were built using the worst-case wire bond DOE parameters to ensure a robust process.
[C]One random defect unrelated to copper wirebond process.
[D]Hi-Thermal QMI529HT-LV Die Attach + SAC305 Solderball (PCN#06A-17)
[E]Site transfer from ATT5 (Hsinchu) + ATT1 (Taouyuan)

Cumulative Temp Cycle Failure Rate = 1/3,709
Cumulative device Temp Cycles = 2,827,300

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4.4 Unbiased HAST (uHAST)

uHAST testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent with JEDEC JESD22-A118, "Accelerated Moisture Resistance - Unbiased HAST," the unbiased HAST conditions are either 96 hours exposure at 130°C and 85% relative humidity, or 264 hours exposure at 110°C and 85% relative humidity. Prior to unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csBGA, caBGA, ftBGA and csfBGA
MSL1 Packages: WLCSP
Stress Conditions: 110°C/85% RH or 130°C/85%RH
Stress Duration: 264 hours or 96 hours

Method: JESD22-A118A/B[A]

Table 4.4.1 uHAST Data

Product Name	Package	Assembly Site	Lot Number	Stress Humidity	Stress Temperature	Stress Duration	Qty	# of Fails
LFXP2-17	256ftBGA	ASEM	Lot #1	85% RH	110°C	264 hours	77	0
LFXP2-17	256ftBGA	ASEM	Lot #2	85% RH	110°C	264 hours	77	0
LFXP2-17	256ftBGA	ASEM	Lot #3	85% RH	110°C	264 hours	76[B]	0
LCMXO2-1200	132csBGA	ASEM	Lot #1	85% RH	110°C	264 hours	77	0
LCMXO2-1200	132csBGA	ASEM	Lot #2	85% RH	110°C	264 hours	77	0
LCMXO2-1200	132csBGA	ASEM	Lot #3	85% RH	110°C	264 hours	77	0
LCMXO3L/XO3LF-4300E	81WLCSP	ATT	Lot #1	85% RH	110°C	264 hours	77	0
LCMXO3L/XO3LF-4300E	81WLCSP	ATT	Lot #2	85% RH	110°C	264 hours	77	0
LCMXO3L/XO3LF-4300E	81WLCSP	ATT	Lot #3	85% RH	110°C	264 hours	77	0
LCMXO3L/XO3LF-6900E	256csfBGA	ATT/ATP	Lot #1	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-6900E	256csfBGA	ATT/ATP	Lot #2	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-6900E	256csfBGA	ATT/ATP	Lot #3	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400C	256caBGA	ATP	Lot #1	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400C	256caBGA	ATP	Lot #2	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400C	256caBGA	ATP	Lot #3	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400C	484caBGA	ATP	Lot #1	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400C	484caBGA	ATP	Lot #2	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400C	484caBGA	ATP	Lot #3	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400E	256csfBGA	ATP	Lot #1	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400E	256csfBGA	ATP	Lot #2	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400E	256csfBGA	ATP	Lot #3	85% RH	110°C	264 hours	80	0

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Product Name	Package	Assembly Site	Lot Number	Stress Humidity	Stress Temperature	Stress Duration	Qty	# of Fails
LCMXO3L/XO3LF-9400C[C]	256caBGA	ATP	Lot #1	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400C[C]	256caBGA	ATP	Lot #2	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400C[C]	256caBGA	ATP	Lot #3	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400C[C]	484caBGA	ATP	Lot #1	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400C[C]	484caBGA	ATP	Lot #2	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400C[C]	484caBGA	ATP	Lot #3	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-2100E[D]	49WLCSP	ATT	Lot #1	85% RH	130°C	96 hours	155	0
LCMXO3L/XO3LF-2100E[D]	49WLCSP	ATT	Lot #2	85% RH	130°C	96 hours	155	0
LCMXO3L/XO3LF-2100E[D]	49WLCSP	ATT	Lot #3	85% RH	130°C	96 hours	154	0

[A]Intercepts csfBGA package qualification.
[B]One unit removed due to mechanical handler damage
[C]Hi-Thermal QMI529HT-LV Die Attach + SAC305 Solderball (PCN#06A-17)
[D]Site transfer from ATT5 (Hsinchu) + ATT1 (Taouyuan)

Cumulative Unbiased HAST failure Rate = 0 / 3,060
Cumulative Unbiased HAST device hours = 607,392

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4.5 Steady State Humidity Bias Life Test (85/85) or Biased Highly-Accelerated Temperature and Humidity Stress Test (BHAST)

HAST activates the same failure mechanisms as the 85/85 test. HAST uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The much longer duration 85/85 stress test uses temperature alone to accelerate penetration of moisture into the package and to the die surface. These biased Temperature/Humidity stresses are used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD22-A110 “Highly-Accelerated Temperature and Humidity Stress Test (HAST)”, the BHAST Condition B is 264 hours exposure at 110°C and 85% relative humidity, while the JEDEC JESD22-A101C “Steady State Temperature Humidity Bias Life Test is 1000 hours exposure at 85°C and 85% relative humidity. Prior to Biased HAST or 85/85 testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csBGA, caBGA, ftBGA and csfBGA

MSL1 Packages: WLCSP

Stress Conditions: Vcc= Max operating condition and 130°C/85% RH, 110°C/85% RH or 85°C/85% RH

Stress Duration: 96 Hours, 264 hours, or 1000 hours, respectively

Method: JESD22-A110D/E[A] or JESD22-A101C

Table 4.5.1 BHAST Data

Product Name	Package	Assembly Site	Lot Number	Stress Humidity	Stress Temperature	Stress Duration	Qty	# of Fails
LFXP2-17	256-ftBGA	ASEM	Lot #1	85% RH	110°C	264 hours	77	0
LFXP2-17	256-ftBGA	ASEM	Lot #2	85% RH	110°C	264 hours	77	0
LFXP2-17	256-ftBGA	ASEM	Lot #3	85% RH	110°C	264 hours	77	0
LCMXO2280	256-ftBGA	ASEM	Lot #1	85% RH	110°C	264 hours	77	1[B]
LCMXO2280	256-ftBGA	ASEM	Lot #2	85% RH	110°C	264 hours	77	1[B]
LCMXO2280	256-ftBGA	ASEM	Lot #3	85% RH	110°C	264 hours	77	1[B]
LCMXO2280	256-ftBGA	ASEM	Lot #4	85% RH	110°C	264 hours	77	0
LCMXO2280	256-ftBGA	ASEM	Lot #5	85% RH	110°C	264 hours	77	0
LCMXO2280	256-ftBGA	ASEM	Lot #6	85% RH	110°C	264 hours	77	1[B]
LCMXO2-1200	132-csBGA	ASEM	Lot #1	85% RH	85°C	1000 hours	25	0
LCMXO2-1200	132-csBGA	ASEM	Lot #2	85% RH	85°C	1000 hours	25	1[B]
LCMXO2-1200	132-csBGA	ASEM	Lot #3	85% RH	85°C	1000 hours	25	0
LCMXO3L/XO3LF-6900C	400-caBGA	ATP	Lot #1	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-6900C	400-caBGA	ATP	Lot #2	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-6900C	400-caBGA	ATP	Lot #3	85% RH	110°C	264 hours	80	0

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Product Name	Package	Assembly Site	Lot Number	Stress Humidity	Stress Temperature	Stress Duration	Qty	# of Fails
LCMXO3L/XO3LF-6900E	324csfBGA	ATT/ATP	Lot #1	85% RH	110°C	264 hours	81	0
LCMXO3L/XO3LF-6900E	324csfBGA	ATT/ATP	Lot #2	85% RH	110°C	264 hours	81	0
LCMXO3L/XO3LF-6900E	324csfBGA	ATT/ATP	Lot #3	85% RH	110°C	264 hours	80	1[C]
LCMXO3L/XO3LF-9400C	484-caBGA	ATP	Lot #1	85% RH	110°C	264 hours	75	1[B]
LCMXO3L/XO3LF-9400C	484-caBGA	ATP	Lot #2	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400C	484-caBGA	ATP	Lot #3	85% RH	110°C	264 hours	80	1[B]
LCMXO3L/XO3LF-9400C	484-caBGA	ATP	Lot #4	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400E	256-csfBGA	ATP	Lot #1	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400E	256-csfBGA	ATP	Lot #2	85% RH	110°C	264 hours	80	0
LCMXO3L/XO3LF-9400E	256-csfBGA	ATP	Lot #3	85% RH	110°C	264 hours	80	0

[A]Intercepts csfBGA package qualification.
[B]Random defect unrelated to copper wirebond process
[C]#SC1511019: elevated pu leakage on 2 pins – ongoing investigation

Cumulative BHAST failure Rate = 7 / 1,730
Cumulative BHAST device hours = 456,720

Cumulative THB failure Rate = 1 / 75
Cumulative THB device hours = 75,000

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4.6 High Temperature Storage Life (HTSL)

HTSL Test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms. Consistent with JEDEC JESD22-A103, the devices are subjected to high temperature storage Condition B: +150 (-0/+10) °C for 1000 hours. Prior to High Temperature Storage, per JESD47, all[A] Pb-free, wirebonded devices are to be subjected to Surface Mount Preconditioning.

MSL3 Packages: csBGA, caBGA, ftBGA and csfBGA

MSL1 Packages: WLCSP

Stress Duration: 1000 hours

Temperature: 150°C (ambient)

Method: JESD22-A103D/E[B]

Table 4.6.1 HTSL Data

Product Name	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Quantity	# of Fails
LCMXO2-1200	132-csBGA	ASEM	Lot #1	150°C	1000 Hours	77	0
LCMXO2-1200	132-csBGA	ASEM	Lot #2	150°C	1000 Hours	76[C]	0
LCMXO2-1200	132-csBGA	ASEM	Lot #3	150°C	1000 Hours	77	0
LFXP2-17	256-ftBGA	ASEM	Lot #1	150°C	1000 hours	77	0
LFXP2-17	256-ftBGA	ASEM	Lot #2	150°C	1000 hours	77	0
LFXP2-17	256-ftBGA	ASEM	Lot #3	150°C	1000 hours	77	0
LFXP2-17	256-ftBGA	ASEM	Lot #4[D]	150°C	1000 hours	76[C]	0
LCMXO2280	324-ftBGA	ASEM	Lot #1	150°C	1000 hours	77	0
LCMXO2280	324-ftBGA	ASEM	Lot #2	150°C	1000 hours	77	0
LCMXO2280	324-ftBGA	ASEM	Lot #3	150°C	1000 hours	77	0
LCMXO3L/XO3LF-4300E	81-WLCSP	ATT	Lot #1	150°C	1000 hours	77	0
LCMXO3L/XO3LF-4300E	81-WLCSP	ATT	Lot #2	150°C	1000 hours	77	0
LCMXO3L/XO3LF-4300E	81-WLCSP	ATT	Lot #3	150°C	1000 hours	76	0
LCMXO3L/XO3LF-6900C	400-caBGA	ATP	Lot #1	150°C	1000 hours	89	0
LCMXO3L/XO3LF-6900C	400-caBGA	ATP	Lot #2	150°C	1000 hours	86	0
LCMXO3L/XO3LF-6900C	400-caBGA	ATP	Lot #3	150°C	1000 hours	78	0
LCMXO3L/XO3LF-6900E	256csfBGA	ATT/ATP	Lot #1	150°C	1000 hours	80	0
LCMXO3L/XO3LF-6900E	256csfBGA	ATT/ATP	Lot #2	150°C	1000 hours	80	0
LCMXO3L/XO3LF-6900E	256csfBGA	ATT/ATP	Lot #3	150°C	1000 hours	80	0

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Product Name	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Quantity	# of Fails
LCMXO3L/XO3LF-9400C	484-caBGA	ATP	Lot #1	150°C	1000 hours	80	0
LCMXO3L/XO3LF-9400C	484-caBGA	ATP	Lot #2	150°C	1000 hours	80	0
LCMXO3L/XO3LF-9400C	484-caBGA	ATP	Lot #3	150°C	1000 hours	80	0
LCMXO3L/XO3LF-9400E	256-csfBGA	ATP	Lot #1	150°C	1000 hours	80	0
LCMXO3L/XO3LF-9400E	256-csfBGA	ATP	Lot #2	150°C	1000 hours	80	0
LCMXO3L/XO3LF-9400E	256-csfBGA	ATP	Lot #3	150°C	1000 hours	80	0

[A]Does not apply to WLCSP and csfBGA
[B]Intercepts csfBGA package qualification.
[C]One unit removed due to mechanical handler damage.
[D]Lot was built using the worst-case wire bond DOE parameters to ensure a robust process.

Cumulative HTSL failure Rate = 0 / 1,971
Cumulative HTSL device hours = 1,971,000

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5.0 MACHXO3L/MACHXO3LF PROCESS WAFER LEVEL RELIABILITY (WLR)

Several key wafer fabrication process related parameters affect the Reliability of the End-Product. These parameters are tested during the Development Phase of the Technology. Passing data (a 10yr lifetime at the reliability junction temperature) must be obtained for three lots minimum for each parameter before release to production. These parameters are:

Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.

Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.

Negative Bias Temperature Instability (**NBTI**): Symptom is a shift in Vth (also a reduction in Idsat).

Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.

Stress Migration (**SM**): Symptom is a void (open) in a metal Via due to microvoid coalescence.

Table 5.0.1 WLR Results

HCI

Device	LVN	LVP	MVN	MVP	HVN	HVP
delta Ids	-10%	-10%	-10%	-10%	-10%	-10%
Celsius	25	25	25	25	25	25
Vgstress	Vd/2	Vd	Vd/2	Vd	Vd/2	Vd
Vds	1.26	-1.26	3.465	-3.465	5.25	-5.25
0.1% TTF	3 lots>34yr DC	3 lots>71yr	3 lots>20yr AC	3 lots>684yr	3 lots >3.5e6 s DC*	3 lots >1e9 s DC*

TDDB

Device	LVN	LVP	MVN	MVP	HVN	HVP	Intermediate IMD	Semi-Global IMD
Celsius	100	100	100	100	100	100	100	100
Vg	1.26	-1.26	3.465	-3.465	5.25	-5.25	3.465	3.465
Max Area	2.2 cm^2	22 cm^2	1 cm^2	2.5 cm^2	5e-4 cm^2	5e-4 cm^2	L/S=100nm	L/S=200nm
0.1% TTF	3 lots>2.5e5 yr	3 lots>1.4e3 yr	3 lots>25yr	3 lots>390 yr	3 lots>1.2e3 yr	3 lots>20 yr	3 lots>229yr	3 lots>6690yr

NBTI

Device	LVP	MVP
delta Vth	50mv	100mv
Celsius	100	100
Vg	-1.26	-3.465
0.1% TTF	3 lots>5.8e5 yr	3 lots>4.2e3 yr

EML

Device	Intermediate	Semi-Global	Global	Top Al
Celsius	100	100	100	100
delta R	+5%	+5%	+5%	+5%
Jmax	6.65E+05	6.65E+05	6.65E+05	2.85E+05
0.1% TTF	3 lots>380 yr	3 lots>77 yr	3 lots>22 yr	3 lots>70yr

SM

Device	Intermediate	Semi-Global	Global
delta R	+100%	+100%	+100%
Celsius	100	100	100
0.1% TTF	3 lots>2400 yr	3 lots>328 yr	3 lots>1.1e4 yr

Note: Reliability life times are based on listed temperature and use conditions. A Detailed WLR report is available upon request. Lattice Semiconductor Corporation document #73-106883.

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6.0 MACHXO3L/MACHXO3LF SOFT ERROR RATE DATA

Soft Error Rate (SER) testing is conducted to characterize the sensitivity of SRAM storage and device logic elements to High Energy Neutron and Alpha Particle radiation. Charge induced by the impact of these particles can collect at sensitive nodes in the device, and result in changes in the internal electrical states of the device. While these changes do not cause physical damage to the device, they can cause a logical error in device operation.

Neutron SRAM SER Rate – This characteristic is the rate of upset of Configuration RAM and Embedded Block RAM (EBR) cells during neutron testing. Devices were configured with a logic pattern, exposed to measured neutron doses, and the device configuration was read back from the device. Changed bits are identified through pattern comparison. Neutron testing is normalized to the published neutron flux rate for New York City at sea level. This rate is measured as Failures in Time (FITs) normalized per million bits in the device to allow for translation across the device families densities.

Alpha SRAM SER Rate – This characteristic is the rate of upset of Configuration RAM and Embedded Block RAM (EBR) cells during Alpha particle testing. Devices were configured with a logic pattern, exposed for a fixed time period to a calibrated Alpha particle source, and the device configuration was read back from the device. Changed bits are identified through pattern comparison. Alpha particle testing is normalized to a background rate of 0.001Alpha/cm2-hr based on characterization of packaging materials. This rate is measured at Failures in Time (FITs) normalized per million bits in the device to allow for translation across the device families densities as Failures in Time (FITs) normalized per million bits in the device to allow for translation across the device families densities.

All testing conforms to JEDEC JESD-89A.

Table 6.0.1 MachXO3L/MachXO3LF MEASURED FITs / Mb

Stress / Structure	SRAM Type	MachXO3L/MachXO3LF Measured Fuses	Failures in Time per Megabit (FITs/Mb)
High Energy Neutron	** Configuration RAM	359,640	363
	* EBR	73,728	611
Alpha Particle	** Configuration RAM	359,640	128
	* EBR	73,728	363

* The EBR SER data was taken on the ECP3. The MachXO3L/MachXO3LF shares the same base technology and SRAM cell.
** The Configuration RAM data was taken on the MachXO2. The MachXO3L/MachXO3LF shares the same base technology and SRAM cell.

Note: Detailed MachXO2 and ECP3 SER reports are available upon request. Lattice Semiconductor Corporation documents #25-106920 and #25-106669 respectively.

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7.0 BOARD LEVEL RELIABILITY (BLR) STRESS METHODS

Reliability testing methods for surface mount electronic components in Wafer Level Chip Scale Packaging (WLCSP) assembled onto printed circuit boards (PCB) are focused on the stresses observed by the manufacturing and test processes and the applications associated with handheld electronic products. The handheld electronic products fit into the consumer and portable market segments with products such as cameras, calculators, cell phones, pagers, palm size PCs, PCMCIA cards, and the like. Special daisy chain test vehicles are constructed for board level reliability (BLR) testing to emulate as closely as possible, the design, material sets and assembly processes of the actual product being qualified.

BLR PCB test boards are designed per JEDEC JESD22-B111 requirements: 0.8mm thick board with 1+6+1 stack (8 layers) layup coated with OSP “Organic Surface Protection”. Units are arranged in a 3x5 configuration on the board measuring 77mm x 132mm. One side provides VIP “Via-In-Pad” connections to the BGA and the flip side provides NVIP “No-VIP” (surface-trace) connections. The design of pad to surface traces must avoid trace cracks. BGA balls mount to NSMD “Non Solder Mask Defined” pads on the PCB.

Board Level Slow-Temperature Cycling (the slowest speed BLR stress) is intended to evaluate and compare the PCB performance of surface mount electronics components in an environment that accelerates solder joint fatigue and creep for handheld electronic products and applications. Pass/fail event detection is accomplished using resistance measurements. All stress tests are performed in accordance with IPC-JEDEC9701A & JESD22-A104, condition G, soak mode 2. Repeated slow-temperature cycling of printed circuit boards from -40C to +125C, for up to 1,000 cycles. Handheld electronic products passing criteria is 208 cycles.

Board Level Cyclic Bend Test (the medium speed BLR stress) is intended to evaluate and compare the PCB performance of surface mount electronics components in an environment that accelerates various assembly and test operations and actual use conditions such as repeated key-presses in mobile phone during the life of the product for handheld electronic products and applications. Pass/fail event detection is accomplished using resistance measurements. All stress tests are performed in accordance with IPC-JEDEC9702 & JEDEC JESD22-B113. Repeated bending of printed circuit boards at 1 to 3 Hz cyclic frequency for up to 200,000 cycles with maximum cross-head displacement of 4 mm. Handheld electronic products passing criteria is 20,000 cycles.

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Board Level Drop & Mechanical Shock (the instantaneous BLR stress) is intended to evaluate and compare PCB drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment determine the compatibility of the component(s) to withstand moderately severe shocks as a result of suddenly applied forces or abrupt change in motion produced by handling, transportation or field operation. Further, handheld electronic products are more prone to being dropped during their useful service life because of their size and weight. Pass/fail event detection is accomplished using datalogging 'opens' detectors. All stress tests are performed in accordance with IPC-JEDEC9703 & JEDEC JESD22-B111 (drop) and JESD-B104 (shock). Repeated drop testing of printed circuit boards at 1500g, 0.5 millisecond half-sine pulse and 2900g, 0.3 millisecond half-sine pulse for up to 1,000 drops. Handheld electronic products passing criteria is 30 drops.

Slow-TC 1st fail is >208 cycles = PASS
Bend testing did not fail after 20,000 cycles = PASS
Drop & Mechanical Shock testing 1st fail is >30 drops @ 2900g = PASS

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Table 7.0.1 Slow-Temperature Cycling

Assembly Site	Product & Package	Die Size (mm)	Ball Pitch (mm)	Temp Range (C) & Dwell time (min)	Cycles per hour	Sample Size	Consumer >208 cycles min.	1st Fail (Cycles)	N (63.2%) (Cycles)	% Fails @ 1,000 Cycles
ATT	LCMXO3L/XO3LF-4300E-81WLCSP	3.7 x 3.8	0.4	-40C to +125C & 5 min at each endpoint	1.5	247 units from 3 lots	Pass	N/A	N/A	0

Table 7.0.2 Bend Testing

Assembly Site	Product & Package	Die Size (mm)	Ball Pitch (mm)	Cross-head Displacement	Frequency (Hz)	Sample Size	Consumer >20,000 bends	1st Fail (Cycles)	N (63.2%) (Cycles)	% Fails @ 200,000 Cycles
ATT	LCMXO3L/XO3LF-4300E-81WLCSP	3.7 x 3.8	0.4	4 mm	1	71 units from 3 lots	Pass	98,000	N/A	7.0

Table 7.0.3 Drop & Mechanical Shock Testing

Assembly Site	Product & Package	Die Size	Ball Pitch (mm)	Drop & Shock	Waveform	Sample Size	Jedec >30 drops	1st Fail (Drops)	N (63.2%) (Drops)	% Fails @ 1,000 Drops
ATT	LCMXO3L/XO3LF-4300E-81WLCSP	3.7 x 3.8	0.4	2900g	0.3 ms half-sine pulse	180 units from 3 lots	Pass	257	N/A	16.1

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8.0 MACHXO3L/MACHXO3LF ADDITIONAL FAMILY DATA

Table 8.0.1 MachXO3L/MachXO3LF Package Assembly Data

Package Attributes/ Assembly Sites	Advanced Semiconductor Engineering, Malaysia (ASEM)	Amkor Philippines (ATP)	Amkor Taiwan (ATT)	Amkor Taiwan (ATT)/ Amkor Philippines (ATP)
Die Family (Product Line)	MACHXO3L/MACHXO3LF	MACHXO3L/MACHXO3LF	MACHXO3L/MACHXO3LF	MACHXO3L/MACHXO3LF
Fabrication Process Technology	Fujitsu 65nm CMOS	Fujitsu 65nm CMOS	Fujitsu 65nm CMOS	Fujitsu 65nm CMOS
Package Assembly Site	Malaysia	Philippines	Taiwan	Taiwan/ Philippines
Package Type	caBGA	caBGA	WLCSP	csfBGA
Ball/Lead Counts	256, 324, 400	256, 324, 400, 484	36, 49, 81	121, 256, 324
Die Preparation / Singulation	wafer saw / full cut	wafer saw / full cut	wafer saw / full cut	wafer saw / full cut
Die Attach Material	Ablebond 2100A	Ablebond 2300 PCN#06A-17: QMI529HT-LV	N/A	SCF-5
Mold Compound Supplier/ID	KEG-1250LKDS	GE-110	N/A	MUF-28
Mold Compound Chlorine (Cl-) content	< 10 ppm	< 10 ppm	N/A	≤ 50ppm
Mold Compound pH level	5 to 7	5 to 7	N/A	6.5 ± 0.5
Wire Bond Material	Palladium-coated Copper (PdCu)	Palladium-coated Copper (PdCu)	N/A	N/A
Wire Bond Methods	Thermosonic Ball	Thermosonic Ball	N/A	N/A
RDL / UBM	N/A	N/A		AZ4620
PBO1 / PBO2	N/A	N/A	HD8820	HD8820
Marking	Laser	Laser	Laser	Laser
Substrate	Core: CCL-HL83NX(A); Prepeg: GHPL830NX(A); Soldermask : AUS308	HL832NX-A; AUS320 Cu-OSP Bottom Finish PCN#06A-17: NiAu Bottom Finish	N/A	HL832NS
Solder ball Material	SAC305	SAC125Ni PCN#06A-17: SAC305	SAC405	SAC125Ni* (9400HE) / SAC 305 (others)

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9.0 REVISION HISTORY

Table 9.0.1 MachXO3L/MachXO3LF Product Family Qualification Summary revisions

Date	Revision	Section	Change Summary
January 2014	A	---	Initial document release.
August 2014	B		81-WLCSP update at new assembly house, Amkor Technology Taiwan (ATT); remove Revision Levels from Jedec tables.
October 2014	C		81-WLCSP update; update Product Qualification Process Flowchart; remove ESD MM from Standard Qualification Testing table (no longer applicable).
November 2014	D		256, 324, 400-caBGA packages at new assembly house, Amkor Technology Philippines.
March 2015	E		Add new XO3LF products; remove ASET.
September 2015	F		NVM description update
November 2015	G		Add 121, 256, 324csfBGA package qualification results.
April 2017	H		Add XO3L/XO3LF – 9400HC/HE silicon qualification results and 484-caBGA/256-csfBGA package qualification results
March 2018	I		Add XO3L-9400HC/HE High Thermal Die-Attach package qualification and ATT ATT5 to ATT1 transfer
June 2019	J		Correct typo in Table 4.2.1 and 4.4.1, update text in Section 4.4

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