Timer/Counter IP Core – Lattice Propel Builder

User Guide

FPGA-IPUG-02139-1.0

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Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
CPU	Central Processing Unit
FPGA	Field Programmable Gate Arrays
LINTR	Lattice Interrupt Interface

1. Introduction

The Lattice Semiconductor Timer/Counter IP is used to track timeouts in the system. It generates an interrupt to the CPU when a timeout is detected.

The Timer/Counter IP design is implemented in Verilog. It can be configured and generated using Lattice Propel™ Builder. It is targeted for all devices and implemented using the Lattice Radiant™ and Lattice Diamond® software Place and Route tool integrated with the Synplify Pro® synthesis tool.

1.1. Features

The Timer/Counter IP includes the following features:

- Generates up to eight timers/counters that operate individually
- Operates in either one-shot and continuous mode
- Counts up or down
- Register configuration through AMBA 3 APB Protocol v1.0
- Interrupt handling conforming to Lattice Interrupt Interface (LINTR) Standard
- User-configurable preload and prescaler value access modes
- User-configurable start and stop controls for software-controlled start and stop

1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.2.2. Signal Names

Signal names that end with:

- *_n* are active low (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals
- *_io* are bi-directional input/output signals

1.2.3. Host

The logic unit inside the FPGA interacts with the Timer/Counter IP through APB.

1.2.4. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

2.1. Overview

The Timer/Counter IP core can generate up to eight timers configured to operate individually.

It consists of a prescaler block that counts the clock source and provides outputs of divided by 2, 4, 8, and so on. This is used to slow down the counting rate of the timer.

The timer block is configurable through APB register access. Refer to the Register Description and Modes of Operation sections for configuration details.

The Timer/Counter IP core also generates an interrupt whenever timers reaches a timeout.

2.2. Block Diagram

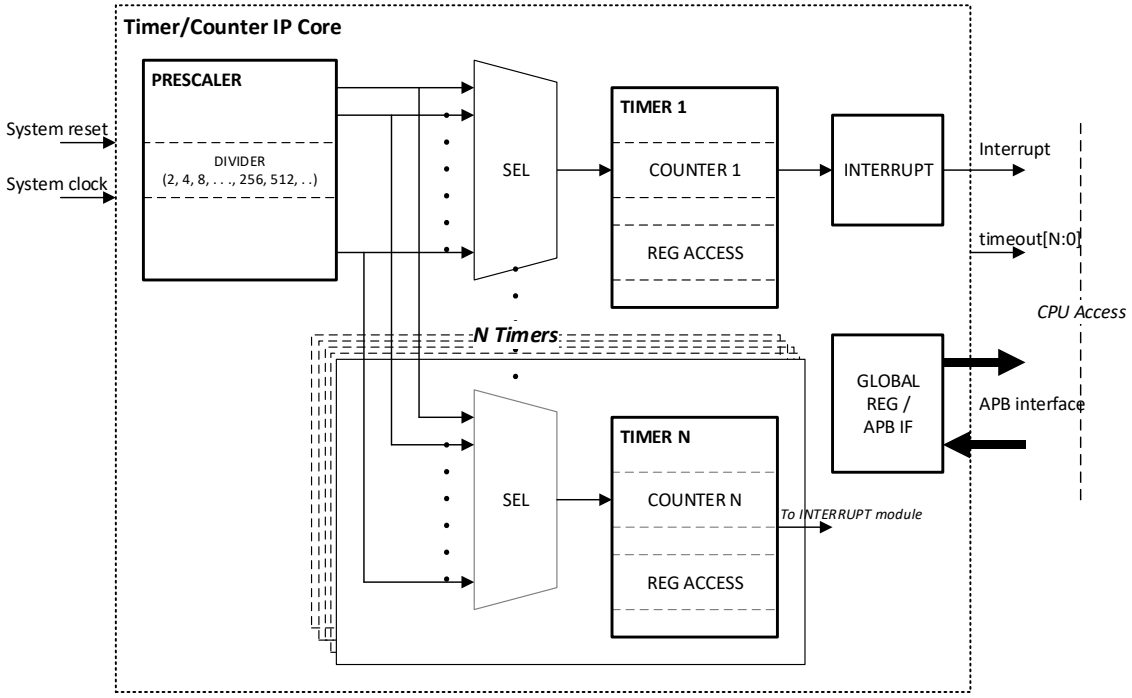

Figure 2.1. Timer/Counter IP Core Block Diagram

2.3. Signal Description

Table 2.1. Timer/Counter IP Core Signal Description

Port	Width	Direction	Description
System Clock and Reset			
clk_i	1	Input	Master clock input
rst_n_i	1	Input	Asynchronous reset active low
APB Slave Interface			
apb_psel_i	1	In	Select signal. Indicates that the slave device is selected and a data transfer is required.
apb_paddr_i	32	In	Address signal.
apb_pwdata_i	32	In	Write data signal.
apb_pwrite_i	1	In	Direction signal. Write = 1, Read = 0
apb_penable_i	1	In	Enable signal. Indicates the second and subsequent cycles of an APB transfer.
apb_pready_o	1	Out	Ready signal. Indicates transfer completion. Slave uses this signal to extend an APB transfer.
apb_prdata_o	32	Out	Read data signal.
Interrupt			
int_o	1	Output	Interrupt request
Others			
timeout_o	N-1	Output	Timeout output signal per N timer. Output a pulse whenever counter reaches timeout.

2.4. Attribute Summary

The Timer/Counter IP Core configurable attributes are as shown in Table 2.2 and are described in Table 2.3.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
No. of Timers	1 – 8	4	—
Prescaler Size	1 – 32	8	—
Timer N Settings (where N == *No. of Timers*)			
Direction	count-up, count-down	count-down	*No. of Timers == N*
Counter Size	1 – 32	2	*No. of Timers == N*
Timer Preloaded Value	0 – 2^(Counter Size)-1	4	*No. of Timers == N*
Disable Prescaler	enable, disable	enable	*No. of Timers == N*
Prescaler Ratio	1:2 – 1:2^(Prescaler Size)	1: 2147483648	*No. of Timers == N*
Software-controlled Retrigger	enable, disable	enable	*No. of Timers == N*
Timer Register Write Accessibility	enable, disable	enable	*No. of Timers == N, Software-controlled Retrigger == enable*

Table 2.3. Attribute Descriptions

Attribute	Description
General	
No. of Timers	Sets the default value of tmr_en field of GBL_CTRL register.
Prescaler Size	Sets the Prescaler counter width. The width determines the maximum divider or prescaler ratio.
Timer N Settings (where N == *No. of Timers*)	
Direction	Set the default value for dir field of CONTROL register.
Counter Size	Sets the internal counter width of the timer. The width determines the maximum time range.
Timer Preloaded Value	This is the initial value of the timer's internal counter. This also sets the default value for load_val of PERIOD register. The input value should be in the range that can be represented by the Counter Size.
Disable Prescaler	Sets the default value pscaler_dis field of CONTROL register.
Prescaler Ratio	Sets the default value of pscaler_ratio field of CONTROL register. See section 2.7.4 for details.
Software-controlled Retrigger	When enabled, the start and stop bits of CONTROL register are controllable through APB access.
Timer Register Write Accessibility	When enabled, the PERIOD Register is writable through APB access.

2.5. Register Description

Global registers are mapped to offsets 0x000-0x004, and per-timer registers are mapped to 0xN0-0xN0C, where N corresponds to the timer number, in the range 1 to *No. of Timers*.

Table 2.4. Summary of Timer/Counter IP Core Registers

Offset	Register Name	Access	Description
0x00	INT_STATUS*	RW1C	Interrupt Status Register
0x04	INT_ENABLE1	RW	Interrupt Enable Register
0x08	INT_SET*	WO	Interrupt Set Register
0x0C	GLB_CTRL	RW	Global Control Registers
0xN0	STATUS	RO	Timer N Status Register
0xN4	CONTROL	RW/RZ	Timer N Control Register
0xN8	PERIOD	RW	Timer N Period Register
0xNC	SNAPSHOT	RW	Timer N Snapshot Register

***Note**: Please see Lattice Hard IP Interface Standard, Chapter 3 for details of these registers.

The behavior of registers to write and read access is defined by its access type, as shown in Table 2.5.

Table 2.5. Access Type Definition

Access Type	Behavior on Read Access	Behavior on Write Access
RO	Returns register value	Ignores write access
WO	Returns 0	Updates register value
RW	Returns register value	Updates register value
RW1C	Returns register value	Writing 1’b1 on register bit clears the bit to 1’b0. Writing 1’b0 on register bit is ignored.
RZ	Returns 0	Writing 1’b1 on register returns to 0 on the next clock cycle.
RSVD	Returns 0	Ignores write access

2.5.1. INT_STATUS

This register represents the source of interrupts.

Name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INT_STATUS	RSVD															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSVD								to8_int	to7_int	to6_int	to5_int	to4_int	to3_int	to2_int	to1_int

Count-down mode – When the internal counter of timer 1 reaches zero, the interrupt bit is set to 1.

Count-up mode – When internal counter of timer 1 overflows, the interrupt bit is set to 1.

Table 2.6. Interrupt Status Register

Field	Name	Description
[0]	to1_int	Timer 1 Timeout Interrupt
[1]	to2_int*	Timer 2 Timeout Interrupt
[2]	to3_int*	Timer 3 Timeout Interrupt
[3]	to4_int*	Timer 4 Timeout Interrupt
[4]	to5_int*	Timer 5 Timeout Interrupt
[5]	to6_int*	Timer 6 Timeout Interrupt
[6]	to7_int*	Timer 7 Timeout Interrupt
[7]	to8_int*	Timer 8 Timeout Interrupt
[31:8]	RSVD	Reserved bits

***Note:** This bit is valid when *No. of Timers* > 1.

2.5.2. INT_ENABLE

This register controls whether the interrupts in the INT_STATUS register assert the int_o signal or not.

Name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INT_ENABLE	RSVD															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSVD								to8_en	to7_en	to6_en	to5_en	to4_en	to3_en	to2_en	to1_en

Table 2.7. Interrupt Enable Register

Field	Name	Description
[0]	to1_en	Timer 1 Timeout Interrupt enable
[1]	to2_en*	Timer 2 Timeout Interrupt enable
[2]	to3_en*	Timer 3 Timeout Interrupt enable
[3]	to4_en*	Timer 4 Timeout Interrupt enable
[4]	to5_en*	Timer 5 Timeout Interrupt enable
[5]	to6_en*	Timer 6 Timeout Interrupt enable
[6]	to7_en*	Timer 7 Timeout Interrupt enable
[7]	to8_en*	Timer 8 Timeout Interrupt enable
[31:8]	RSVD	Reserved bits

***Note:** This bit is valid when *No. of Timers* > 1. Writing to this register does not affect anything.

2.5.3. INT_SET

This register sets the interrupts in the INT_STATUS register.

Name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INT_SET	RSVD															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSVD								to8_set	to7_set	to6_set	to5_set	to4_set	to3_set	to2_set	to1_set

Table 2.8. Interrupt Set Register

Field	Name	Description	Access	Default
[0]	to1_set	Timer 1 Timeout Interrupt set	RW	0
[1]	to2_set*	Timer 2 Timeout Interrupt set	RW	0
[2]	to3_set*	Timer 3 Timeout Interrupt set	RW	0
[3]	to4_set*	Timer 4 Timeout Interrupt set	RW	0
[4]	to5_set*	Timer 5 Timeout Interrupt set	RW	0
[5]	to6_set*	Timer 6 Timeout Interrupt set	RW	0
[6]	to7_set*	Timer 7 Timeout Interrupt set	RW	0
[7]	to8_set*	Timer 8 Timeout Interrupt set	RW	0
[31:8]	RSVD	Reserved bits	RO	0

***Note:** This bit is valid when *No. of Timers* > 1. Writing to this register does not affect anything.

2.5.4. GBL_CTRL

Global register settings of the Timer/Counter IP Core.

Name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GBL_CTRL	RSVD															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSVD								tmr_en							

Table 2.9. Global Register

Field	Name	Description	Access	Default
[7:0]	tmr_en	Enable or disables timer. Each bit represents each timer. Bits can be set simultaneously. [0] – Enable timer 1 when set to 1 [1] – Enable timer 2 when set to 1 [2] – Enable timer 3 when set to 1 [3] – Enable timer 4 when set to 1 [4] – Enable timer 5 when set to 1 [5] – Enable timer 6 when set to 1 [6] – Enable timer 7 when set to 1 [7] – Enable timer 8 when set to 1	RW	*No. of Timers*
[31:8]	RSVD	Reserved bits	RO	0

2.5.5. STATUS

This is the status register for timer *N*.

Name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STATUS	RSVD															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSVD															tmr_run

Table 2.10. Status Register

Field	Name	Description	Access	Default
[0]	tmr_run	When internal counter is running, this bit is read as 1. When internal counter is not running, it is read as 0.	RO	0
[31:1]	RSVD	Reserved bits	RO	0

2.5.6. CONTROL

This register controls the mode of operation, direction, counter sizes, and retriggerable ability of each timer.

Name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CONTROL	RSVD															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	pscaler_ratio								RSVD			pscaler_dis	stop	start	dir	cont

Table 2.11. Control Register

Field	Name	Description	Access	Default
[0]	cont	Counter mode of operation. This bit determines how the internal counter behaves when it reaches timeout. Set to 1 – Continuous: the counter keeps running until it is stopped by the stop bit. Set to 0 – One-shot: the counter stops when it reaches timeout. When the counter reaches timeout, it reloads with the value stored in PERIOD register, regardless of the setting of this bit. When attribute Software-controlled Retrigger == disable, the timer keeps running and is not affected by the value of this bit.	RW	1
[1]	dir	Direction of counter. Set to 0 – count-down. The internal counter decrements from preloaded value. Set to 1 – count-up. The internal counter increments from preloaded value to maximum counter.	RW	0
[2]	start[1]	Start the counter. Set to 1 – causes the internal counter to begin counting down or up. If the timer is stopped before reaching to zero or maximum, writing 1 to this bit causes the timer to continue counting from the number currently held in its counter. If the timer is already running, writing any value to this bit have no effect.	RZ	0

Field	Name	Description	Access	Default
[3]	stop[1]	Stop the counter. Set to 1 – causes the internal counter to stop counting. This bit has no effect when: the timer has already stopped a '0' is written to this bit the attribute *Software-controlled Retrigger == disable*	RZ	0
[4]	pscaler_dis	Disables prescaler selection. It uses 1:1 ratio of the system clock frequency.	RW	Disable Prescaler
[7:5]	RSVD	Reserved	RO	0
[15:8]	pscaler_ratio	Prescaler ratio or the divide ratio. See section 2.7.4 for details. When pscaler_dis = 0, timer is not affected by this register.	RW	Prescaler Ratio
[31:16]	RSVD	Reserved	RO	0

***Note**: When a 1 is written to both start and stop bits simultaneously, the priority is the stop bit.

2.5.7. PERIOD

Name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PERIOD	load_val															
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	load_val															

Table 2.12. Period Register

Field	Name	Description	Access	Default
[31:0]	load_val	The internal counter is loaded with the value stored in this register. When attribute *Software-controlled Retrigger == enable*, writing on this register updates the internal counter, and the count-down or count-up continues. When attribute *Software-controlled Retrigger == disable*, writing on this register does not affect the internal counter. When attribute *Timer Register Write Accessibility == disable*, writing on this register causes the counter to reset to the fixed value specified in the attribute *Timer Preloaded Value*.	RW	*Timer Preloaded Value*

2.5.8. SNAPSHOT

Name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SNAPSHOT	snap_val															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	snap_val															

Table 2.13. Snapshot Register

Field	Name	Description	Access	Default
[31:0]	snap_val	Specifies the snapshot value of the internal counter	RO	0

2.6. Modes of Operation

2.6.1. Software-controlled Retrigger enabled

When attribute *Software-controlled Retrigger == enable,* timer is configurable/controllable through register access.

2.6.2. Software-controlled Retrigger disabled

When attribute *Software-controlled Retrigger == disable*, the behavior of the timer is always in continuous mode and is not affected by the settings in the CONTROL register. When it reaches the timeout event, it reloads to the value set in the attribute *Timer Preloaded Value*.

Issuing a write access to the PERIOD register causes the counter to restart to the value set in the *Timer Preloaded Value* attribute, regardless of the *Timer Register Write Accessibility* setting.

2.6.3. Timeout and Interrupt

When attribute *Direction == count-down,* a timeout event occurs when counter reaches 0x0.

When attribute *Direction == count-up,* a timeout event occurs when counter reaches the maximum count.

Whenever a timeout event occurs, the interrupt status registers (INT_STAT) mapped to the timeout signal asserts.

2.6.4. Prescaler

Table 2.14 shows the prescaler ratio with its corresponding pscaler_ratio register setting. The prescaler counter size is configurable up to 32 bits for wide time range selection.

Table 2.14. Prescaler Ratio Table

Prescaler Counter Bit	Prescaler Ratio	pscaler_ratio[7:0]							
[0]	1:2	0	0	0	0	0	0	0	0
[1]	1:4	0	0	0	0	0	0	0	1
[2]	1:8	0	0	0	0	0	0	1	0
[3]	1:16	0	0	0	0	0	0	1	1
[4]	1:32	0	0	0	0	0	1	0	0
[5]	1:64	0	0	0	0	0	1	0	1
[6]	1:128	0	0	0	0	0	1	1	0
[7]	1:256	0	0	0	0	0	1	1	1
[8]	1:512	0	0	0	0	1	0	0	0
[9]	1:1024	0	0	0	0	1	0	0	1
[10]	1:2048	0	0	0	0	1	0	1	0
[11]	1:4096	0	0	0	0	1	0	1	1
[12]	1:8192	0	0	0	0	1	1	0	0
[13]	1:16384	0	0	0	0	1	1	0	1
[14]	1:32768	0	0	0	0	1	1	1	0
[15]	1:65536	0	0	0	0	1	1	1	1
[16]	1:131072	0	0	0	1	0	0	0	0
[17]	1:262144	0	0	0	1	0	0	0	1
[18]	1:524288	0	0	0	1	0	0	1	0
[19]	1:1048576	0	0	0	1	0	0	1	1
[20]	1:2097152	0	0	0	1	0	1	0	0
[21]	1:4194304	0	0	0	1	0	1	0	1
[22]	1:8388608	0	0	0	1	0	1	1	0
[23]	1:16777216	0	0	0	1	0	1	1	1
[24]	1:33554432	0	0	0	1	1	0	0	0
[25]	1:67108864	0	0	0	1	1	0	0	1
[26]	1:134217728	0	0	0	1	1	0	1	0
[27]	1:268435456	0	0	0	1	1	0	1	1
[28]	1:536870912	0	0	0	1	1	1	0	0
[29]	1:1073741824	0	0	0	1	1	1	0	1
[30]	1:2147483648	0	0	0	1	1	1	1	0
[31]	1:4294967296	0	0	0	1	1	1	1	1

2.7. Sample configuration

Sample use case:

If you choose a *Prescaler Ratio* of 1:512 with a system clock frequency of 50 MHz (20 ns),

1 count (a tick) of the internal counter of the timer is:

$$20\ ns\ x\ 512 = \mathbf{10.24\ us}$$

If the *Counter Size* is set to 16 bits, maximum period is:

$$16 - bit\ counter\ x\ 10.24\ us = \mathbf{671\ ms}$$

Appendix A. Resource Utilization

Table A.1. Resource Utilization

No. of Timer	Registers	LUTs	EBRs	Target Device	Synthesis Tools
4	462	754	0	CrossLink™-NX Certus™-NX	Synopsys® Synplify Pro N-2018.03L-SP1-1

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, November 2021

Section	Change Summary
All	Initial release.

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