UART Model VIP - Lattice Propel Builder

User Guide

FPGA-IPUG-02146-1.0

October 2020

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
LUT	Lookup-Table
UART	Universal Asynchronous Receiver/Transmitter
VIP	Verification Intellectual Property

1. Introduction

The Lattice Semiconductor UART Model VIP (Verification IP) is used for verification purposes only. It is a UART model that is able to receive as well as transmit serial data.

The UART Model VIP design is implemented in System Verilog. It can be configured and generated using the Lattice Propel™ Builder software. It is for simulation only and is not targeted to any device.

1.1. Features

The UART Model has the following features:

- Configurable bit rate
- Configurable payload bits
- UART receiver
- UART transmitter

1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on System Verilog.

2. Functional Descriptions

2.1. Overview

The UART Model VIP is used to handle UART transactions for the verification environment as shown in Figure 2.1. The ports with *_debug* suffix are for debug only and can be configured to be present or not present.

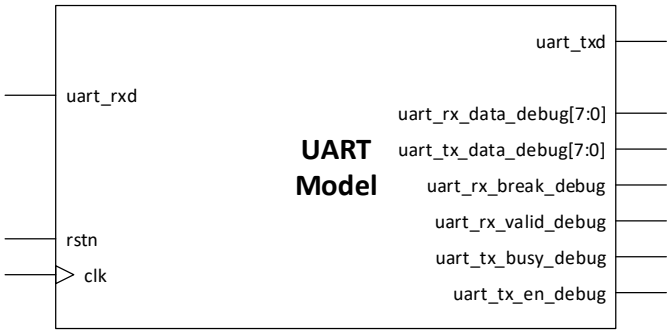

Figure 2.1. UART Model VIP Block Diagram

2.2. Signal Description

Table 2.1 lists the ports of the UART Model VIP.

Table 2.1. UART Model Ports

Name	Type	Width	Description
clk	in	1	Clock input
rst_n	in	1	Reset input, active low
uart_rxd	in	1	UART receive port
uart_txd	out	1	UART transmit port
uart_rx_data_debug	out	8	Receiver input data, for debug only
uart_rx_break_debug	out	1	Receiver data broken (all received data bits are 0), for debug only
uart_rx_valid_debug	out	1	Receiver data valid, for debug only
uart_tx_data_debug	out	8	Transmitter output data, for debug only
uart_tx_busy_debug	out	1	Transmitter busy sending data, for debug only
uart_tx_en_debug	out	1	Transmitter enable, for debug only

2.3. Attribute Summary

The configurable attributes of the UART Model VIP are shown in Table 2.2 and are described in Table 2.3.
The attributes can be configured through the Propel Builder software.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
CLK_MHZ	Int	50	—
BIT_RATE	115200, 9600	115200	—
PAYLOAD_BITS	7, 8	8	—
STIMULUS_GEN	0, 1	0	—
STACK_DEPTH	Int	128	Enabled when STIMULUS_GEN = 1
STIMULUS_FILE_NAME	Path string	—	Enabled when STIMULUS_GEN = 1
DEBUG_PINS_EN	Bool	False	—

Table 2.3. Attributes Description

Attribute	Description
CLK_MHZ	Input clock frequency
BIT_RATE	UART bit rate
PAYLOAD_BITS	UART payload bits
STIMULUS_GEN	Sending of UART data from designated file at the beginning of simulation 0 – do not send, 1 – send.
STACK_DEPTH	Depth of the buffer used to contain the transmitter data from the file. The length of each buffer item equals to PAYLOAD_BITS.
STIMULUS_FILE_NAME	Path of the file containing the transmitter data
DEBUG_PINS_EN	Enabling of debug pins 0 – disable, 1 – enable.

3. UART Model VIP Generation

This section provides information on how to generate the UART Model VIP module using Propel Builder.

To generate the UART Model VIP module:

1. In Propel Builder, create a new verification design, and select the UART Model VIP package.
2. Enter the module name and click **Next** as shown in Figure 3.1.

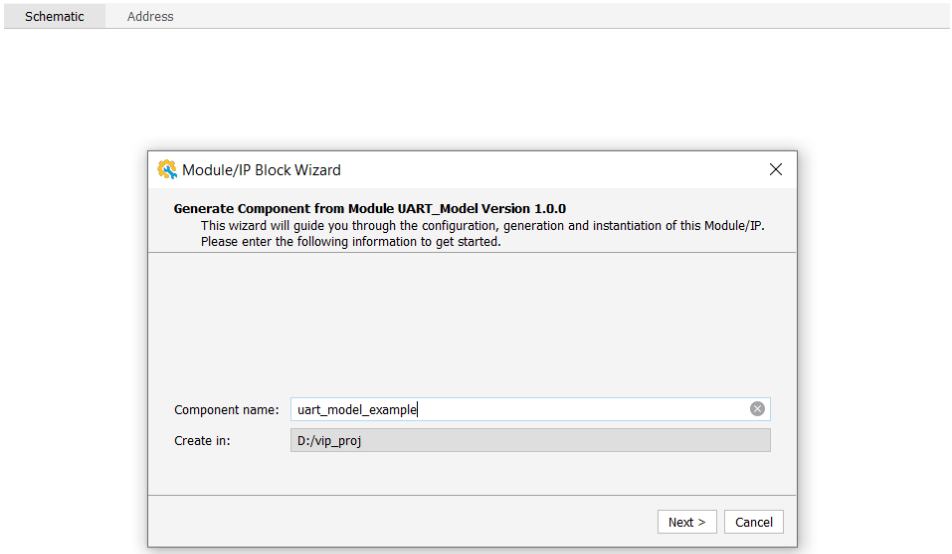

Figure 3.1. Entering the Module Name

3. Configure the parameters as needed, then click **Generate**.

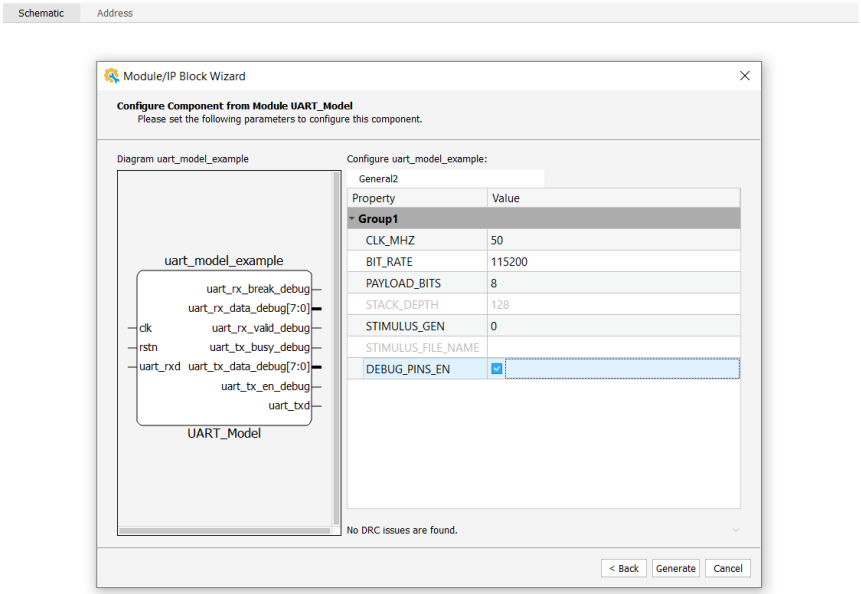

Figure 3.2. Configuring the Parameters

4. Verify the information and click **Finish**.

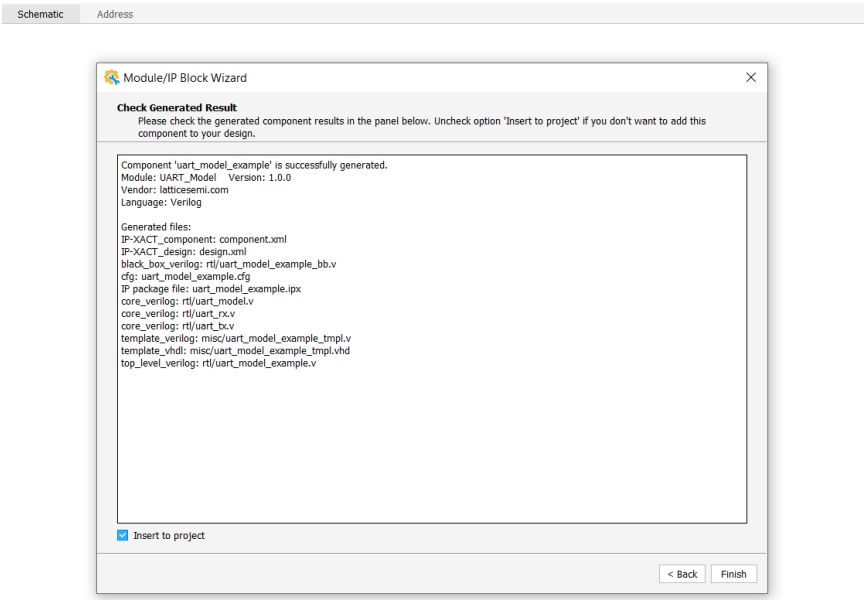

Figure 3.3. Verifying the Result

5. Confirm or modify the module instance name, then click **OK**.

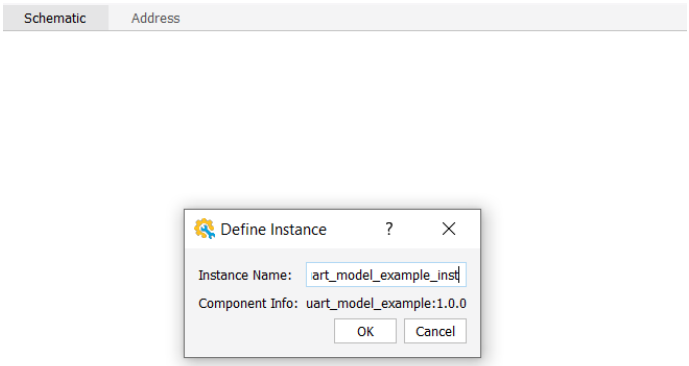

Figure 3.4. Specifying the Instance Name

The UART Model VIP instance is successfully generated.

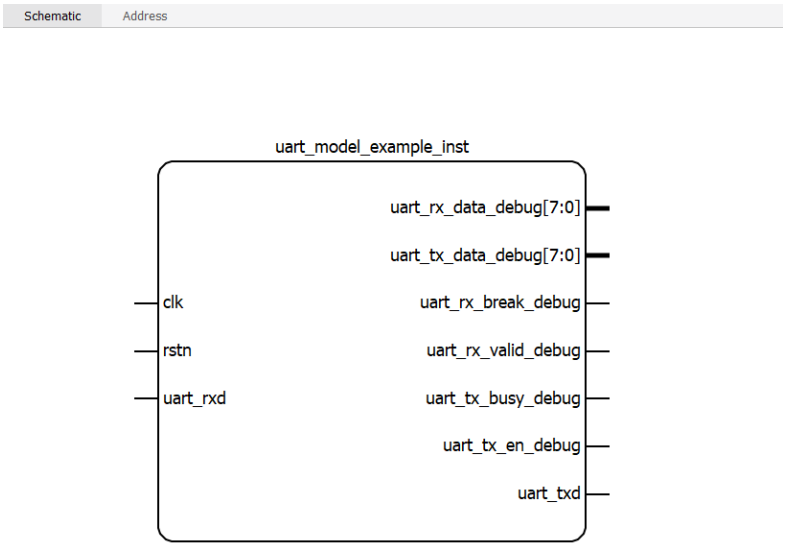

Figure 3.5. Generated Instance

References

- MachXO3D FPGA web page in latticesemi.com
- CrossLink-NX FPGA web page in latticesemi.com
- Lattice Propel 1.0 User Guide
- Lattice Diamond Software 3.11 User Guide
- Lattice Radiant® Software 2.1 User Guide

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, October 2020

Section	Change Summary
All	Initial release.

www.latticesemi.com