



March 19, 2018

Subject: PCN#02A-18 Notification of Changes to the CrossLink™ Data Sheet

Dear Lattice Customer,

Lattice Semiconductor is providing this notification of changes to the CrossLink™ Data Sheet.

Change Description

The new CrossLink™ Family Data Sheet (FPGA-DS-02007 Version 1.4 dated February 2018) includes adjustments to the two parameters listed:

Generic SDR Interfaces - General Purpose I/O Pin Parameters Using Clock Tree Without PLL					
Parameter	Description	DS Version 1.3		DS Version 1.4	
		Min	Max	Min	Max
t _{SU_DELAY}	Clock to Data Setup – PIO Input Register with Input Delay for zero t _{HD}	1.02 ns	---	1.25 ns	---

Generic SDR Interfaces - General Purpose I/O Pin Parameters Using Clock Tree With PLL					
Parameter	Description	DS Version 1.3		DS Version 1.4	
		Min	Max	Min	Max
t _{SU}	Clock to Data Setup – PIO Input	0.17 ns	---	0.20 ns	---

See the data sheet revision history for other clarifications and changes.

There is no change to any device bitstream design. There will be a change to the Diamond™ 3.10SP2 software which is scheduled to be released on March 29, 2018.

Affected Products

The Ordering Part Numbers (OPNs) affected by this PCN are as follows:

- LIF-MD6000-6UWG361TR
- LIF-MD6000-6UMG64I
- LIF-MD6000-6MG81I
- LIF-MD6000-6JMG80I
- LIF-MD6000-6KMG80I

Note: This PCN also affects all package, grade and tape/reel options and any custom devices (i.e. factory programmed, special test, etc.) which are derived from any of the devices listed above.

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Datasheet Specifications

The updated CrossLink™ Family Data Sheet (FPGA-DS-02007 Version 1.4 dated February 2018) with the changes described above is available on the Lattice website.

Recommended Action

The timing changes apply to applications with inputs in Single Data Rate (SDR) mode. This includes a pad configured as a GPIO input and/or a design incorporating the SDR Soft IP.

Customers should confirm that the signals connected to the affected inputs still meet the updated setup and hold times relative to the signal sources. Customers should also recompile the project with Diamond™ 3.10SP2 software to ensure that the design still achieves timing closure during static analysis. As previously stated, there is no change to the design's bitstream and re-generation of the bitstream is not needed.

Customers who have further questions regarding this specification change are encouraged to contact local field support or sales@latticesemi.com.

PCN Timing

The datasheet changes are effective immediately and retroactively. There are no changes to the silicon and therefore samples are not applicable to these data sheet changes.

Sincerely,

Lattice PCN Administration