

MachXO 300mm Fab Transition Circuit Observations and Mitigation

Lattice is issuing this Product Bulletin to inform its customers of certain circuit observations and to supply possible mitigation strategies.

Background: Lattice issued PCN#05A-14 “**Notification of Intent to Utilize an Alternate Qualified Foundry and Alternate Qualified Mask Sets for the MachXO Products**” in 2014 and PCN#03A-15 “**Notification of Intent to utilize an Alternate Qualified Foundry and Alternate Qualified Mask Sets for the FPGA and Power Management sections of the Platform Manager products**” which declared Lattice’s intent to transition from Fujitsu’s 200 mm fab to their adjacent 300 mm fab in Mie, Japan. The transition has gone smoothly for the majority of our MachXO customers in the last two years. The vast majority of the customers have seen no change to the MachXO device’s form, fit or function. Similarly, customers who took advantage of the sample program for MachXO evaluation have reported fewer issues with the new material. Lattice has received no reports from Platform Manager customers related to the fab transition.

Observation: A small number of MachXO customers have been impacted by some characteristics of the Alternate Qualified Foundry and Mask Set MachXO product. The observed deviations are within the MachXO existing datasheet specifications and are well within the expected process variations. Nevertheless, the small deviations have adversely impacted some customer designs which 1) exceeded the datasheet output drive specifications, 2) were utilized in marginally designed circuit environments for a given output drive setting, or 3) utilized True-LVDS capable I/O in a ‘hot-socket’ condition.

Lattice is providing this document as a guide for mitigation as customers receive 300 mm material into their production pipelines.

Scenario #1: Lower Output Drive

In ‘overdrive’ conditions, the MachXO and Platform Manager FPGA I/O single ended LVCMOS output driver may not provide the same I_{OH} source output current and/or reach similar V_{OH} .

An ‘overdrive’ condition is defined as utilizing an output driver to source current in excess of its characterized rating. For example, an LVCMOS33 8 mA driver attempting to drive 3.3 V into a DC load of 220 ohms, which requires 15 mA to sustain $V_{OH}(\min)$, is in an ‘overdrive’ condition. LVCMOS33 16 mA is the appropriate drive strength and brings the application into datasheet compliance. Using the MachXO or Platform Manager FPGA output in an ‘overdrive’ condition

is not recommended. Choosing the appropriate drive strength substantially eliminates any future susceptibility to process variations.

In designs which exceed the drive specification by 2x or more, drive strength reductions of up to 22% can be observed. Designs which do not exceed the rated drive capability do not see any deviation from the datasheet specification.

Mitigation: For customers who have reported a reduced V_{OH} , increasing the output buffer drive strength has eliminated the issue for the vast majority of the cases. In rare applications with multiple outputs, care is required to increase drive appropriately while not exceeding the average DC current draw limits of the device. Note, it is necessary to re-build the MachXO JEDEC programming file using Lattice Diamond design software, or re-build the Platform Manager FPGA JEDEC file in either Diamond or PAC-Designer software, to modify the output drive strength.

Scenario #2: Signal Integrity

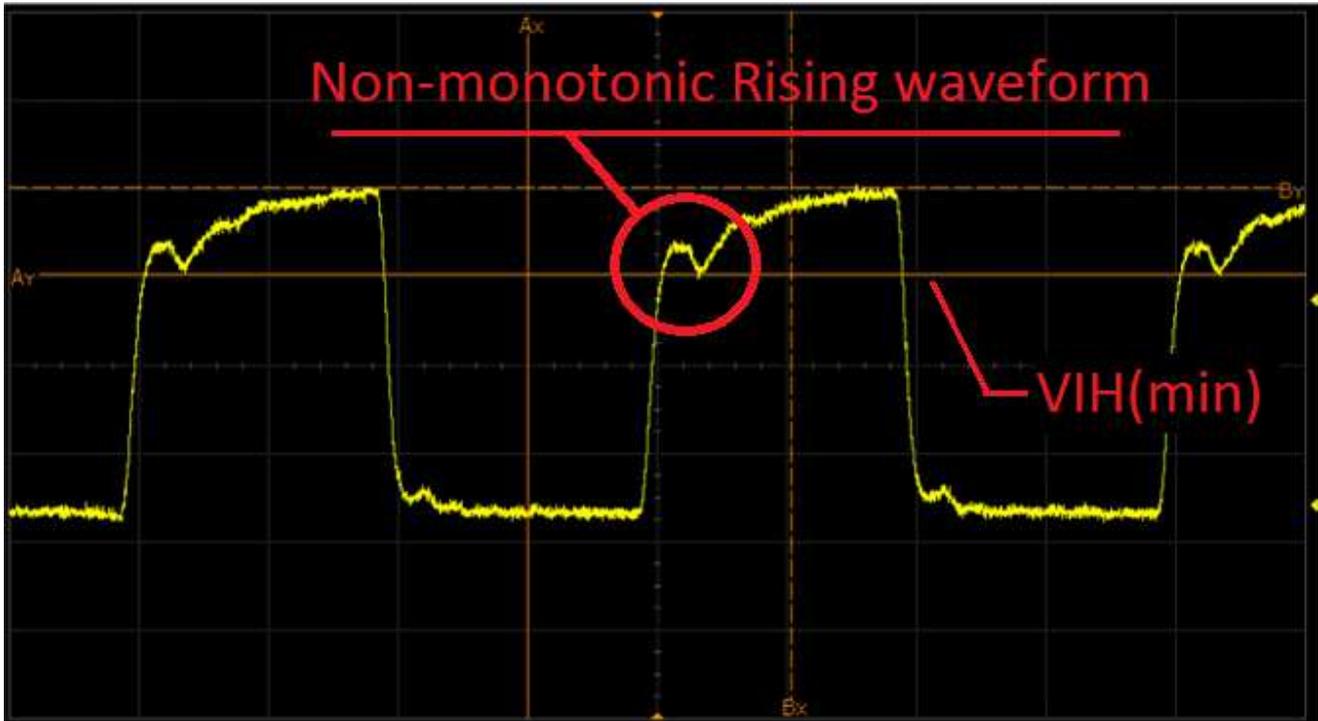
In 'marginal' circuits, transmission line effects (for example, non-monotonic rising edges, reflections and glitches) may adversely impact the output waveform. Unintentional signal transitions may migrate into the logic decision region of the downstream receiver.

A 'marginal' signal integrity condition is defined when the output signal contains a glitch or reflection resulting in non-monotonic rising edges which lay just outside the receiver's decision region bounded by $V_{IH(min)}$. See Figure 1 for an example of a marginal signal condition. Lattice supplies IBIS models for the MachXO and Platform Manager FPGA output drivers, enabling circuit designers to simulate their circuit environment prior to PCB design, or to verify actual signal behavior prior to volume production. Simulation enables the designer to choose the appropriate drive strength and termination scheme combination to eliminate 'marginal' conditions. Choosing the appropriate drive strength and termination substantially eliminates circuit susceptibility to process variations.

In designs with 'marginal' signal integrity, the use of Alternate Qualified Foundry and Mask Set MachXO or Platform Manager FPGA product can result in unacceptable increase in system failure rate. Most often, increasing the MachXO drive strength can compensate the circuit enough to move multiple signal transitions above the decision threshold $V_{IH(min)}$.

Mitigation: For customers who have reported increased system failure rates due to non-monotonic edges, simply increasing the output buffer drive strength has eliminated the issue in some cases. In other cases it was necessary to use IBIS modeling to tune the external circuit in conjunction with increasing drive strength. Note, it is necessary to re-build the MachXO JEDEC programming file using Lattice Diamond design software, or re-build the Platform Manager FPGA JEDEC file in either Diamond or PAC-Designer software, to modify the output drive strength.

Figure 1: Marginal Signal Condition



Scenario #3: Hot-Socket behavior for True-LVDS capable I/O

In ‘marginal’ circuits utilizing the True-LVDS capable I/O in the MachXO product, the True-LVDS capable buffer may sink increased leakage current (I_{DK_LVDS}), adversely impacting critical signals during ‘hot-socket’ conditions.

Roughly 50% of GPIO in banks 2, 3, 6 and 7 in MachXO 1200 LUT and 2280 LUT devices are True-LVDS capable. (MachXO-256, MachXO-640, and Platform Manager products do not support True-LVDS I/O and are not impacted.) A robust MachXO design takes into account the higher ‘hot-socket’ leakage current (I_{DK_LVDS}) possible in True-LVDS capable I/O, even when not used as an LVDS-type interface. A ‘marginal’ circuit is defined as one not designed to withstand or tolerate the typical 35mA I_{DK_LVDS} as specified in the [MachXO Data Sheet DS1002](#) Hot Socketing Specifications. A ‘hot-socket’ condition is defined where the GPIO pad voltage V_{in} is greater than the corresponding V_{ccio} bank voltage ($V_{in} > V_{ccio}$). ‘Hot-socket’ conditions can typically be found in systems with sequenced power-supplies, or when device inputs are energized (e.g. over backplanes or cables) before FPGA power is applied, or when device inputs remain energized after FPGA power is removed.

An example ‘marginal’ circuit would include a reliance on an external pull-up or series resistor to hold a valid ‘high’ signal level when the MachXO bank V_{ccio} is unpowered. Most practical

pull-up resistors are not sized to withstand a typical 35mA leakage sink into the MachXO GPIO buffer, while a series resistor may create an excessive voltage drop.

In customer applications with 'marginal' circuits not designed to withstand or tolerate typical 35mA I_{DK_LVDS} , the use of Alternate Qualified Foundry and Mask Set MachXO FPGA product can result in an unacceptable increase in the system failure rate. The failure rate may increase with temperature.

Mitigation: There are multiple system-level approaches to mitigation.

- Modify power-supply sequencing to ensure early or simultaneous powering of the MachXO Vccio banks with respect to critical signal energization.
- Re-work or re-layout the printed circuit board to re-assign critical signals (e.g. reset signals, clock signals, power supply enables, etc.) to non-True-LVDS capable pins.
- Increase pull-up resistor strength if the signal driver is capable of sinking high-current.
- Contact Lattice Sales and Marketing for up-to-date production options.

Note, it is necessary to re-build the MachXO JEDEC programming file using Lattice Diamond design software in the Diamond software if pin-assignments change due to PCB modification.

Customers are advised to utilize the above mitigation strategies to prevent possibility of field failures or performance marginality.

CONTACT

If you have any questions or require additional information, please contact www.latticesemi.com/techsupport

Sincerely,

Lattice Semiconductor MachXO Product Line Management

Revision History

Date	Version	Description of Revisions
14-Sep-2016	1.0	Initial Release
16-Sep-2016	1.1	Updated Tech Support Contact
12-Oct-2016	1.2	Added Platform Manager information
12-Jun-2017	2.0	Added 'Hot-Socket' application information