

Sensor Management via MIPI SLIMbus

Integrated SLIMbus Solution Using the iCE40 Ultra-Low Density FPGA

MIPI SLIMbus Overview

The Serial Low-power Inter-chip Media Bus (SLIMbus™) is a standard interface between a baseband or application processor and peripheral components in mobile terminals. It was developed within the MIPI Alliance. The interface supports many digital audio components simultaneously, and carries multiple digital audio data streams at differing sample rates and bit widths.

SLIMbus is implemented as a synchronous 2-wire, configurable Time Division Multiplexed (TDM) frame structure. It has supporting bus arbitration mechanisms and message structures which permit reconfiguration of the bus operational characteristics to system application needs at runtime. Physically, the data line (DATA) and the clock link (CLK) interconnect multiple SLIMbus components in a multi-drop bus topology. Figure 1 shows a conceptual view of a possible real world SLIMbus system.

SLIMbus Technical Detail

There are two signals:

- · Clock Any frequency, can have multiple drivers
- Data NRZI Transition = 1, no transition = 0, packetized serial bus, multi-drop

Device Classes:

- Manager Device Bus configuration and administration, can be more than one
- Framer device Delivers clock. Also transmits Frame Sync and Framing Information channels.
- Interface Device Provides bus management services for each component
- · Generic Provides application functionality

Clock

- Root frequency = <28MHz
- Gear Frequency multiplier by factor of 2, gears 0-10
- · Clock can be changed, stopped and re-started

Cells, Slots, Subframes, Frames, Superframes

- Cell Data bit bounded by two consecutive positive clock edges
- Slot 4 contiguous cells (MSB LSB)
- Frame 192 contiguous slots (S0 S191)
- · S0 Control Space 4 sync bits
- · S96 Control Space 4 framing bits
- Subframe 6, 8, 24, 32 contiguous slots
- S0 always control space (could be S0 or S96 of frame)
- · Slots not control space are data space
- Superframe 8 contiguous frames.
- Duration fixed in slots but not in time since clock can be changed

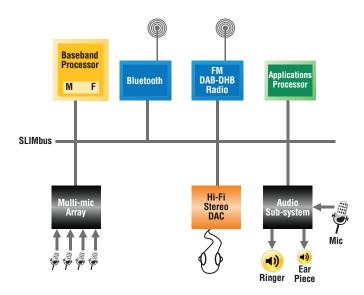


Figure 1: Conceptual SLIMbus System

Designer's Challenge

Sensors are changing the landscape of today's smartphones. Various sensor types are now showing the potential to alter user input methods, user interfaces, and to enable new genres of use cases for mobile handsets. Sensors not only enhance the user interface to smartphones but are also used to monitor environmental conditions such as battery, temperature, and ambient light. In fact, today's high-end smartphones can contain anywhere from 15 to 20 different sensors.

Typically, sensors are available with an I²C interface and a mobile processor usually comes with two to three I²C masters. Some sensors are sensitive to performance and need dedicated one-to-one connection to the processor, which creates an I²C shortage in the processor. Ideally, it can connect sensors through other expansion ports such as a memory bus via a bridging device. However, with the popularity of Package-on-Package (PoP), memory is no longer available for the bridging device to attach onto. While a SPI port is another alternative, it is usually used for digital TV and WLAN which needs a dedicated one-to-one connection.



Lattice SLIMbus Solution

SLIMbus is a good alternative for sensor management. SLIMbus IP is implemented in the iCE40™ FPGA with multiple I²C masters for sensor management. The SLIMbus IP is compliant with the SLIMbus specification version 1.01.01. It is designed for a data rate of up to 28.8Mbps and it is capable of supporting multiple I²C devices and GPIO port expansion (see Figure 2). With the flexible iCE40 FPGA architecture, a number of I²C and GPIO ports can be customized to better fit a designer's needs. With more processors adopting SLIMbus in their latest architectures, such as the Marvell Armada and TI OMAP4/OMAP5 processors, SLIMbus is a better choice moving forward.

Features

- Up to 4x I²C masters
- GPIO (1 x 4bit) interface
- Multiple SLIMbus function ports can drive multiple I²C masters
- I²C compliant masters supporting 100KHz and 400KHz (fast mode) operations
- · Separate SLIMbus function port for GPIO
- Asynchronous protocol, expandable to others (such as Isochronous, Asynchronous Push and Pull)
- I²C slave interrupts transferred to SLIMbus messages
- 28.8 Mbps throughput

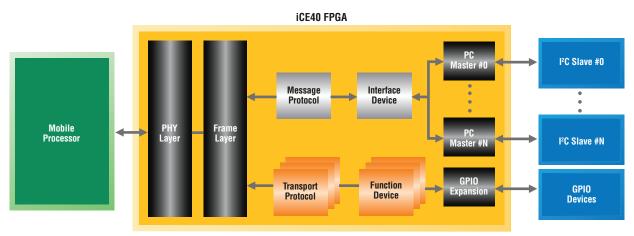


Figure 2: Lattice SLIMbus to I²C Expander Block Diagram.

Lattice offers design services for qualified accounts for modifying designs or adding additional functionality within the iCE40 FPGA. Please contact your Lattice local sales representative for more information.

Applications Support

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