

# Platform Manager™ 2

## Scalable Hardware Management Controller

Platform Manager 2 devices feature programmable analog with FPGA on a single chip to integrate all hardware management (power, thermal and control plane management) functions in a circuit board. The Platform Manager 2 architecture uses centrally located hardware management algorithm within the FPGA to control distributed hardware management expanders (L-ASC10 ICs) to integrate power, thermal and control plane management functions cost effectively from simple to complex boards

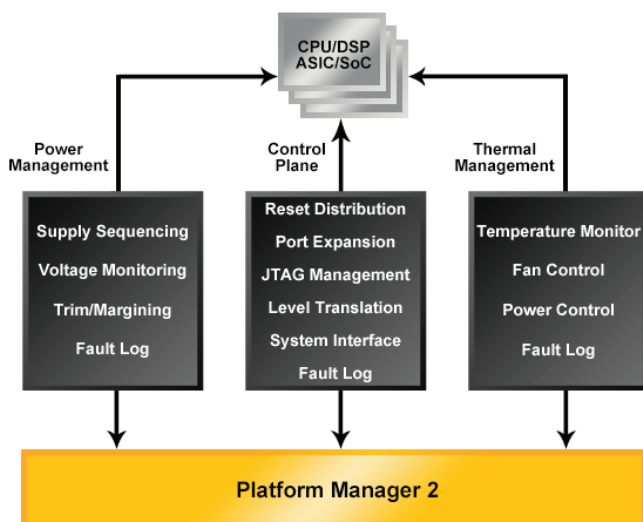
The Platform Designer™ tool integrated in Lattice Diamond® software provides a single design environment to integrate a circuit board's hardware management using LogiBuilder (GUI-based logic entry), Verilog or VHDL. The correct-by-construction (automatic selection, customization and wiring of IPs for a given design) design methodology enables seamless scaling of analog channels, Digital I/Os and FPGA LUTs to optimally meet specific hardware management requirements of a given board.

Power management functions include monitoring, supply sequencing, fault log, voltage scaling/VID control, trimming and margining functions. Thermal management includes temperature monitoring, fan speed control, power control and fault log. The control plane management includes reset distribution, I<sup>2</sup>C/SPI port expansion, level translation, system interface, fault logging, and other glue logic.

Increases Reliability	<ul style="list-style-type: none"> <li>• Ample monitoring resources for full fault coverage</li> <li>• Accurate (0.2%) and fast (&lt;100us) Fault detection on any channel</li> <li>• Minimized fault propagation through abundant communication between hardware management sub-blocks</li> <li>• Integrated power, thermal, control plane management algorithm in a single device</li> </ul>
Reduces Time to Market	<ul style="list-style-type: none"> <li>• Single design environment covers wide range of design complexities reducing design time</li> <li>• Fully verified hardware management through end-to-end simulation</li> <li>• Reduced design effort through correct-by-construction design methodology</li> <li>• Distributed sense and centralized control methodology minimizes circuit board layout congestion</li> <li>• Fault log, software based regression test support reduces board debug time</li> </ul>
Lowers BOM and Cost	<ul style="list-style-type: none"> <li>• Reduce BOM cost up to 50% versus multiple ICs</li> <li>• Needs fewer number of I/Os in a CPLD</li> <li>• Reduced board area and layers saves additional cost</li> </ul>
Reduces Risk	<ul style="list-style-type: none"> <li>• Simulation reduces design errors before board layout</li> <li>• Re-programmability minimizes risk of board re-spins</li> <li>• Significantly reduces time-to-market</li> </ul>

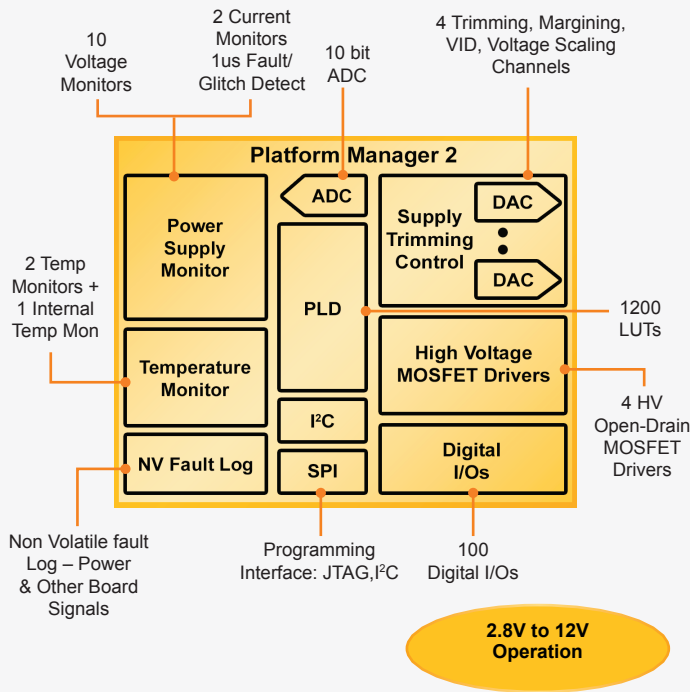
### Key Features and Benefits

- Optimized Hardware Management through Scalability**
  - 10 to 80 precision voltage monitor channels
  - 3 to 24 temperature monitoring channels
  - 60 to 384 I/Os and 640 to 9400 LUTs density
- Precision Voltage Monitoring Increases Reliability**
  - Programmable threshold from 0.67V to 5.7V & 4.5V to 13.2V
  - Differential input sensing
  - Over/under voltage detection with window comparison
  - 10-bit voltage measurement ADC
- Temperature Monitoring Simplifies Thermal Management**
  - Measures temperature using external diode
  - Over/under temperature detection
  - Temperature measurement range -60 to +150°C
- High-side Current Measurement Reduces BOM**
  - Measures current across shunt resistor
  - Differential range 7.5mV to 200mV
  - Common mode voltage up to 13V
  - Programmable gain amplifier for current measurement
  - Fast fault detection (1µs) and over current detection
- High-Voltage FET Drivers Reduce # POLs Needed**
  - Scalable from 4 to 32 N-channel MOSFET drivers
  - Digitally controlled power supply ramp control
  - Open drain output support
- Margining and Trimming for Quality Assurance**
  - Scale from 4 to 32 power supplies
  - Digital closed-loop mode of operation
  - Voltage scaling and VID control
- PLD to Integrate Power, Thermal & Control Plane Functions**
  - Up to 9400 LUTs and up to 384 user I/Os
  - Support for multiple interface standards
- System Level Support**
  - Single 3.3V or 12V supply operation
  - Industrial temperature range
- In-System Re-programmability Reduces Risk**
  - On-chip configuration memory
  - JTAG/I<sup>2</sup>C programming interface and background update
  - Dual-boot recovery



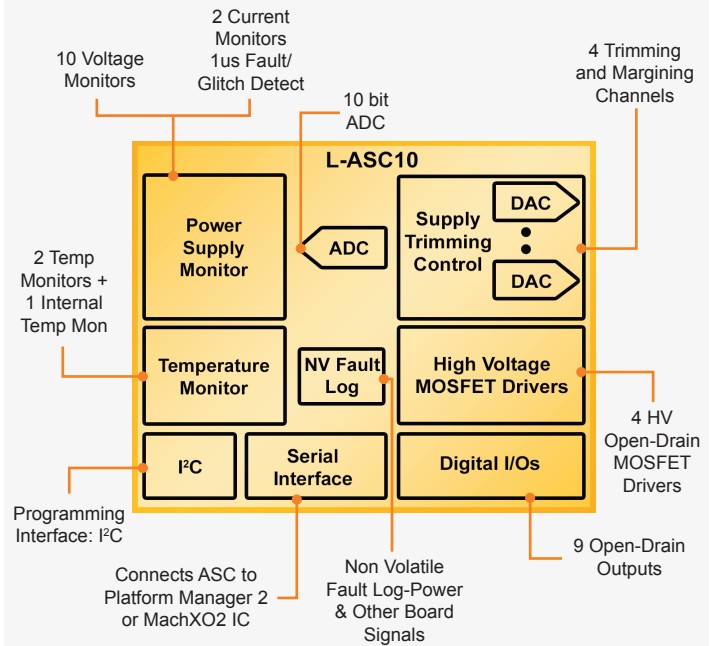
## Platform Manager 2 Architecture

### Hardware Management Controller

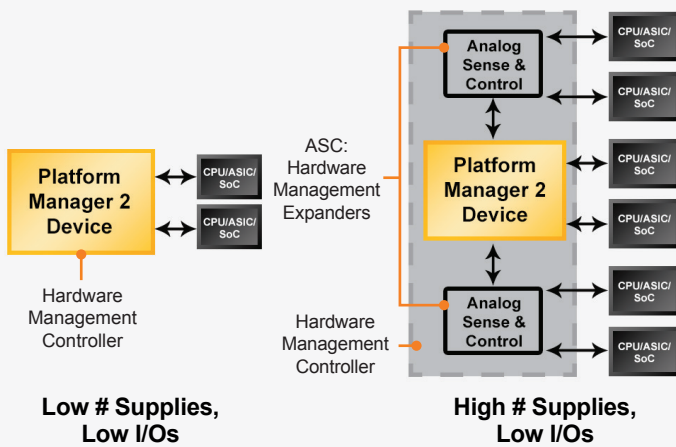


## Analog Sense and Control (L-ASC10)

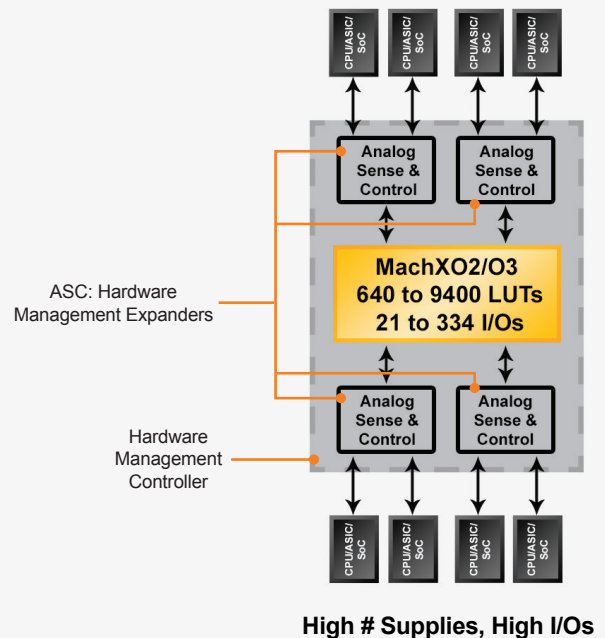
### Hardware Management Expander



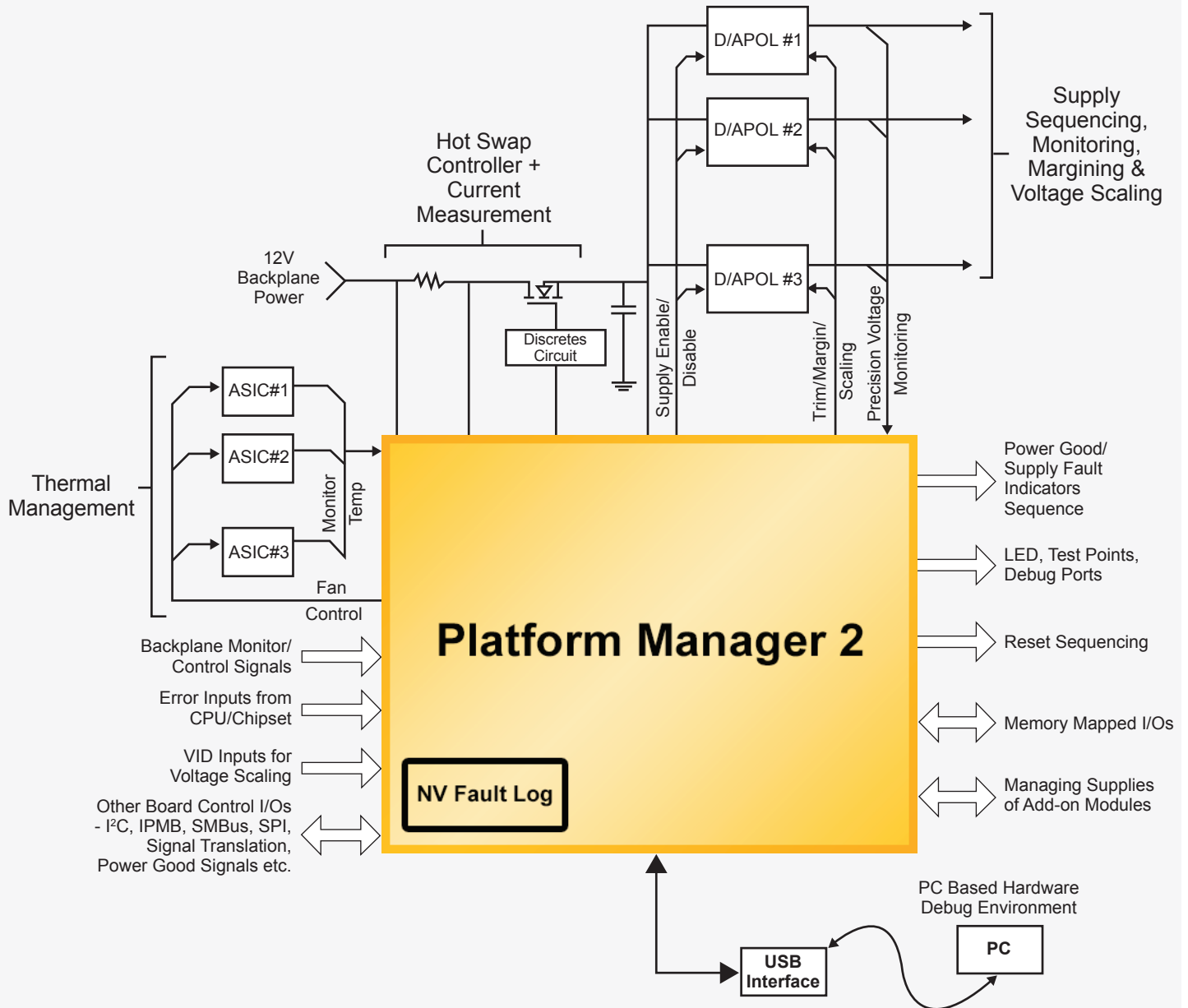
## Hardware Management Using Platform Manager 2



## Hardware Management Using MachXO2/XO3 + L-ASC10



# Hardware Management With Platform Manager 2



## Advantages

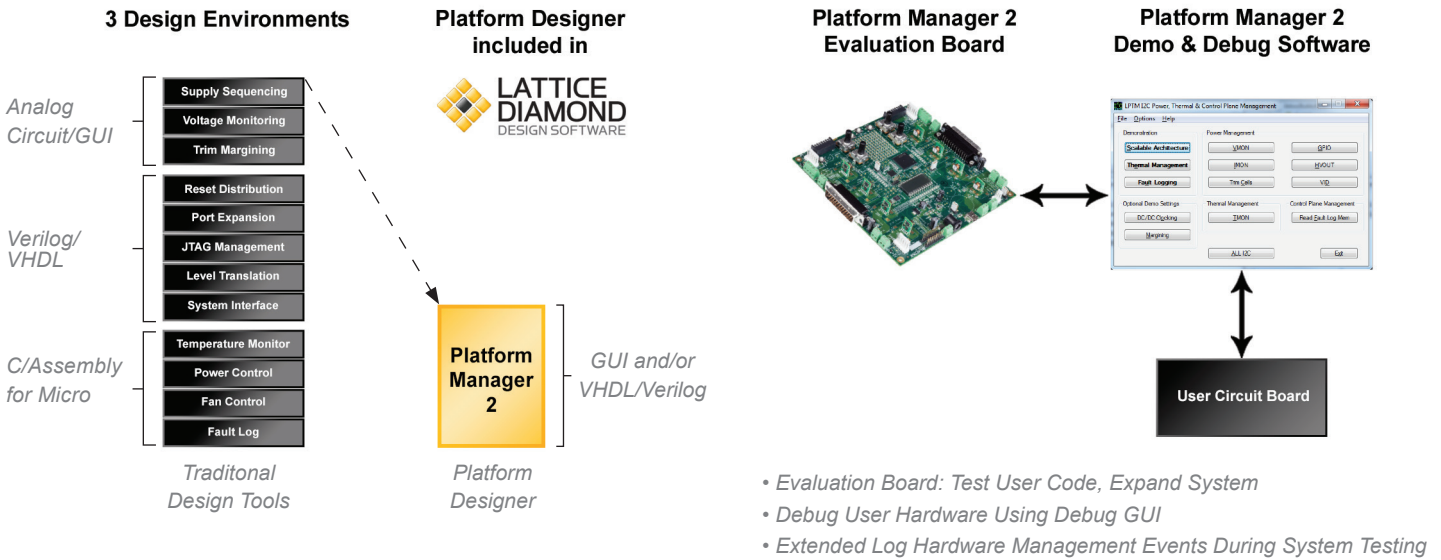
- **Increased Reliability**
- **Smaller Board Space**
- **Reduced Number of Components**
- **Reduced Risk of Board Re-spin**
- **Reduced Time-to-market**
- **Standard Solution Across a Wide Range of Applications**
- **Single Design Environment with End-to-end Simulation**

# Platform Designer

Unified, Flexible, Verifiable Design Methodology

# Development Tools

Development Boards + Debug Aid Software



## Platform Manager 2 Family

	H/W Management Expander	Hardware Management Controller
	L-ASC10	LPTM21
Voltage Monitoring Inputs	10	10
Current Monitoring Inputs	2	2
Temperature Monitoring Inputs	2	2
Number of Trimming Channels	4	4
MOSFET Drives	4	4
On-Chip Non-Volatile Fault Log	✓	✓
Number of LUTs	-	1280
Distributed RAM (kbits)	-	10
EBR SRAM (kbits)	-	64
Number of EBR Blocks (9 kbits)	-	7
User Flash Memory (kbits)	-	64
Number of PLLs	-	1
Communication I/F	I <sup>2</sup> C	I <sup>2</sup> C/SPI/JTAG
Programming Interface	I <sup>2</sup> C	I <sup>2</sup> C/SPI/JTAG
Operating Voltage	3.3	2.8V to 12V
Insystem Update Support	Yes	
Package Options	Digital I/Os	
48-pin QFN (7 X 7)	9	
237-Ball ftBGA (1mm) (17X17)		106

### Applications Support

[www.latticesemi.com/support](http://www.latticesemi.com/support)



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