JPEG-DX-S

Baseline and Extended JPEG Decoder

The JPEG-DX-S IP core is an area-efficient, high-performance JPEG decoder conforming to the Baseline Sequential DCT and the Extended Sequential DCT modes of the ISO/IEC 10918-1 standard.

It decompresses JPEG images, and also video payload for Motion-JPEG container formats. It supports 8- or 12-bit color samples and up to four color components, in all widely-used color subsampling formats. The decoder processes one color sample per clock cycle, enabling it to process Full-HD video even in low-cost FPGAs. One of the smallest JPEG decoders available, it requires under 12,000 LUT4s when mapped on a Lattice FPGA.

Once programmed, the easy-to-use encoder operates on a standalone basis, parsing marker segments and decompressing coded data with no assistance from a host processor. The decoder reports the image format (i.e., resolution, subsampling format, and color sample-depth) to the system, so that the decoded images are properly further processed and/or displayed.

SoC integration is straightforward thanks to standardized AMBA® interfaces: AXI Streaming for pixel and decompressed data, and a 32-bit APB slave interface for registers access.

Customers with a short time to market requirements can use CAST's IP Integration Services to receive complete JPEG subsystems. These integrate the JPEG encoder with video interface controllers, Hardware UDPIP or Transport Stream networking stacks, or other IP cores available from CAST.

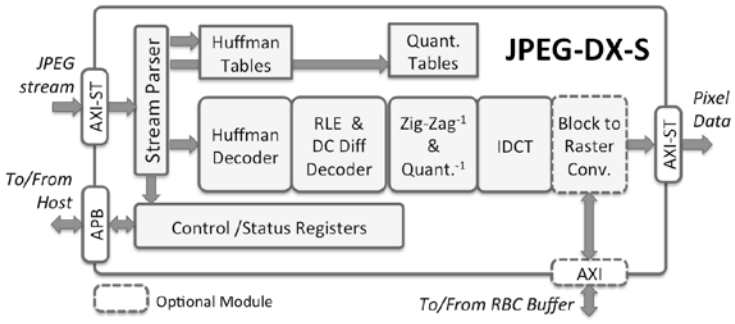
The core is designed with industry best practices, and its reliability and low risk have been proven through both rigorous verification and customer production. Its deliverables include a complete verification environment and a bit-accurate software model.

Applications

The JPEG-DX-S core's excellent performance and low silicon resource usage make it suitable for implementing a variety of digital imaging applications, including:

- Residential, corporate, airborne, and other security or surveillance systems.
- Machine vision and video link decoders/terminals for industrial, defense, or other systems.
- Medical imaging system, and advanced driver assistance systems.

Block Diagram



Features

Area-efficient, high-performance 8/12-bit JPEG decoder for ASICs and FPGAs

Standards Support

- ISO/IEC 10918-1 Standard Baseline and Extended Decoder (Sequential DCT modes)
- Single-frame JPEG images and Motion JPEG payloads
- Up to four color components
- 8- and 12-bit color samples
- All widely used color-sub-sampling formats, and any image size up to 64k x 64k
- All scan configurations and all JPEG formats
- All marker segments expect DNL
- Up to four Huffman Tables
- Up to four b-nit or 18-bit Quantization tables

Interfaces

- AXI Streaming I/O data interfaces
- APB Control/Status interface
- Optional AHB wrapper with DMA capabilities

Performance and Size

- One decoded sample per clock cycle
- Small silicon footprint (less than 12k LUT4s)

Ease of Integration

- Requires no programming or control from host
- Reports image format
- Detects and reports marker syntax errors
- Delivered with bit-accurate software model
- Optional Block-to-Raster Conversion with AXI or standard memory interface towards the lines buffer

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Silicon Resources Utilization

The JPEG-DX-S can be mapped to any Lattice Device (provided sufficient silicon resources are available) and optimized to suit the particular project's requirements. The following table provides sample implementation and performance data for the default configuration of the core.

Family / Device	Logic	Block RAMs	DSP Comp.	Fmax (MHz)
ECP5U / LAE5U-12F	11.843 LUT4s 8,340 Slices	9	8	70

Note that the implementation figures do not represent the highest speed or smallest area possible for the core. Please contact CAST to discuss silicon resource utilization and performance for your target technology.

Verification

The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products and is proven in both ASIC and FPGA technologies.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms and includes everything required for successful implementation. The ASIC version includes:

- Verilog RTL source code
- Sophisticated self-checking Testbench
- Software (C++) Bit-Accurate Model
- Sample simulation and synthesis scripts
- Comprehensive user documentation

JPEG Cores available from CAST

The JPEG-DX-S is a member of the JPEG family of cores that CAST offers. The following table summarizes the family members and highlights their basic features.

	JPEG-E-S Baseline JPEG Encoder	**JPEG-EX-S** Extended JPEG Encoder	**JPEG-EX-F** Ultra Fast Ext. JPEG Encoder	**JPEG-D-S** Baseline JPEG Decoder	**JPEG-DX-S** Extended JPEG Decoder	**JPEG-DX-F** Ultra Fast Ext. JPEG Encoder
Functionality	Encoder			Decoder		
Baseline JPEG	✔	✔	✔	✔	✔	✔
Extended Sequential JPEG	✖	✔	✔	✖	✔	✔
Motion JPEG Payload	✔	✔	✔	✔	✔	✔
Sub-sampling Formats	Any with up to four components including Single–color, 4:4:4, 4:2:2, 4:2:0					
Image Resolution	16x16 to 64k x 64k					
Max. Sample Depth	8	12	12	8	12	12
Rate Control	✔	✔	✔	N/A	N/A	N/A
Raster Conversion	Included – Optionally Instantiated					
Color Samples/Cycle	1	1	1 to 32	1	1	1 to 32
Number of LUT4s in LATTICE FPGAs	11k	13k	22k[1]	10k	12k	18k[1]
Available in RTL Source Code	✖	✔	✔	✖	✔	✔
Available as targeted netlist	✔	✔	✔	✔	✔	✔

1) Silicon Resources for two samples/cycle configuration, and 12 bits per color sample

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BEYOND SEMICONDUCTOR
The JPEG-DX-S core is sourced from Technology Partner Beyond Semiconductor.