MachXO USB Starter Kit

Complete USB working solution for designing with the unique Lattice MachXO non-volatile programmable logic technology

MachXO - Crossover PLD

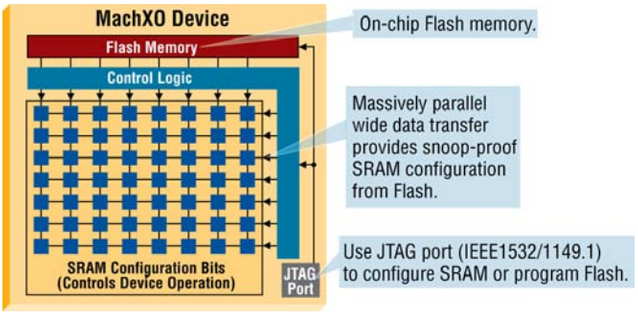
The MachXO family of non-volatile infinitely reconfigurable Programmable Logic Devices (PLDs) is designed for applications traditionally implemented using CPLDs or low-capacity FPGAs

The MachXO family combines an optimized Look-Up Table (LUT) fabric with Lattice's ispXP technology to provide the high pin-to-pin performance and instant-on associated with CPLDs, with the flexibility of FPGAs, all in a single low-cost device.

The MachXO Starter Kit is a simple, yet versatile solution allowing for detailed analysis of the MachXO performance and technology.

The board is also a convenient platform to help you get started with your own MachXO design Lattice's ispLEVER development tools included in the MachXO Starter Kit offer a comprehensive design environment for the MachXO architecture.

MachXO Configuration



Key Features

1. MachXO device LCMXO640C-3TN144C
2. Built in USB download capability with USB controller and MachXO256 device
3. Power supply and JTAG via USB
4. 24 Mhz oscillator
5. Power LED and 8 status LEDs
6. 4-DIP switch and push button reset
7. USB A connector and 1.8M USB cable
8. Lattice Starter Software on DVD
9. Data and Tutorials

Ordering Information

Product	Description	Ordering Part #
MachXO USB Starter Kit	USB MachXO evaluation board	HWD-XO-USB

www.hardware-design.de

Lattice Semiconductor Corporation
More of the Best

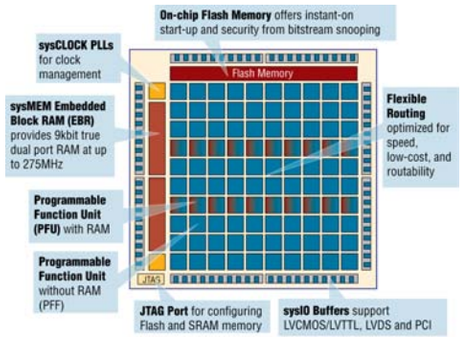
LATTICE : MORE OF THE BEST

MachXO Family

Key Features and Benefits

- Non-Volatile, Infinitely Reconfigurable
- Instant-on, powers up in less than 1mS
- Single-chip, no external configuration memory
- Excellent design security, no bit stream to intercept
- Performance to 3.5ns Pin-to-Pin
- TransFR Technology Allows Simple Field Upgrades
- Flexible LUT Architecture
- 256 to 2280 LUT4s
- 73 to 271 I/Os with extensive package options
- Density migration supported
- Embedded and Distributed Memory
- Up to 27.6 Kbits sysMEM Embedded Block RAM
- Includes dedicated FIFO control logic
- Up to 7.7 Kbits distributed RAM
- Flexible I/O Buffer
- Programmable sysIO™ buffer supports wide range of interfaces:
  - LVCMOS 3.3/2.5/1.8/1.5/1.2
  - LVTTL
  - PCI*
  - LVDS*, Bus-LVDS*, LVPECL*,
- sysCLOCK PLLs
- Up to two analog PLLs per device
- Clock multiply, divide and phase shifting
- Sleep Mode Reduces Standby Power to <100µA
- System Level Support
- IEEE Standard 1149.1 Boundary Scan
- On chip 20MHz oscillator for configuration and user logic
- Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply
- Commercial: 0 to 85C (TJCOM)
- Industrial: -40 to 100C (TJIND)
- AEC-Q100 qualified: -40 to 125C (TJAUTO)

* MachXO1200 and 2280 devices only.



Parameter	LCMXO256	LCMXO640	LCMXO1200	LCMXO2280
LUTs	256	640	1200	2280
Distributed RAM (Kbits)	2	6.1	6.4	7.7
Embedded Block RAM – EBR (Kbits)	–	–	9.2	27.6
Number of EBR Blocks	–	–	1	3
V_{CC} Voltage (V) Options	1.2V or 1.8/2.5/3.3V	1.2V or 1.8/2.5/3.3V	1.2V or 1.8/2.5/3.3V	1.2V or 1.8/2.5/3.3V
Number of PLLs	–	–	1	2
Number of I/O Banks	2	4	8	8
Maximum Number of I/Os	78	159	211	271
Maximum Number of LVDS Pairs*	–	–	27	33
Packages & I/O Combinations				
100-pin TQFP (14 x 14 mm)**	78	74	73	73
144-pin TQFP (20 x 20 mm)		113	113	113
100-ball csBGA (8 x 8 mm)	78	74		
132-ball csBGA (8 x 8 mm)		101	101	101
256-ball ftBGA (17 x 17 mm)		159	211	211
324-ball ftBGA (19 x 19 mm)				271

** Number of LVDS outputs can be increased by emulating with external resistors.*

*** In the 100-pin TQFP package, designs can not migrate from LCMXO640 to 1200.*