Enhanced MachXO3™ Family Overview

The MachXO3™ family is Lattice's latest instant-on, lowest cost per I/O, non-volatile FPGA line, ideally suited for control PLD and bridging applications across many types of systems in communications, computing, industrial and consumer segments. Spanning from 640 to 9400 LUTs and available in lower power E (1.2 V core) or easy-to-use C (3.3/2.5 V core) versions, the MachXO3 family offers the latest in small packaging, microwatt power consumption and high I/O count. Designed for an easy integration of advanced control and security functions in servers and communication systems, this family also meets the high-bandwidth and high-resolution requirements for mobile consumer, industrial, and medical applications. The MachXO3L devices include multi-time programmable Non-Volatile Configuration Memory (NVCM), while the MachXO3LF devices support infinitely programmable Flash.

Key Features

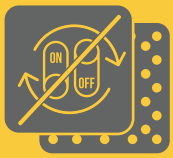
- **640 – 9400 LUTs density options**
- **Up to 384 I/Os**
  - 900 Mbps
  - 1.0 V to 3.3 V I/O Interface
- **Hard I²C & SPI cores**
- **High performance PLLs, built-in oscillator with low-skew edge clock routing**
- **Password protection against malicious erasure/updates**
- **Soft Error Correction (SEC) to deterministically recover from Soft Errors**
- **Hitless I/O to support device reconfiguration in high availability systems**

Enhanced MachXO3L Family	XO3L-640	XO3L-1300	XO3L-2100	XO3L-4300	XO3L-6900	XO3L-9400
Features	XO3LF-640	XO3LF-1300	XO3LF-2100	XO3LF-4300	XO3LF-6900	XO3LF-9400
Density LUTs	640	1300	2100	4300	6900	9400
EBR RAM (Kbits)	64	64	74	92	240	432
PLL	1	1	1	2	2	2
Multi Time Programmable NVCM	XO3L-640	XO3L-1300	XO3L-2100	XO3L-4300	XO3L-6900	XO3L-9400
Flash	XO3LF-640	XO3LF-1300	XO3LF-2100	XO3LF-4300	XO3LF-6900	XO3LF-9400
SPI Interface	1	1	1	1	1	1
I²C interface	2	2	2	2	2	2
Oscillator	1	1	1	1	1	1
Timer/Counter	1	1	1	1	1	1
MIPI D-PHY Support	Yes	Yes	Yes	Yes	Yes	Yes
Packages						
36-ball WLCSP (0.4, 2.5 x 2.5)		28				
49-ball WLCSP (0.4, 3.2 x 3.2)			38			
81-ball WLCSP (0.4, 3.8 x 3.8)				63		
121-ball csfBGA (0.5, 6 x 6)	100	100	100			
256-ball csfBGA (0.5, 9 x 9)		206	206	206	206	206
324-ball csfBGA (0.5, 10 x 10)			268	268	269	
256-ball caBGA (0.8, 14 x 14)		206	206	206	206	206
324-ball caBGA (0.8, 15 x 15)			279	279	279	
400-ball caBGA (0.8, 17 x 17)				335	335	335
484-ball caBGA (0.8, 19 x 19)						384

Explore MachXO3, visit www.latticesemi.com/MachXO3

Enhanced Features

Hitless I/O



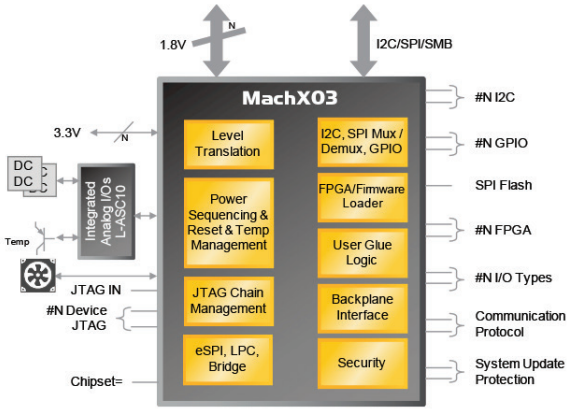
- Power recycling not needed for reconfiguration
- Improved SED immunity for critical nets
- No software modifications needed

SEC / SED

- Detect and log soft error events
- Background soft error mitigation
- Controlled soft error injection for debugging soft error mitigation

900 Mbps I/O

- Bridging support for high-resolution images
- Futureproof your designs for sensors and displays
- Coupled with increased EBR for improved image sharpness



Control PLD

- Embedded I²C, SPI hardware blocks simplify designs
- Non-volatile PLD (640 to 9400 LUTs & 28 to 384 I/O) provides widest application coverage in servers, communication boxes and Industrial controllers
- Perform voltage level translation with ease
- Reduce overall cost by integrating Power Manager and Temperature Sense ICs

CSI-2 Image Sensor Interfacing

- Supports CSI-2 High Speed Differential Signaling
  - Both Rx and Tx interfaces available
- From 1-4 lanes of CSI-2 at up to 900 Mbps
- Can be implemented in a WLCSP (3.2 x 3.2mm)
- RAW, YUV or RGB supported

DSI LCD Display Interfacing

- Supports DSI transmit signaling
  - HS (High Speed) Mode transmit
  - LP (Low Power) Mode transmit and receive
- Can be implemented in a 49 WLCSP (3.2 x 3.2mm)
- Supports DSI formats RGB, YCbCr and User Defined
- Input can also be DSI to enable LCD screen replacements

Applications Support
www.latticesemi.com/support

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