

ORCA ORLI10G Evaluation Board

Measure the Performance of a 10Gbits/s Integrated Data Communication Solution

Making the Right Choice...

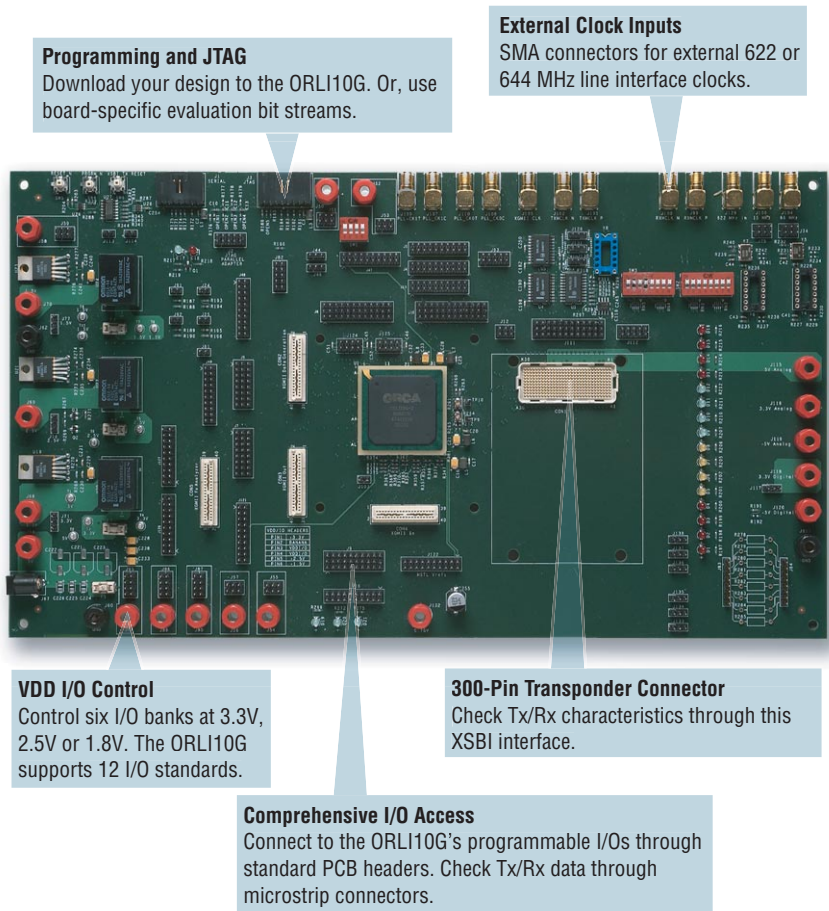
Choosing the right 10Gbits/s solution is an important investment decision, but evaluating your options shouldn't be complicated. Lattice has created the ORCA® OLI10G Evaluation Board so you can efficiently test the performance of a real-world 10Gbits/s design based on the ORLI10G Field Programmable System Chip (FPSC) architecture.

Examine Features Such as:

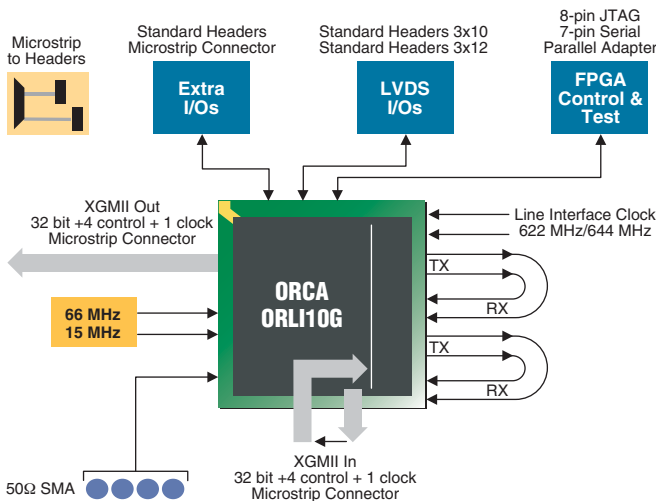
- FPSC flexibility and features
- ORLI10G functionality and performance
- Programmable I/O capabilities
- Output strength and clarity

Working on an ORLI10G Application?

Use the ORLI10G Evaluation Board to help develop your customized ORLI10G data-communications solution in an established and flexible environment.

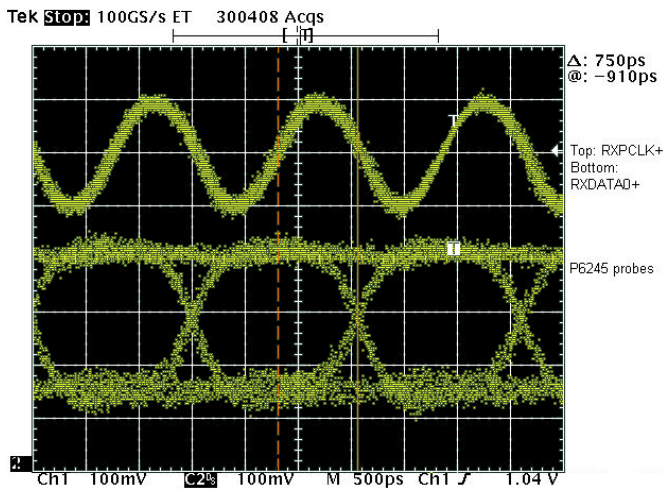


ORLI10G Evaluation Board and Block Diagram



Full Feature Set

- 316 of the ORLI10G's I/Os are accessible on the board, including:
 - 32-bit dual data rate
 - XGMII IN and OUT (with four control signals and one clock)
 - 3x10 / 3x12 LVDS I/Os
 - I/O available directly from more than 600K FPSC system gates.
- Includes a regulated power supply for easy set-up.
- Downloadable programming bit streams are available from www.latticesemi.com for testing specific functions of the ORLI10G.



About the ORCA ORLI10G...

Lattice's ORLI10G is an ORCA Series 4-based Field Programmable System Chip which integrates a high-speed dedicated line interface with a flexible FPGA logic core.

- More than 600K of usable FPGA gates, internal performance of >250MHz.
- Compatible with system standards such as OC-192/STM-64 SONET/SDH, Quad OC-48/STM-16 10 Gbits/s Ethernet and 10 Gbits/s OTN (Digital Wrapper/Strong FEC) or 12.5 Gbits/s SuperFEC.
- Integrated Tx/Rx programmable PLLs for conversion between line-side and system-side 16-bit LVDS data rates of up to 850Mbit/s.
- Timing and jitter specifications compliant to OIF 99.102.5 standard.
- Receive-side interface can be split into four separate asynchronous 2.5 Gbits/s interfaces.
- Programmable I/O with programmable drive and slew rate control supports LVTTTL, LVCMOS, GTL, GTL+, PECL, SSTL/3, HSTL, ZBT, DDR, LVDS, BLVDS and LVPECL.
- 316 Programmable user I/O

See www.latticesemi.com for complete specifications of the ORLI10G.

ispLEVER™ Development Tools

ispLEVER is an integrated software system for the development of all Lattice programmable logic devices, including the ORLI10G. The ispLEVER software incorporates ASIC design techniques and FPGA development methodologies that meet today's high-speed design demands.



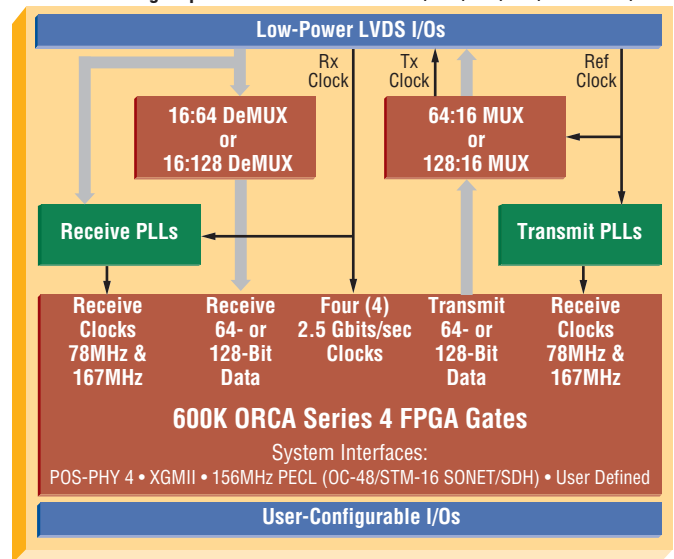
ORLI10G Has an Eye for You!

Getting data from A to B with minimal distortion has always been important. But with data wavelengths shorter than your backplane, clean signals are crucial! We've focused our engineering efforts on the ORLI10G I/O structure to provide high-quality data transmission exceeding today's tight standards.

With the ORLI10G Evaluation board, you can measure the I/O performance of the ORLI10G in an environment you control. The signal to the left is an actual data-eye of an XSBI / 10Gbit Ethernet signal generated by the ORLI10G's LVDS I/Os, operating at 644MHz.

ORCA ORLI10G Block Diagram

Selectable High-Speed Data Rates – 16X 622/645/667/781/850 Mbits/sec



- Included with the ORLI10G Evaluation Board:
 - ORLI10G-2BM680 device
 - ORCA Download Cable
 - Power supply
 - Board schematic and bill of materials
- Available on www.latticesemi.com:
 - ORLI10G Eval Board User Manual and Tutorial
 - IBIS and HSPICE models, and BSDL files
 - Schematic and Gerber files
 - Evaluation bit streams

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www.latticesemi.com

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