Lattice provides customers with low cost and low power programmable solutions that are ready-to-use right out of the box. A full suite of tested and interoperable solutions is available for Ethernet applications, including:

- FPGAs with Embedded Ethernet-compliant SERDES
- A Complete Portfolio of Soft and Hard IP Cores for 10GbE, 2.5GbE, 1GbE, and 10/100 Ethernet Stacks
- Application Specific Development Boards, Systems and Reference Designs
- Test and Interoperability Reports for PMA, PCS and MACs

**Ready-to-Use Ethernet Portfolio**

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**LatticeECP3™ Low Cost FPGA**

- Low Cost Digital SERDES
  - Ideal for low cost chip-to-chip and small factor backplane applications
  - Exceeds XAUI Tx and Rx requirements
  - 1000BaseX Jitter Compliant
- Up to 16 Channels per Device
  - Useful for multi-port switching
- Complete End-to-End Solution
  - Soft XAUI PCS and 10GbE MAC implementations available
  - Soft SGMII and TS-MAC implementations available
- Very Low SERDES Power (~110mW Per Channel Typical @ 3.2Gbps)
- Low Cost FPGA Fabric
  - High end features at low cost

**LatticeSC™ Extreme Performance FPGA**

- High Performance Analog SERDES
  - Exceeds XAUI TX and RX requirements
  - Ideal for long Ethernet-based backplanes
- Up to 32 Channels per Device
  - Useful for multi-port switching
- Data Rates Up to 3.8 Gbps
  - Exceeds XAUI baud rate specifications
- Complete End-to-End Solution
  - Rich PCS functionality
  - flexiMAC™ supports both GbE and 10GbE MACs, saves cost and power
  - Soft SGMII and TS-MAC implementation available
- Very Low SERDES Power (105mW Per Channel Typical @ 3.125Gbps)
- Extreme Performance FPGA Fabric
  - 500MHz block level performance

### XAUI PCS
- **Platform:** ECP3
- **Soft IP**
- Compliant to IEEE802.3ae for XAUI
- Implements TX and RX State Machines
- XGMII Interface to FPGA Fabric

### GbE & SGMII PCS
- **Platform:** ECP2, ECP2M, SC/M
- **Soft IP**
- Compliant to IEEE802.3z
- MAC or PHY Modes (Pin Selectable)
- RX and TX State Machines and Autonegotiation
- Rate Adaptation for 10/100 MII Frames
- 8-bit GMII MAC Interface

### flexiPCS™
- **Platform:** SCM
- **Hard PCS Block**
- Supports IEEE802.3ae XAUI and IEEE GbE PCS
- GMII (GbE) and XGMII Interfaces to FPGA Fabric

### Tri-Speed MAC
- **Platform:** ECP2, ECP2M, XP2, SC
- **Soft IP**
- 10/100/1000 Mbps Operation
- Compliant to IEEE 802.3z
- Generic FIFO Interface
- Programmable IPG
- TX and RX Statistics Vectors
- Multicast Address Filtering
- Management Interface
- FCS on TX and RX
- Supports:
  - Full Duplex control with PAUSE frames
  - VLAN tagged frames
  - Automatic padding of short frames
  - Automatic re-transmission on collision
  - Broadcast and multicast frames
  - Jumbo packets (up to 8192 bytes)

### 10GbE MAC
- **Platform:** ECP2, ECP2M, SC
- **Soft IP**
- Compliant to IEEE802.3ae-2002
- Optional HiGig/+ Capability for Broadcom StrataXGS I/II Switches (LatticeSC only)
- XAUI or XGMII Interface
- System Aide FIFO Interface
- Programmable IPG
- TX and RX Statistics Vectors
- Multicast Address Filtering
- MDIO Interface
- Supports:
  - Full duplex control with PAUSE frames
  - VLAN tagged frames
  - Automatic padding of short frames
  - FCS on TX and RX
  - Jumbo packets

### flexiMAC
- **Platform:** SCM
- Implemented on MACO Structured ASIC Technology
- Can be Configured as a 10G or 1G MAC
- Saves Up to 5K LUTs in FPGA Real Estate
- Low Power Implementation (100mW max)
- No IP Licensing Fees

### 2.5GbE MAC
- **Platform:** SC
- **Soft IP Bundle**
- 10/100/1000 Mbps Operation
- Compliant to IEEE 802.3z
- Generic FIFO interface
- Programmable IPG
- TX and RX Statistics Vectors
- Multicast Address Filtering
- MII/GMII Interface
- Management Interface
- FCS on TX and RX
- Supports:
  - Full Duplex control with PAUSE frames
  - VLAN tagged frames
  - Automatic padding of short frames
  - Automatic re-transmission on collision
  - Broadcast and multicast frames
  - Jumbo packets

### XAUI to SPI4.2 Fabric Interface
- **Platform:** SCM
- **Hard and Soft IP Bundle**
- Bundle Includes:
  - No-charge Bridge Reference design with source code
  - SPI4.2 MACO (No IP licensing fee)
  - 10GbE MAC IP
  - Optional HiGig® Capability for Broadcom StrataXGS® I/II Switches
  - Single Instance Fits into LatticeSC15 Device
    - 17x17 256fpBGA – industry's smallest footprint (by 40%)
    - Lowest power SERDES at 3.125Gbps (105mW)
    - Lowest power SPI4.2 implementation (0.85W)
  - Maximum Bandwidth of 12.5Gbps
  - Tested with Broadcom StrataXS Switches
  - Lattice Developed and Supported
LatticeMico32 Tri-Speed Ethernet Media Access Controller (TSMAC) demo shows the capability of the TSMAC IP core to function in a real network environment.

- Uses Lattice open source LatticeMico32 soft RISC processor
- Web server application
- Includes MAC device drivers and open source lightweight IP (lwIP) stack

The LatticeMico32 Tri-Speed Ethernet Media Access Controller (TSMAC) demo requires no test equipment, lengthy setup or complex explanation. The demo uses a Web server to demonstrate the Tri-Speed MAC IP core, using the open-source lightweight IP (lwIP) network stack.

Lattice Ethernet Evaluation Platforms

<table>
<thead>
<tr>
<th>Board Name</th>
<th>Ethernet Interfaces</th>
<th>Other Interfaces</th>
<th>Memory Interfaces</th>
</tr>
</thead>
<tbody>
<tr>
<td>LatticeECP3 Evaluation Platforms</td>
<td>• SMAs for SERDES (4 channels) • RJ-45</td>
<td>• PCIe x4 Edge Finger</td>
<td>• DDR3 Component (8 bit)</td>
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<tr>
<td>I/O Protocol Board</td>
<td>• SMAs for SERDES (4 channels) • RJ-45</td>
<td>• SPI4.2 Connector</td>
<td>• DDR2 Component (18 bit)</td>
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<tr>
<td>LatticeECP2M™ Evaluation Platforms</td>
<td>• SMAs for SERDES (3 channels) • Breakout Card for RJ-45</td>
<td>• PCIe x4 Edge Finger</td>
<td>• DDR2 Component (18 bit)</td>
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<tr>
<td></td>
<td>• RJ-45</td>
<td>• SMAs for LVDS I/O</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• RJ-45</td>
<td>• BNC for SMPTE</td>
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<tr>
<td>LatticeSC Evaluation Platforms</td>
<td>• SMAs for SERDES (8 channels) • SPI for MSA300 • Breakout Card for RJ-45</td>
<td>• SPI4.2</td>
<td>• DDR2 SODIMM (64 bit)</td>
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<tr>
<td></td>
<td>• RJ-45</td>
<td>• SMAs for LVDS I/O</td>
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<tr>
<td></td>
<td>• RJ-45</td>
<td>• DDR2 Component (18 bit)</td>
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<tr>
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<td>• SMAs for SERDES (4 channels) • Breakout Card for RJ-45</td>
<td>• PCIe x4 Edge Finger</td>
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<tr>
<td></td>
<td>• RJ-45</td>
<td>• SMAs for LVDS I/O</td>
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<tr>
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<td>• SFP Optical Cage (SGMII)</td>
<td>• DDR2 Component (18 bit)</td>
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<td></td>
<td>• SMAs for LVDS I/O</td>
<td>• DDR2 Component (18 bit)</td>
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<tr>
<td></td>
<td>• RJ-45</td>
<td>• PCIe x1 Edge Finger</td>
<td>• RLDAM and QDR2 (18 bit)</td>
</tr>
</tbody>
</table>

The LatticeMico32 Tri-Speed MAC Demo Board
Hardware Testing
Lattice tests all critical components of the Ethernet stack rigorously, and puts a great deal of emphasis on interoperability with proven 3rd party silicon platforms. The following test documentation is available for customer review.

PMA ELECTRICAL CHARACTERIZATION
See Lattice technical note TN1084 and supplements (available under NDA) for ANSI11.2 and IEEE802.3-2002 Electrical Tests for LatticeECP3, LatticeECP2M and LatticeSC SERDES.

INTEROPERABILITY
The following test and interoperability documentation is available for customer review:

<table>
<thead>
<tr>
<th>Lattice Device Family</th>
<th>Ethernet Protocol</th>
<th>Marvell Alaska 88E1111/881112</th>
<th>Broadcom StrataXGS</th>
<th>PMC Sierra PM3388</th>
</tr>
</thead>
<tbody>
<tr>
<td>LatticeECP3</td>
<td>1GbE PMA/PCS</td>
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<td>✓</td>
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<td>SGMII PMA/PCS</td>
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<tr>
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<td>SPI4.2</td>
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<td>✓</td>
</tr>
</tbody>
</table>

Lattice IPexpress™ Tool
The IPexpress tool revolutionizes the way users design with Lattice IP cores and greatly simplifies IP design. The IPexpress design flow enables users to fully characterize IP in real-time. The designer can then instantiate the user-configured IP and complete the design process, including full timing simulation and bitstream generation.

VIEW IP CORES AVAILABLE FOR DOWNLOAD
From the Lattice IP Server Tab within IPexpress, you can view available ispLeverCORE™ user-configurable IP cores for download.

INSTALL OR DOWNLOAD IP CORES
You can download and install ispLeverCORE user-configurable IP cores on your computer, or you can simply download them and install them later.

Lattice’s IPexpress tool can be used to easily configure both MACO hard IP and Lattice’s growing selection of soft IP cores.

Lattice Ethernet Portfolio Guide