

## Product Brief : DisplayPort 1.4a IP Core Lattice Jedi-D1

DisplayPort heralds a new alternative in video connectivity. Designed to enable low cost direct drive monitors and backed by industry leaders (Intel, DELL, Apple etc) DisplayPort is not hindered by license and royalty fees.

The Bitec DisplayPort IP core for Lattice Jedi-D1 FPGA devices offers a cost-efficient industry leading solution to rapidly develop and deliver displays offering a superior viewing experience within ever-shrinking product lifecycles. The core is used extensively in FPGA based products and in high-volume OEM ASIC applications.

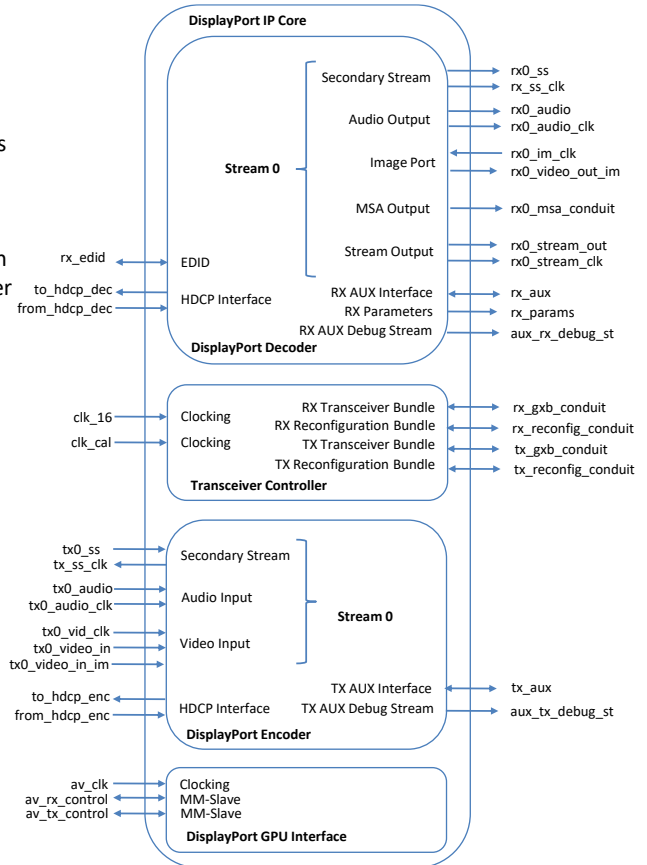
The Bitec DP IP core accepts 1,2,3 or 4 lanes at arbitrary link rates. In accordance with the DP specification 1.4a, the core will adapt and train to the transmitting source capability via a firmware driven policy maker API.

The source and sink cores accept v/h/d-sync and parallel RGB data. Audio data and raw Auxiliary data ports to the cores provide flexible side-band messaging.

Bitec also offer a tailoring service for bespoke designs. For more information contact Bitec.

### Features

- Feature rich parametrization for optimal designs
- Efficient clock resource usage
- Support for 1,2,3 & 4-lane
- Support DisplayPort 1.4a (eDP support)
- Support 1.62Gbps increment link rates
- Dual/quad symbol modes
- Versatile PMA/PHY interface (PiPE 5.2 support)
- Single/dual/quad pixel modes
- 6,8,10,12 & 16 bit color support
- Multi bus support register control interface
- Supports RGB, YCbCr Colorimetric Formats (444,422,420)
- Support RAW and Y-only color formats
- API Controlled AUX channels up to 256-byte messages
- Optional HDCP 2.2/1.3 Support
- 8-Channel Audio
- Adaptive-Sync support
- Forward Error Correction
- eDP Features supported
- ALPM
- Power optimized architecture via clock management
- Full, portable API in C-language for policy layer



### Preliminary Resource Usage (4-Lane 8.1Gbps)

- DP RX : 12k LUT4, 8k PFU, 33 EBR
- DP TX : 2.5k LUT4, 2.5k PFU, 35 EBR

### Deliverables

- Encrypted or source code DP 1.4 IP
- Binary or source code API libraries
- Documentation
- FPGA Example designs
- Simulation environment
- Constraint files

Contact [info@bitec-dsp.com](mailto:info@bitec-dsp.com) for more information