Lattice Sets Midrange FPGA Collision

By Linley Gwennap (May 24, 2021)

Known for tiny low-power FPGAs, Lattice Semiconductor is raising its sights to the market's midrange. It disclosed a new FPGA family called Avant that will include members with at least five times the gate count of its existing products. After starting development in late 2019, it expects to introduce the first Avant devices late next year.

Lattice competes in the low-end FPGA segment, where it holds about a 25% market share, using its innovative Nexus products, which feature up to 39,000 logic cells (LUTs) and 2.5Mbits of SRAM with 5Gbps I/O (see *MPR 2/3/20,* "Lattice First With FPGA in FD-SOI"). In this segment, it competes against the FPGA leaders, Intel and Xilinx, in addition to smaller suppliers such as Efinix and Microchip.

The company says it was drawn into the midrange segment at the request of customers, who aren't getting innovation from their current suppliers. Xilinx shipped its first midrange Artix 7 products back in 2013, the same year that Intel's midrange Arria 10 FPGA family was announced. Since that time, those vendors have focused on new high-end products such as Versal and Agilex while offering only minor variations in their less expensive lines.

While disclosing Avant to investors, Lattice withheld product details until next year's announcement. The new line could include products with up to 300,000 logic cells, which would top Artix 7. If Avant scales memory by a similar amount, it would match the 13Mbits of the top-end Artix 7. But Arria 10 ranges from 160,000 logic cells to 1.1 million and offers far more SRAM. These older devices use 28nm or 20nm manufacturing; we expect Lattice will jump to a more advanced node such as 14nm to reduce the cost and power of its new devices. If the company continues to employ FD-SOI, Samsung's 18FDS process is another option.

According to Lattice, Avant will include new system interfaces appropriate for midrange FPGAs. Artix features 6.6Gbps transceivers, while Arria provides 17Gbps transceivers and PCIe Gen3 controllers. Avant will omit a CPU subsystem, however, at least initially. The Arria devices all have dual Cortex-A9 CPUs; Xilinx instead offers Zynq-branded FPGAs with two or four Cortex-A53 cores and other SoC interfaces.

By delivering Avant, Lattice hopes to double its available market, adding the $2.5 billion midrange segment to the $2.2 billion low-end segment it already serves. (These market sizes are 2024 projections.) But without hard CPUs and covering only a portion of the Arria line, the initial Avant parts will target just a fraction of that new segment. Over time, however, the company could build out its new line to cover more of the midrange.

Initial Avant applications include automotive subsystems, robotics, and communications infrastructure—markets where Lattice already has many customers. These customers are familiar with the company's tools and software, which will also support the future Avant products. Thus, the new strategy should create significant growth opportunities while taking advantage of distracted competitors. ♦