MachXO5-NX Hardware Checklist

Technical Note

FPGA-TN-02274-1.0

October 2022

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AC	Alternating Current
ADC	Analog to Digital Converter
BGA	Ball Grid Array
DC	Direct Current
DLL	Delay-Locked Loop
DRR3	Double Data Rate 3
ESR	Equivalent Series Resistance
FPGA	Field-Programmable Gate Array
HCSL	High-Speed Current Steering Logic
HSUL	High-Speed Unterminated Logic
I/O	Input/Output
JTAG	Joint Test Action Group
LVDS	Low-Voltage Differential Signaling
LVSTL	Low-Voltage Swing Terminated Logic
MIPI	Mobile Industry Processor Interface
NDA	Non-Disclosure Agreement
OSC	Oscillator
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
SSTL	Stub Series-Terminated Logic
SerDes	Serializer/Deserializer

1. Introduction

When designing complex hardware using the MachXO5™-NX device, the user must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware implementation items relative to the MachXO5-NX device. The document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

The device family consists of FPGA densities ranging from 25k to 80k Logic Cells. This technical note assumes that the reader is familiar with the MachXO5-NX device features as described in MachXO5-NX Family Data Sheet (FPGA-DS-02102). The data sheet includes the functional specification for the device. Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

Refer to MachXO5-NX Family Data Sheet (FPGA-DS-02102) for details. The critical hardware areas covered in this technical note are:

- Power supplies as they relate to the MachXO5-NX power supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Important: Refer to the following documents for detailed recommendations.

- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286)
- Thermal Management (FPGA-TN-02044)
- sysDSP User Guide for Nexus Platform (FPGA-TN-02096)
- High-Speed PCB Design Considerations (FPGA-TN-02148)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02150)
- HSPICE SerDes simulation package (available under NDA, contact the license administrator at lic_admin@latticesemi.com)
- MachXO5-NX-related pinout information can be found on the Lattice website.

2. Power Supplies

At power up the V_{CC}, V_{CCAUXA}, V_{CCI01}, and V_{CCI02} power supplies are monitored to determine when the MachXO5-NX should de-assert its internal Power-On Reset state and enter Power Good condition, which starts device initialization and configuration. These supplies should come up monotonically. Other supplies are not monitored during power-up but need to be at valid and stable level before the device configuration is complete.

Table 2.1 describes the power supplies and the appropriate voltage levels for each supply.

Table 2.1. Single-Ended I/O Standards

Supply	Voltage (Nominal Value)	Description
V_{CC}	1.0 V	FPGA core power supply. Required for Power Good condition.
V_{CCECLK}	1.0 V	FPGA core clock power supply.
V_{CCAUX}	1.8 V	Auxiliary power supply pin for I/O Bank 0, Bank 1, Bank 2, Bank 3, Bank 4, Bank 7, Bank 8, and Bank 9. Used for generating stable drive current for the I/O.
$V_{CCAUXHx}$	1.8 V	Auxiliary power supply pin for I/O Bank 5, and Bank 6. Used for generating stable drive current for the I/O and stable current for the differential input comparators.
V_{CCAUXA}	1.8 V	Auxiliary Supply Voltage for internal analog circuitry. Required for Power Good condition.
$V_{CCIO[9:0]}$	Wide-Range Banks: Bank 1: 3.3 V Only Banks 0, 2, 3, 4, 7, 8, 9: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V High-Speed Banks: Banks 5, 6: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V	Bank I/O Driver Supply Voltage. Each bank has its own V_{CCIO} supply. V_{CCIO1} and V_{CCIO2} have pins used for device configuration and are required for Power Good condition.
$V_{CCADC18}$	1.8 V	ADC Block power supply. Should be isolated from excessive noise.
ADC_REFP[1:0]	1.2 V to 1.8 V Typical	ADC External Reference. Should be isolated from excessive noise and have high accuracy (< 0.1%).

2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of ±5% of these voltages. The 5% tolerance includes any noises.

2.2. Power Source

It is recommended that the designed voltage regulators are accurate to within 3% of the optimum voltage to allow power noise design margin.

When calculating the voltage regulator total tolerance, include:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to regulator's feedback pin which sets regulator's output voltage
- Expected voltage drops due to power filtering ferrite bead's ESR * expected current draw
- Expected voltage drops due to current measuring resistor's ESR * expected current draw

With 3% tolerance allocated to the voltage source, the design has a remaining 2% tolerance for noise and layout related issues. The 1.0 V rail is especially sensitive to noise as every 10 mV is 1% of the rail voltage. For PLLs, target less than 0.25% peak noise.

3. Power Supply Decoupling and Component Selection

Providing a quiet filtered supply is important for all rails and critical for the analog rails. Supplies should be decoupled with adequate power filters. Bypass capacitors must be located close to the device package pins with very short traces to keep inductance low.

For the best performance, use careful pin assignments to keep noisy I/O pins away from sensitive functional pins. The leading causes of PCB related crosstalk to sensitive blocks are related to FPGA outputs located in close proximity to the sensitive power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet filtered supplies for the analog supplies; however, robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

It is critical to have very low-noise highly-filtered supplies for the MachXO5-NX ADCs. These supplies are also paired with dedicated ground pins.

3.1. Recommended Power Filtering Groups and Components

Table 3.1. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}, V_{CCECLK}	10 µF x 2 + 100 nF per pin	Core and clock logic. Tie V_{CC} and V_{CCECLK} pins together. 1.0 V
V_{CCAUX}, $V_{CCAUXHx}$ (Single Ended)	120 Ω FB + 10 µF + 100 nF per pin	Auxiliary power supply pins. $V_{CCAUXHx}$ banks not using high-speed differential pair I/O can be tied together with V_{CCAUX} pins. 1.8 V
$V_{CCAUXHx}$ (Fast Differential)	120 Ω FB + 10 µF + 100 nF per pin	I/O Bank 5 and Bank 6, which use high-speed differential pair I/O should use a separate FB + Capacitor filter not connected with V_{CCAUX}. 1.8 V
V_{CCAUXA}	120 Ω FB + 10 µF + 100 nF per pin	Auxiliary power supply pin for internal analog circuitry 1.8 V
$V_{CCIO[9:0]}$	10 µF + 100 nF per pin for each V_{CCIOx}	Bank I/O. Unused banks can use a single 1.0 µF. For banks with lots of outputs or large capacitive loading replace the 10 µF with a 22 µF (or use two 10 µF). Bank 1: 3.3 V Only Banks 0, 2, 3, 4, 7, 8, 9: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V Banks 5, 6: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V
$V_{CCADC18}$	220 Ω or 120 Ω FB + 10 µF + 100 nF per pin	ADC Blocks. If both ADC blocks are not used, leave open. 1.8 V
ADC_REFP[1:0]	220 Ω or 120 Ω FB + 1.0 µF + 100 nF per pin	ADC Block External Reference. Must have very low noise and high accuracy reference (<= 0.1% Tolerance). Voltage source/regulator should be filtered by 220 Ω or 120 Ω FB + 1 µF If ADC block is not used, connect its ADC_REFPx to ground through 0 Ω resistor. 1.2 V to 1.8 V Typical

3.2. Unused ADC Blocks

- If both ADC blocks are unused leave $V_{CCADC18}$ open.
- Unused ADC blocks should connect ADC_REFPx to ground through 0 Ω resistor.
- V_{SSADC} pin should connected to the board's ground plane even if ADC blocks are unused.

3.3. Ferrite Bead Selection

- Most designs work well using ferrite beads between 120 Ω @100 MHz and 240 Ω @100 MHz.
- Ferrite bead induced noise voltage from ESR * CURRENT should be < 1% of rail voltage for non-analog rails and < 0.25% for sensitive rails.
- Non-PLL rails should use ferrite beads with ESR between 0.025 Ω and 0.10 Ω depending on current load.
- PLL rails draw low current, which allow ferrite beads with ESR <= 0.3 Ω.
- Small package size ferrite beads have higher ESR than large package size ferrite beads of same impedance.
- High impedance ferrite beads have higher ESR than low impedance ferrite beads in the same package size.

3.4. Ground Pins

- All ground pins need to be connected to the board's ground plane.
- V_{SSADC} pins are sensitive to noise and should be isolated from fast switching high current pathways on the ground plane. Ground plane islands can be used to help isolate sensitive grounds from noisy ground areas. The ground plane islands must connect at only one location to the main ground plane. Connection locations should be at least 2 mm wide. Only signals in the same domain as the ground plane island should be referenced to that island.

3.5. Clock Oscillator Supply Filtering

When providing an external reference clock to the FPGA from, for example, a single-ended or differential clock oscillator, proper power supply isolation and decoupling of the clock oscillator is recommended. A typical bypassing circuit is shown in Figure 3.1.

When specifying components, choose good quality ceramic capacitors in small packages, and place them as close to the clock oscillator supply pins as practically possible. *Good quality* capacitors for bypassing generally meet the following requirements:

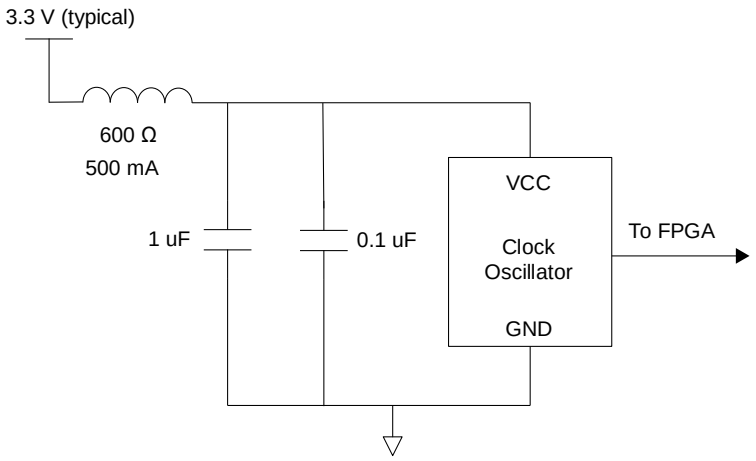

Figure 3.1. Clock Oscillator Bypassing

3.5.1. Capacitor Dielectric

Use dielectrics such as X5R, X7R, and similar which have good capacitance tolerance (<= ±20%) over temperature range. Avoid Y5V, Z5U, and similarly poor capacitance-controlled dielectrics.

3.5.2. Voltage Rating

Capacitor working capacitance decreases non-linearly with higher voltage bias. To maintain capacitance, the capacitor voltage rating should target at least 80% higher than the voltage rail (maximum). Example: 3.3 V rail bypass capacitors should use the commonly available 6.3 V rating as a minimum.

3.5.3. Size

Smaller body capacitors have lower inductance, work to higher frequencies, and improve board layout. For a given voltage rating, smaller body capacitors tend to cost more than larger body capacitors. Optimizing between market pricing and size related inductance, the following capacitor sizes are recommended:

Table 3.2. Recommended Capacitor Sizes

Capacitance	Size Preferred	Size Next Best
0.1 uF	0201	0402
1.0 uF, 2.2 uF	0402	0201
4.7 uF	0402	0603
10 uF	0402	0603
22 uF	0805	0603

4. Power

4.1. Power Sequencing

There is no power up sequence required for the MachXO5-NX device.

4.2. Power Estimation

Once the MachXO5-NX device density, package, and logic implementation is decided, power estimation for the system environment should be determined based on the Power Calculator provided as part of the Lattice Radiant® design tool. When estimating power, the designer should keep two goals in mind:

- Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current and maximum DC and AC current for the given system environmental conditions.
- Thermal considerations are also important. The thermal design of the system environment and MachXO5-NX device should be able to support operating at maximum operating junction temperature.

The above two criteria should be taken into consideration early in the design phase.

5. Configuration Considerations

PCB layout design and breakout suggestions are outlined in PCB Layout Recommendations for BGA Packages (FPGA-TN-02024). For application-specific assembly guidance, consult the design guidelines of the assembly service provider.

The MachXO5-NX device includes provisions to configure the FPGA via the JTAG interface or several modes utilizing the sysCONFIG port. The JTAG port includes a 4-pin interface. The interface requires the following PCB considerations.

Table 5.1. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
TDI/SI	10 kΩ pull-up to V_{CCIO1}
TMS/SCSN	10 kΩ pull-up to V_{CCIO1}
TDO/SO	10 kΩ pull-up to V_{CCIO1}
TCK/SCLK	2.2 kΩ pull-down to GND
JTAG_EN	4.7 kΩ pull-down to GND (JTAG port disabled) or 1.0 kΩ pull-up to V_{CCIO1} (JTAG port enabled)

Every PCB is recommended to have easy access to FPGA JTAG pins, even if the primary configuration interface is not using the JTAG port. This JTAG port enables debugging in the final system. For best results, route the TCK, TMS, TDI, and TDO signals to a common test header along with V_{CCIO2} and ground.

External resistors are necessary on configuration signals if they are used to handshake with other devices. External pull-resistors are not necessary on individual configuration pins when the signal pin is not persisted.

Recommended pull-up resistors to the appropriate bank V_{CCIO} and pull-down to board ground should be used on the pins in Table 5.2.

Table 5.2. Pull-up/Pull-down Recommendations for Configuration Pins

Pin	PCB Connection
PROGRAMN	4.7 kΩ pull-up to V_{CCIO1}
INITN	10 kΩ pull-up to V_{CCIO1}
DONE	10 kΩ pull-up to V_{CCIO1}
JTAG_EN	4.7 kΩ pull-down to GND (JTAG port disabled) or 1.0 kΩ pull-up to V_{CCIO2} (JTAG port enabled)
TMS/SCSN	10 kΩ pull-up to V_{CCIO2}
SCL/SDA*	1.0 kΩ to 4.7 kΩ pull-up to V_{CCIO2}

***Note**: Pull-up resistors are not required in Slave I3C configuration mode.

Table 5.3. Configuration Pins Needed per Programming Mode

Configuration Mode	Bank	Enablement	Clock		Bus Size	Pins
			Pin	I/O		
JTAG	1	JTAG_EN pin*	TCLK	Input	1	TCK, TMS, TDI, TDO
SSPI	1	Activation key*	SCLK	Input	1	SCLK, SCSN, SI, SO
					2	SCLK, SCSN, SD0, SD1
					4	SCLK, SCSN, SD0, SD1, SD2, SD3
I^2C/I3C	1	Activation key	SCL	Input	1	SCL, SDA

***Note**: JTAG and SSPI ports share pins. When JTAG_EN is asserted, the JTAG port takes precedence over SSPI.

6. I/O Pin Assignments

It is common practice for designers to select pinouts for their system very early in the design cycle. For the FPGA designer, this requires a detailed knowledge of the targeted FPGA device. Designers often use a spreadsheet program to initially capture the list of the design I/O. Lattice Semiconductor provides detailed pinout information that can be downloaded from the Lattice Semiconductor website in .csv format for designers to use as a resource to create pinout information. For example, by navigating to the pinout.csv file, the user can gather the pinout details for all the different package offerings of the device in the family, including I/O banking, differential pairing, Dual Function of the pins, and input and output details.

6.1. Early I/O Release

The MachXO5-NX device supports an Early I/O Release feature, which allows the I/O that reside in the I/O banks on the left and right of the device (I/O Bank 2, I/O Bank 3, Bank 4, I/O Bank 7, Bank 8, and I/O Bank 9), to assume user-defined drive states at the beginning of bitstream processing. The Early I/O Release feature releases the I/O after processing the I/O configuration for the left and right banks, which is located near the head of the bitstream data. Once data is programmed in the left/right Memory Interface Block (MIB) the I/O is released to a predefined state. This feature is enabled by setting the EARLY_IO_RELEASE preferences to ON in the Lattice Radiant Device Constraint Editor.

In addition, Early I/O Release requires you to instantiate an output buffer register with an asynchronous set or reset function, to indicate the desired drive *1* or drive *0* behavior, respectively, during the Early Release period. Unregistered outputs in Early-Release banks drive High-Z until full device configuration is complete. Be aware that some of the I/O in Bank 2, including the dual-purpose sysCONFIG I/O, cannot be utilized as Early Released I/O. Also, if the ECDSA bitstream authentication is enable for the MachXO5-NX device, the Early I/O Release feature is not supported.

7. Clock Inputs

The MachXO5-NX device provides certain pins for use as clock inputs in each I/O bank. These pins are shared and can alternately be used for General Purpose I/O.

When these pins are used for clocking purpose, the user needs to pay attention to minimize signal noise on these pins. Refer to MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286).

These shared clock input pins can be found under the Dual Function column of the pinlist .csv file.

High-speed differential interfaces (such as MIPI) being received by the FPGA must route their differential clock pair into a pair of inputs that support differential clocking, labeled PCLKTx_y (+true) and PCLKCx_y (-complement).

When providing an external reference clock to the FPGA, ensure that the oscillator's output voltage to the FPGA does not exceed the bank's voltage. For banks with V_{CCIO} voltage of 1.5 V and lower, it is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's V_{CCIO}. An LVDS oscillator can also be used if AC coupled and then DC biased at half the V_{CCIO} voltage. An example of a dual footprint design supporting HCSL and LVDS shown in Figure 7.1.

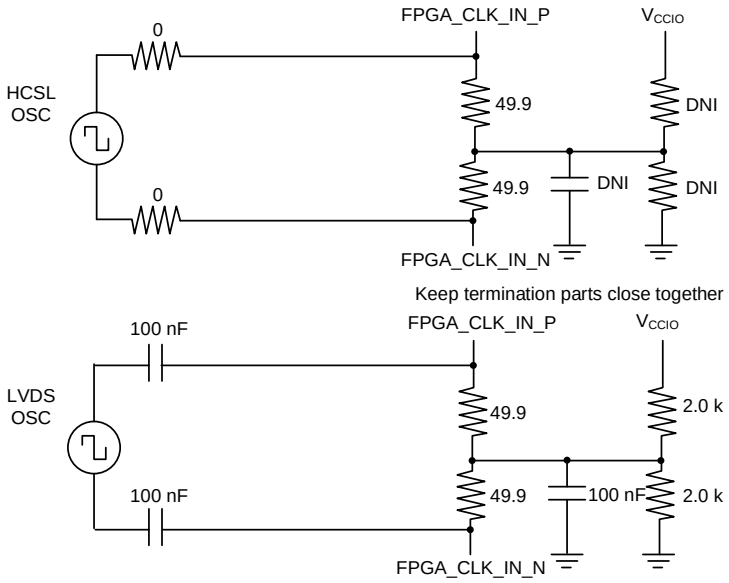

Figure 7.1. PCB Dual Footprint Supporting HCSL and LVDS Oscillators

8. Pinout Considerations

The MachXO5-NX device supports many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to implementation of the PCB design on these high-speed interfaces. The pinout selection must be completed with an understanding of the interface building blocks implemented in the FPGA fabric. These include IOLOGIC blocks such as DDR3, clock resource connectivity, and PLL and DLL usage. Avoid placing noisy I/Os next to sensitive analog I/Os. Refer to MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286) for rules pertaining to these interface types.

8.1. LVDS Pin Assignments

True LVDS outputs are available on I/O pins on the device bottom Banks 5 and 6 only. Top, left, and right side I/O banks do not support True LVDS output standard. Differential input pairing can be found in the pinlist csv file.

Emulated LVDS output are available on pairs around all banks, and requires external termination resistors. This is described in sysI/O Usage Guide for Nexus Platform (FPGA-TN-02067).

8.2. HSUL, SSTL, and LVSTL Pin Assignments

The HSUL, SSTL and LVSTL interfaces are referenced I/O standards require an external reference voltage. HSUL, SSTL and LVSTL are supported on the device bottom Banks 5 and 6 only. The V_{REF} pin(s) should get high priority when assigning pins on the PCB. These pins can be found in the Dual Function column with V_{REF} label. Each bank includes a separate V_{REF} voltage. V_{REF} sets the threshold for the referenced input buffers. Each I/O is individually configurable based on the bank supply and reference voltages.

9. DPHY Pin Considerations

High-speed signaling requires careful PCB design. Maintaining good transmission line characteristics is a requirement. A continuous ground reference should be maintained with high-speed routing. This includes tightly length matched differential routing (no larger than ±4 mil length mismatch) with very few discontinuities.

The DPHY clock input must use a PCLK pin so that it can be routed directly to the edge clock tree. Refer to High-Speed PCB Design Considerations (FPGA-TN-02178) for suggested methods and guidance. In the MachXO5-NX, the DPHY is a soft DPHY implementation.

10. Checklist

Table 10.1. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	Core Supplies		
1.1.1	V_{CC} and V_{CCECLK} core @ 1.0 V ±3% (allowing for 2% noise).		
1.1.2	Use a PCB plane for V_{CC} core with proper decoupling.		
1.1.3	V_{CC} and V_{CCECLK} core sized to meet power requirement calculation from software.		
1.1.4	V_{CCAUX}, $V_{CCAUXHx}$, and V_{CCAUXA} @ 1.8 V ±3% (allowing for 2% noise).		
1.1.5	V_{CCAUX}, $V_{CCAUXHx}$, and V_{CCAUXA} Must be *quiet* and isolated from other switching noises.		
1.1.6	V_{CCAUX} pins ganged together with $V_{CCAUXHx}$ pins for banks without high-speed differential pair I/O. Solid PCB plane is recommended.		
1.1.7	$V_{CCAUXHx}$ banks with high-speed differential pair I/O should use separate FB + Capacitor filter not connected with V_{CCAUX}. Solid PCB plane is recommended.		
1.1.8	V_{CCAUXA} pins should be ganged together and use FB + Capacitor filtering. Solid PCB plane is recommended.		
1.2	I/O Supplies		
1.2.1	*Wide Range* V_{CCIO1} 3.3 V Only.		
1.2.2	*Wide Range* V_{CCIO} (Banks 0, 2, 3, 4, 7, 8, 9) are between 1.2 V to 3.3 V.		
1.2.3	All *High Performance* (Banks 5, 6) V_{CCIO} are between 1.0 V to 1.8 V.		
1.2.4	Configuration V_{CCIO} (Banks 1, 2) match system voltages.		
1.2.5	$V_{CCIO[9:0]}$ used based on user design.		
1.3	ADC power supply		
1.3.1	$V_{CCADC18}$ is 1.8 V ±3% (allowing for 2% noise).		
1.3.2	$V_{CCADC18}$ *quiet* and *isolated*.		
1.3.3	Use accurate voltage reference for ADC_REFP[1:0] (<= ±0.1%)		
1.3.4	If both ADC blocks are unused leave VCCADC18 open.		
1.3.5	Unused ADC blocks should connect ADC_REFPx to ground through 0 Ω resistor.		
1.3.6	V_{SSADC} pin should connected to the board's ground plane even if ADC blocks are unused.		
1.4	Grounds		
1.4.1	All ground pins must be connected to low impedance ground plane.		
2	**JTAG**		
2.1	Pull-up or Pull-down on JTAG_EN, per Table 5.1.		
2.2	Keep JTAG_EN accessible on PCB to recover JTAG port, especially during development.		
2.3	Keep JTAG port pins accessible on PCB, especially during development		
2.4	Pull-down on TCK per Table 5.1.		
2.5	Pull-up on TMS per Table 5.1.		
3	**Configuration**		
3.1	Pull-ups or pull-downs on persisted configuration specific pins per Table 5.1 and Table 5.2.		
3.2	V_{CCIO1}, V_{CCIO2} bank voltage matches sysCONFIG peripheral devices such as SPI Flash		
4	**Special Pin Assignments**		
4.1	V_{REF} assignments followed for single-ended SSTL inputs		
4.2	Properly decouple the V_{REF} source		

	Item	OK	NA
5	**Critical Pinout Selection**		
5.1	Pinout is chosen to address FPGA resource connections to I/O logic and clock resources per MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286).		
5.2	Shared general purpose I/O are used as inputs for FPGA PLL and Clock inputs.		
5.3	Differential pair I/O polarity: I/O are named P[T/B/L/R] [Number]_[A/B] Diff pair positive signal connects to name ending in A, Negative connects to name ending in B.		
5.4	Differential clock inputs must use a PCLK pin so the clock input can be routed directly to the edge clock tree.		
5.5	Soft MIPI on banks 5 and 6 only.		
6	**LPDDR3 and DDR3 Interface Requirements**		
6.1	DQ, DM, and DQS signals should be routed in a data group and should have similar routing and matched via counts. Using more than three vias is not recommended in the route between the FPGA controller and memory device.		
6.2	Maintain trace length matching to a maximum of ±20 mil between any DQ/DM and its associated DQS strobe within a DQ group. Use careful serpentine routing to meet this requirement.		
6.3	All data groups must reference a ground plane within the stack-up.		
6.4	DDR trace reference must be solid without slots or breaks. It should be continuous between the FPGA and the memory.		
6.5	Provide a separation of 3 W spacing between a data group and any other unrelated signals to avoid crosstalk issues. Use a minimum of 2 W spacing between all DDR traces excluding differential CK and DQS signals. (W is the minimum width of the signal trace allowed)		
6.6	Assigned FPGA I/O within a data group can be swapped to allow clean layout. Do not swap DQS assignments.		
6.7	Differential pair of DQS to DQS_N trace lengths should be matched to ±10 mil.		
6.8	Resistor terminations (DQ) placed in a fly-by fashion at the FPGA is highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mil.		
6.9	LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±100 mil.		
6.10	Address/control signals and the associated CK and CK_N differential FPGA clock should be routed with a control trace matching ±100 mil.		
6.11	CK to CK_N trace lengths must be matched to within ±10 mil.		
6.12	Address and control signals can be referenced to a power plane if a ground plane is not available. Ground reference is preferred.		
6.13	Address and control signals should be kept on a different routing layer from DQ, DQS, and DM to isolate crosstalk between the signals.		
6.14	Differential terminations used by the CLK/CLKN pair must be located as close as possible to the memory.		
6.15	Address and control terminations placed after the memory component using a fly-by technique are highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mils.		

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, October 2022

Section	Change Summary
All	Initial release.

www.latticesemi.com