Mach-NX Hardware Checklist

Technical Note

FPGA-TN-02235-1.0

December 2020

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
I^2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LVDS	Low-Voltage Differential Signaling
PCB	Printed Circuit Board
PLD	Programmable Logic Device
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSPI	Slave Serial Peripheral Interface

1. Introduction

When designing complex hardware using the Mach-NX™ PLD, you must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware requirements related to the Mach-NX devices. This document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

The Mach-NX PLDs are low power, instant-on, Flash based devices with high integration and on-board System-on-Chip (SoC) features. This technical note assumes that the reader is familiar with the Mach-NX device features as described in the Mach-NX Family Data Sheet (FPGA-DS-02084).

The critical hardware areas covered in this technical note include:

- Power supplies as they relate to the Mach-NX supply rails and how to connect them to the PCB and the associated system.
- Configuration and how to connect the configuration mode selection for proper power up configuration.
- Device I/O interface and critical signals.

Important: Refer to the following documents for detailed recommendations.

- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- Power Estimation and Management for Mach-NX Devices
- Mach-NX sysI/O Usage Guide (FPGA-TN-02233)
- Implementing High-Speed Interfaces with Mach-NX Devices (FPGA-TN-02234)
- Mach-NX Programming and Configuration Usage Guide (FPGA-TN-02231)
- Using Hardened Control Functions in Mach-NX Devices (FPGA-TN-02222)

2. Power Supply

The V_{CC} and V_{CCIO0} power supplies determine the Mach-NX internal *power good* condition. These supplies need to be at a valid and stable level before the device can become operational. In addition, there are six (V_{CCIO1} to V_{CCIO6}) supplies that power the remaining I/O banks, and two auxiliary supplies, VCCAUX and VCCB. Table 2.1 shows the power supplies and the appropriate voltage levels for each.

Refer to the Mach-NX Family Data Sheet (FPGA-DS-02084) for more information on the voltage levels.

Table 2.1. Power Supply Description and Voltage Levels

Supply	Voltage (Nominal Value)	Description
V_{CC}	1.0 V	Core power supply
V_{CCIO0}	2.5 V or 3.3 V	Power supply pins for I/O Bank 0. banks.
V_{AUX}	1.8 V	Auxiliary power supply pin for internal analog circuitry.
V_{CCB}	1.8 V	Power supply for auxiliary core functions.
V_{CCIO1}, V_{CCIO2}, V_{CCIO5}, V_{CCIO6}	1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V	Power Supply pins for I/O Banks 1, 2, 5 and 6
V_{CCIO3}, V_{CCIO4}	1.0 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V	Power Supply pins for I/O Banks 3 and 4

2.1. Power Sequencing

There is no power-up sequence required for the Mach-NX device.

3. Power Estimation

Once the Mach-NX device density, package, and logic implementation are determined, power estimation can be performed using the Power Calculator tool, which is provided as part of the Lattice Diamond® design software. While performing power estimation, you should keep two specific goals in mind.

- Power supply budgeting should be considered based on the maximum of the power-up in-rush current, configuration current or maximum DC and AC current for a given system environmental condition.
- The ability of the system environment and Mach-NX device packaging to support the specified maximum operating junction temperature.

By determining these two criteria, system design planning can take the Mach-NX power requirements into consideration early in the design phase.

This is explained in Power Estimation and Management for Mach-NX Devices.

4. Configuration Considerations

Mach-NX devices contain two types of memory, SRAM and Flash. SRAM is volatile memory and contains the active configuration. Flash is non-volatile memory that provides on-chip storage for the SRAM configuration data. Additional external Flash memory is required for SoC configuration data and code storage, and must be connected to SoC QSPI Monitor Channel 0 (refer to the SoC section).

The Mach-NX device includes multiple programming and configuration interfaces:

- 1149.1 JTAG
- Self-download
- Slave SPI
- Dual Boot
- I²C

For ease of prototype debugging, it is recommended that every PCB should have easy access to the programming and configuration pins.

The configuration logic arbitrates access from the interfaces by the following priority. When higher priority ports are enabled, Flash access by lower priority ports will be blocked.

- JTAG Port
- Slave SPI Port (SN low activates the SPI port)
- I²C Primary Port

Note: Erased device has all programming and configuration ports enabled by default. When the device is erase ensure SN and PROGRAMN are not driven low.

For a detailed description of the programming and configuration interfaces, refer to Mach-NX Programming and Configuration Usage Guide (FPGA-TN-02231).

The use of external resistors is always needed if the configuration signals are being used to handshake with other devices. Pull-up and pull-down resistor (4.7 kΩ) recommendations on different configuration pins are listed below.

Table 4.1. Default State of the sysCONFIG™ Pins

Pin Name	Pin Function (Configuration Mode)	Pin Direction (Configuration Mode)	Default Function (User Mode)
PROGRAMN	PROGRAMN	Input with weak pull-up, external pull-up to V_{CCIO0}.	PROGRAMN
INITN	I/O	I/O with weak pull-up.	User-defined I/O
DONE	I/O	I/O with weak pull-up, external pull-up to V_{CCIO0}.	User-defined I/O
CCLK	SSPI	Input with weak pull-up.	User-defined I/O
SN	SSPI	Input with weak pull-up, external pull-up to V_{CCIO2}.	User-defined I/O
SI/SPISI	SSPI	Input	User-defined I/O
SO/SOSPI	SSPI	Output	User-defined I/O
CSSPIN	I/O	I/O with weak pull-up, external pullup to V_{CCIO2}.	User-defined I/O
SCL	I²C	Bi-Directional open drain, external pull-up.	User-defined I/O
SDA	I²C	Bi-Directional open drain, external pull-up.	User-defined I/O
TDI	TDI	Input with weak pull-up.	TDI
TDO	TDO	Output with weak pull-up.	TDO
TCK	TCK	Input. Recommended 4.7 kΩ pull-down.	TCK
TMS	TMS	Input with weak pull-up.	TMS
JTAGENB	I/O	Input with weak pull-down.	I/O

5. SoC

5.1. Platform Firmware Resiliance (PFR) Application

The SoC supports PFR applications. Supported hardware configurations and external circuits are described in Mach-NX PRF and SoC Architecture User Guide (FPGA-TN-02230).

5.2. External SPI Flash

External Flash memory is required for SoC configuration data and firmware storage, and must be connected to SoC QSPI Monitor Channel 0. Ensure that the external SPI Flash V_{CC} and the Mach-NX V_{CCIO0} are at the same level. Ensure that the SPI Flash V_{CC} is at the recommended operating level.

QSPI Moniitor Channel 0 can be connected in either SPI or QSPI mode. See Table 5.1, below. After SoC configuration, the QSPI_Monitor Channel 0 is used by the SoC for SPI/QSPI bus monitoring.

Table 5.1. SoC Configuration Pin Connection

Pin Name	Pin Function (Configuration Mode)	Pin Direction (Configuration Mode)	Pin Function (Monitor Mode)
QSPI_MON0_CLK	Clock	Output	QSPI_MON0_CLK
QSPI_MON0_CSN	Chip Select	Output	QSPI_MON0_CSN
QSPI_MON0_DQ0	MOSI/SIO0	Input	QSPI_MON0_DQ0
QSPI_MON0_DQ1	MISO/SIO1	Output/Input	QSPI_MON0_DQ1
QSPI_MON0_DQ2	SIO2	Input	QSPI_MON0_DQ2
QSPI_MON0_DQ3	SIO3	Input	QSPI_MON0_DQ3

6. PROGRAMN Initial Power Considerations

The Mach-NX PROGRAMN is permitted to become a general purpose I/O. The PROGRAMN only becomes a general purpose I/O after the configuration bitstream is loaded. When power is applied to the Mach-NX device, the PROGRAMN input performs the PROGRAMN function. It is critical that any signal input to the PROGRAMN have a high-to-low transition period that is longer than the V_{CC} (min) to INITN rising edge time period. Transitions faster than this time period prevent the Mach-NX device from becoming operational. Refer to the description of PROGRAMN in Mach-NX Programming and Configuration Usage Guide (FPGA-TN-02231).

7. Pinout Considerations

The Mach-NX PLDs support many applications with high-speed interfaces. These include various rule-based pin-outs that need to be understood prior to the implementation of the PCB design. The pin-out selection must be completed with an understanding of the interface building blocks of the FPGA fabric. These include IOLOGIC blocks such as DDR, clock resource connectivity, and PLL usage. Refer to Implementing High-Speed Interfaces with Mach-NX Devices (FPGA-TN-02234) for rules pertaining to these interface types.

7.1. Clock Inputs

The Mach-NX device provides certain pins for use as clock inputs in each I/O bank.These pins are shared and can alternately be used for General Purpose I/O.

When these pins are used for clocking purpose, you need to pay attention to minimize signal noise on these pins. Refer to Implementing High-Speed Interfaces with Mach-NX Devices (FPGA-TN-02234).

These shared clock input pins can be found under the Dual Function column of the pinlist csv file.

8. True-LVDS Output Pin Assignments

True-LVDS outputs are on Bank 0 of the Mach-NX devices. When using the LVDS outputs, a 2.5 V or 3.3 V supply needs to be connected to the Bank 0 V_{CCIO} supply rails. Refer to Mach-NX sysI/O Usage Guide (FPGA-TN-02233) for more information.

9. Back Leakage Considerations

When the part is powered down, there are some situations where current is still present due to active I/O, similar to a hot socketing situation. This can potentially cause the internal voltage supply to rise to power-on reset levels and start device operation. To mitigate for this back leakage current, it is recommended to add a weak pulldown resistor to the voltage supply. This should be set to value sufficient to keep the voltage below the POR trip point of the device with the worst case I/O back leakage current applied.

10. Checklist

	Mach-NX Hardware Checklist Item	OK	N/A
1	Power supply		
1.1	Core supply VCC at 1.0 V		
1.2	I/O power supply VCCIO0 at 2.5 V or 3.3 V		
1.3	Auxiliary power supplies V_{AUX} and V_{CCB} at 1.8 V		
1.4	I/O power supplies V_{CCIO1}, V_{CCIO2}, V_{CCIO5}, V_{CCIO6} at 1.2 V to 3.3 V		
1.5	I/O power supplies V_{CCIO3}, V_{CCIO4} at 1.0 V to 1.8 V		
1.6	Power estimation		
2	Configuration		
2.1	Configuration options		
2.2	Pull-up on PROGRAMN, INITN, DONE		
2.3	Pull-up on SSPI mode pins		
2.4	Pull-up on I^2C mode pins		
2.5	JTAG default logic levels		
2.6	PROGRAMN high-to-low transition time period is larger than the VCC (min) to INITN rising edge time period		
3	SoC External SPI flash		
4	I/O pin assignment		
4.1	True LVDS pin assignment considerations		

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, November 2020

Section	Change Summary
All	Initial release.

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