Lattice Radiant Software Known Issues

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Type Conventions Used in This Document

Convention	Meaning or Use
Bold	Items in the user interface that you select or click. Text that you type into the user interface.
<*Italic*>	Variables in commands, code syntax, and path names.
Ctrl+L	Press the two keys at the same time.
`Courier`	Code examples. Messages, reports, and prompts from the software.
`...`	Omitted material in a line of code.
`.` `.` `.`	Omitted lines in code and report examples.
`[ ]`	Optional items in syntax descriptions. In bus specifications, the brackets are required.
`( )`	Grouped items in syntax descriptions.
`{ }`	Repeatable items in syntax descriptions.
`|`	A choice between items in syntax descriptions.

Contents

Lattice Radiant Software Known Issues

This section lists the known issues and workarounds of the Radiant software. Descriptions include the software versions and devices affected. If you are looking for a workaround to a problem, search for related terms including the tool name or a word from an error message, or scan the Contents. If you want issues for a certain version, search for the version number. This will find issues affecting that version and issues fixed in that version of the software.

Design Entry

Radiant software main window stops working on Windows 10 when Dell Backup and Recovery software is installed

When Dell Backup and Recovery software is installed, it conflicts with the Radiant software, and may cause it to stop working.
Workaround: Uninstall Dell Backup and Recovery software.

Versions affected: 1.0
Fixed: 1.1
Devices affected: All
Bug number: DNG-2303

IP Catalog

DPHY derating for CrossLink-NX does not work

For assistance with this issue, please contact Lattice Technical Support.
Versions affected: 2.0, 2.0 SP1
Fixed: 2.1
Devices affected: CrossLink-NX
Bug number: DNG-8247

After enabling IP Evaluation, an error message stating License Checkout Failed appears when generating bitstream

Workaround: Click OK on the error message. Bitstream generation should continue as normal.
Versions affected: 2.0, 2.0 SP1
Fixed: 2.1
Devices affected: All
Bug number: DNG-8932

If PLL IP is regenerated, a warning icon still appears.

After PLL IP is regenerated to the latest version based on a warning icon, the warning icon still appears beside the regenerated IPX file in the File List window > Input Files.
Workaround: Ignore the warning icon after regeneration.
Versions affected: 2.0, 2.0 SP1
Fixed: 2.1
Devices affected: All
Bug number: DNG-8948

Radiant software 1.0 Foundation IP can pass Radiant software 2.0 SP1 flow but can't be regenerated with R2.0 SP1 IP Catalog.

Workaround: In Radiant 2.0 SP1 Release Notes, refer to "Migrating IPs" section of "Updating Projects from an Earlier Version".
Versions affected: 2.0, 2.0 SP1
Fixed 2.1
Devices affected: iCE40UP
Bug number: DNG-8955

When generating PLL, calculations are not performed automatically. User must click “Calculate” button before generating PLL.

- When using the Radiant IP Catalog graphical user interface, if the Calculate button is not clicked before generating PLL, the PLL analog parameter values in the RTL will be incorrect. This affects all designs using PLL, such as GDDR 7:1 Receive Interface and GDDR with enabled PLL instantiation.

  Workaround: For configurations that use PLL, click the "Calculate" button before clicking the “Generate” button.

- If the ipgen command is used to generate PLL, the PLL analog parameter values in the RTL will be incorrect. This affects all designs using PLL, such as GDDR 7:1 Receive Interface and GDDR with enabled PLL instantiation.

  Workaround: For configurations that use PLL, the PLL must be manually generated using the Radiant IP Catalog graphical user interface. Click the “Calculate” button before clicking the “Generate” button.

Devices affected: CrossLink-NX
Versions affected: 2.0
Fixed: 2.0 SP1
Bug number: DNG-8701

For the Soft MIPI TX mode, the B side result of clock and data are wrong

For assistance with this issue, please contact Lattice Technical Support.
Versions affected: 2.0
Fixed: 2.0 SP1
Devices affected: CrossLink-NX
Bug number: DNG-8199, DNG-8640

Simulation

ActiveHDL crashes or errors out unexpectedly with syn.vo file for LSE flow

In some cases, ActiveHDL will crash when trying to compile the syn.vo file and cause whole compile flow failure.
For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX
Versions affected: 2.1
Bug number: DNG-8143

When simulating Generic DDR, there may be a mismatch in the RTL and post-route simulation. Silicon is not affected.

For assistance with this issue, please contact Lattice Technical Support.
Devices affected: CrossLink-NX, Certus-NX
Versions affected: 2.1
Bug number: DNG-9639

When using Aldec Active-HDL the RTL simulation of DLLDEL will output 'x' for VHDL DDR case when the clk < 100Mhz

Workaround: Initialize clk signal as 1'b1 in the test bench and toggle the other signal after a delay of 20 ns.
Versions affected: 2.0, 2.0 SP1
Fixed: 2.1
Devices affected: CrossLink-NX
Bug number: DNG-8401

Constraints Views

Some IO constraints may not work as expected when designed with SystemVerilog

For assistance with this issue, please contact Lattice Technical Support.
Devices affected: CrossLink-NX, Certus-NX
Versions affected: 2.1
Bug number: DNG-9019

For QFN72 package, the SSO data of LVCMOS18 with SLOW SLEWRATE is not correct (too high).

For assistance with this issue, please contact Lattice Technical Support.
Devices affected: CrossLink-NX
Versions affected: 2.0
Fixed: 2.1
Bug number: DNG-8378

Floorplan View: When using the left mouse button to zoom while objects are selected, the selected objects will be lost

Workaround: If there are objects selected, zoom using the wheel mouse button or keys Ctrl + and Ctrl – keys
Versions affected: 1.0

Fixed: 1.1
Devices affected: All
Bug number: DNG-3231.

Timing Constraint Editor: It is not possible to drag and drop objects from RTL view into the Timing Constraint Editor while in Detach mode on certain computers

Workaround: If you run into this issue, use “Attach” mode to drag and drop objects from RTL view into the Timing Constraint Editor.
Versions affected: 1.0
Fixed: 1.1
Devices affected: All
Bug number: DNG-2728

Synthesis

For SystemVerilog designs using LSE, synthesis fails when “default_nettype” is set to none

Workaround: Attempt one of the following:

- Do not set “default_nettype none” in RTL.
- Set the top level unit as follows: In Radiant, choose **Project > Active Implementation > Set Top-level Unit.**

Devices affected: CrossLink-NX, Certus-NX
Versions affected: 2.1
Bug number: DNG-9710

When Synplify Pro is used for SystemVerilog based designs, some cases may fail when Reveal is inserted

For assistance with this issue, please contact Lattice Technical Support.
Devices affected: CrossLink-NX, Certus-NX
Versions affected: 2.1
Bug number: DNG-9103

Post-syn fails when using Reveal with soft IP ROM

Workaround: If you need to use Reveal with soft-IP ROM, then the data width of the ROM should be no more than 18 bits.
Versions affected: 2.0
Fixed: 2.0 SP1
Devices affected: CrossLink-NX
Bug number: DNG-8627

Lattice Synthesis Engine (LSE) does not implement async mult

LSE does not implement async mult. LSE always uses MAC16.
Versions affected: 1.1
Fixed: 2.0
Devices affected: All
Bug number: DNG-3144

The syn_useioff attribute does not work for LSE

This attribute controls selective register to be pack into I/O pad cell based on timing requirements. LSE "Use IO Registers" Strategy option is set to Auto to use IO registers whenever applicable. Those IO register inferences cannot be individually prevented by the user HDL attribute “syn_useioff = 0”.

Versions affected: 1.0, 1.1
Fixed: 2.0
Devices affected: All
Bug number: DNG-3382
Workarounds (2 options):

1. Use the global option "Use IO Registers = False" in Strategy Manager if the design permits, in which LSE will not pack any register into I/O pad cell unless instantiated.
2. Use Synplify Pro for Lattice synthesis tool

No warning message issued by Synplify Pro when Synplify encryption key is missing

When the encrypted design without a valid key is not be synthesized by Synplify Pro, it should provide a warning message. Note that the encrypted design will still be protected.

Versions affected: 1.1
Fixed: 2.0
Devices affected: All
Bug number: DNG-5300

For designs with multiple assignments to same parameter, Synplify Pro synthesis will pick up the first assignment without any warning message. Users may get unexpected results

Workaround: Remove any unused assignments and keep the ones with the expected value.
Versions affected: 1.0

Fixed: 1.1
Devices affected: All
Bug number: DNG-2077

LOC attribute does not work for locating registers for Synplify Pro synthesis

Workaround: Use “ldc_set_location” constraint in .pdc file to set location constraints for registers.
Versions affected: 1.0
Fixed: 1.1
Devices affected: All
Bug number: DNG-2767

Implementation Flow

MAP incorrectly reports number of DPHY and PCIE/ADC resources for CrossLink-NX QFN72 package.

For assistance with this issue, please contact Lattice Technical Support.
Versions affected: 2.0, 2.0 SP1, 2.1
Devices affected: CrossLink-NX
Bug number: DNG-8297

NVCM Boot time fluctuates when Osc frequency range strategy setting is set to 'Fast'

Workaround: Use ‘Medium’ setting.
Versions affected: 2.0, 2.0 SP1
Fixed: 2.1
Devices affected: iCE40UP
Bug number: DNG-6499

PCLKDIV doesn't work without DCS

Work around: The DCS is required for PCLKDIV. The PCLKDIV output drives the CLK0 port of DCS and SEL port of DCS must be tied to GND.
Versions affected: 2.0, 2.0 SP1
Fixed: 2.1
Devices affected: CrossLink-NX
Bug number: DNG-8991

MAP does not report correct number of SEIO33 I/Os when sysCONFIG pins are used, and this can cause a resource violation

Workaround: In Radiant software, when enabling sysCONFIG pins in an LIFCL device, you need to set ldc_prohibit constraints on the sysCONFIG pins.
For example:
If you set JTAG_PORT = ENABLE, you need to prohibit usage of 4 JTAG pads: TDI, TCK, TMS, TDO. Those 4 pads are E12, F12, E13, E11 in LIFCL-40 CSBGA289 package.
So, add the following constraints in the design:

{noformat}
ldc_prohibit -site E12
ldc_prohibit -site F12
ldc_prohibit -site E13
ldc_prohibit -site E11
{noformat}

Versions affected: 2.0
Fixed: 2.0 SP1
Devices affected: CrossLink-NX
Bug number: DNG-8636

Place & Route (PAR): Some designs may encounter long run times

Versions affected: 1.0
Fixed: 1.1
Devices affected: All
DNG-3007
Workaround: Turn off the Place & Route Design Strategy “Path-based Placement” option.

Timing Analysis

PLL output is always 0 with advdataflow and dbg option for Active-HDL and Riviera

Workaround: Don’t use options advdataflow and dbg to run simulation with Active-HDL.
Versions affected: 2.0
Fixed: 2.0 SP1
Devices affected: CrossLink-NX
Bug number: DNG-7752

Hold Time calculation shows user speed grade for setup and hold calculation.

The timing engine uses the user speed grade for both setup and hold calculation. This is not the behavior users of Diamond software are expecting. Future versions of Radiant software will change this behavior to do setup calculation at the user speed grade and hold calculation at the M speed grade.

Versions affected: 1.1
Fixed: 2.0
Devices affected: All
Bug number: DNG-5651

If there are overlapping set_clock_uncertainty constraints, the most constraining one will be honored by the Timing engine

Here is an example of the issue:

```
set_clock_uncertainty 1.33 -from [get_clocks myclk1] -to [get_-
clocks myclk2] –setup

set_clock_uncertainty 3.0 [get_clocks myclk2] -setup
```

In the case above, 3.0 will be applied as the constraint.

Versions affected: 1.0
Fixed: 1.1
Devices affected: All
Bug number: DNG-2761
Workaround: None. This limitation will be reviewed and addressed in future version.

Programming

Programmer software may not work properly if you open two or more Radiant software projects at the same time

When two Radiant software projects are opened at the same time with only one using the imported .xcf file, the Programmer software may not operate properly. Clicking on the Programmer icon for the first project opens the .xcf file. If you subsequently click on the programmer icon of the second project, the Programmer will close the first .xcf file and open the second. The second .xcf file will be empty and Programmer will show an error message.
Workaround: If you need two Radiant software projects opened at the same time, close the first Radiant software project before clicking on the programmer icon of the second project.

Versions affected: 1.0
Fixed: 1.1
Devices affected: All
DNG-2915

Other Topics

Tutorial project source files embedded in Radiant 2.0 software for CrossLink-NX Tutorial are incorrect and cause a synthesis error.

Workaround: Use updated tutorial project source files. A .zip file containing updated tutorial project source files can be downloaded from here:

https://www.latticesemi.com/view_document?document_id=52825

The updated tutorial can be downloaded from here:

https://www.latticesemi.com/view_document?document_id=52757

Versions affected: 2.0
Fixed: 2.0 SP1
Devices affected: CrossLink-NX
Bug number: DNG-8739

Revision History

The following table gives the revision history for this document.

Date	Version	Description
06/22/2020	2.1	Added new known issues for Radiant 2.1. Listed previous known issues that have been resolved
03/12/2020	2.0 SP1	Added new known issues for Radiant 2.0 SP1. Listed previous known issues that have been resolved
12/17/2019	2.0	Added new known issues for Radiant 2.0. Listed previous known issues that have been resolved
04/08/2019	1.1	Added new known issues for Radiant 1.1. Listed previous known issues that have been resolved
02/14/2018	1.0	Initial Release.