CrosslinkPlus Qualification Summary

Lattice Document # MS-200071 January 2021

TABLE OF CONTENTS

1.0 INTRODUCTION ... 3

Table 1.0.1 CrossLinkPlus Product Family Attributes ... 4

2.0 LATTICE PRODUCT QUALIFICATION PROGRAM ... 5

Figure 2.0.1 Lattice Standard Product Qualification Process Flow ... 6

Table 2.0.1 Typical Qualification Tests for Components in Non-Hermetic Packages ... 8

3.0 QUALIFICATION DATA CROSSLINKPLUS PRODUCT FAMILY ... 9

3.1 CrossLinkPlus Product Family Life (HTOL) Data ... 9

Table 3.1.1 CrossLinkPlus Product Family Life Results ... 9

3.2 CrossLinkPlus Product Family – ESD and Latch Up Data ... 10

Table 3.2.1 CrossLinkPlus ESD-HBM Data ... 10

Table 3.2.2 CrossLinkPlus ESD-CDM Data ... 10

Table 3.2.3 CrossLinkPlus I/O Latch Up >100mA @ HOT (105°C) Data ... 11

Table 3.2.4 CrossLinkPlus Vcc Latch Up >1.5X @ HOT (105°C) Data ... 11

3.3 Non-Volatile Low Temperature Data Retention (LTDR) ... 12

Table 3.3.1 CrossLinkPlus LTDR Results ... 12

3.4 Non-Volatile Post-Cycle High Temperature Data Retention (PCHTDR) ... 13

Table 3.3.1 CrossLinkPlus PCHTDR Results ... 13

3.5 Accelerated Soft Error Rate (ASER) ... 14

Table 3.3.1 40LP-SA (40nm) SER ... 14

4.0 PACKAGE QUALIFICATION DATA FOR CROSSLINKPLUS PRODUCT FAMILY ... 15

Table 4.0.1 Summary of Package Reliability Test Results ... 15

4.1 Surface Mount Preconditioning Testing ... 16

Table 4.1.1 Surface Mount Precondition Data ... 16

4.2 Temperature Cycling (TC) ... 17

Table 4.2.1 Temperature Cycling Data ... 17

4.3 Steady-State Temperature Humidity Bias Life Test (THB) ... 18

Table 4.3.1 THB Data ... 18

4.4 Steady-State Unbiased Temperature Humidity Life Test (TH) ... 19

Table 4.4.1 TH Data ... 19

4.5 High Temperature Storage Life (HTSL) ... 20

Table 4.5.1 High Temperature Storage Life Data ... 20

5.0 REVISION HISTORY ... 21

Table 6.0.1 CrossLinkPlus Product Family Qualification Summary Revisions ... 21

1.0 INTRODUCTION

CrossLinkPlus™ from Lattice Semiconductor is a programmable video bridging device that supports a variety of protocols and interfaces for mobile image sensors and displays. The device is based on Lattice FPGA 40nm technology. It combines the extreme flexibility of an FPGA with the low power, low cost and small footprint of an ASIC.

CrossLinkPlus supports video interfaces including MIPI® DPI, MIPI DBI, CMOS camera and display interfaces, OpenLDI, FPD-Link, FLATLINK, MIPI D-PHY, MIPI CSI-2, MIPI DSI, SLVS200, SubLVDS, HiSPi and more.
Lattice Semiconductor provides many pre-engineered IP (Intellectual Property) modules for CrossLinkPlus. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

The Lattice Diamond® design software allows large complex designs to be efficiently implemented using CrossLinkPlus. Synthesis library support for CrossLinkPlus devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the CrossLinkPlus device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Interfaces on CrossLinkPlus provide a variety of bridging solutions for smart phone, tablets, wearables, VR, AR, Drone, Smart Home, HMI as well as adjacent ISM markets. The device is capable of supporting high-resolution, high-bandwidth content for mobile cameras and displays at 4k UHD and beyond.

This report details the Commercial/Industrial reliability qualification results of the Lattice CrossLinkPlus Product Family.

Table 1.0.1 CrossLinkPlus Product Family Attributes

Part Attributes	LIF-MDF6000 64UCFBGA
Die Fabrication Site	USJC
Package Assembly Site	ASE Kaohsiung
Final Test Site	ASE Kaohsiung
Die Family (Product Line)	CrossLinkPlus
Wafer Size	300mm
Fabrication Process Technology	40LP-SA (40nm CMOS)
Die Channel Length	Min 40nm
Number of Mask Steps	45
Die Size (W x L x T) (µm)	2899x2899x300
Die Metallization	Cu
# of Metallization Layers	9
Die Interlevel Dielectric	IMD 1-5 – uLK, IMD 6-7 – LowK, IMD 8-9 - TEOS
Die Passivation	PSG/SiN
Passivation Thickness	PSG – 4000 Å, SiN - 5000 Å
Die Preparation/Singulation	Laser Groove + Wafer Saw
Package Type / Pin Count	UCFBGA / 64
Package Size (mm)	3.5x3.5
Mold Compound Supplier/ID	Sumitomo
Mold Compound Type	G311SAC
Flammability Rating	V-0
Fire Retardant Type/Composition	Metal Hydroxide
Bump Composition	Cu Pillar + SnAg1.8
UBM	Ti/Cu
Repassivation Material	Polyimide
Bump Diagram	ABD-190069(A)
Substrate Thickness	0.242 mm
# of Substrate Metal Layers	4
Substrate Panel Singulation Method	Saw singulation
Solder Ball Composition	SAC1205
Solder Ball Diameter	0.250mm
Solder Ball Pitch	0.4mm
Operating Supply Voltage Range	1.14-1.26 V
Operating Temperature Range, Ta	-40°C to +85°C
Operating Frequency Range	(see datasheet)
LUTs	5936
sysMEM Blocks (9kb)	20
Embedded Memory (kb)	180
Distributed RAM Bits (kb)	47
General Purpose PLL	1
Embedded I2C	2
Oscillator (10KHz)	1
Oscillator (48KHz)	1
Hardened MIPI D-PHY	2*
I/O	29
Core Voltage	1.2V

* Additional D-PHY Rx interfaces are available using programmable I/O

2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Lattice Semiconductor's Reliability Monitor Program Procedure (Doc. 101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. 100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. 100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8D process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in Failures in Time (FIT). Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

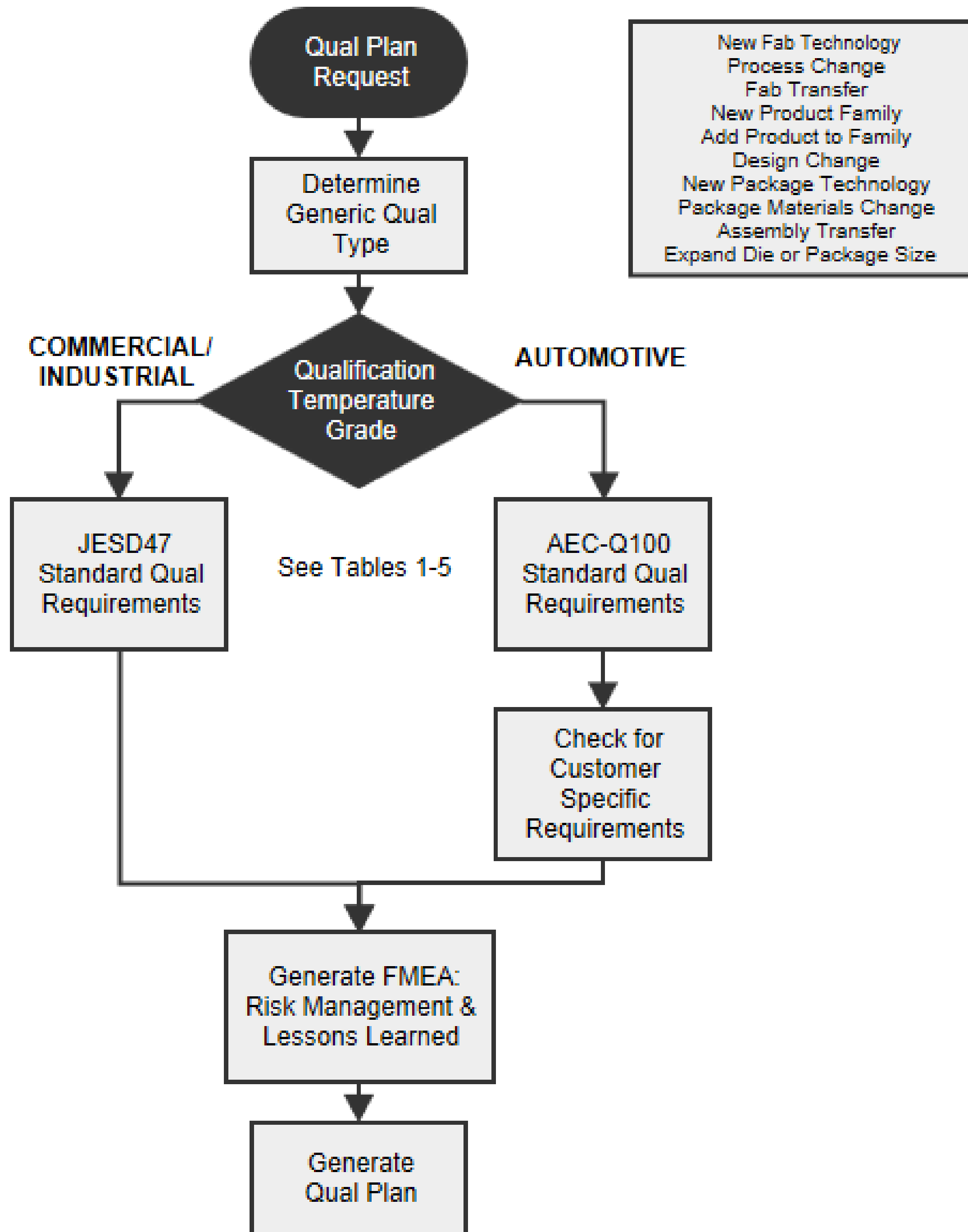
Product families are qualified based upon the requirements outlined in Table 2.0.1. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

The ECP5, CrossLink, and CrossLinkPlus families are all 40nm technology-based product offerings that leverage the same silicon design blocks, wafer fabrication design rules, bills of materials, and assembly processes & test sites. Therefore, the CrossLinkPlus FPGA product family qualifications are based on a combination of device specific qual data and family generic qual data as per the Lattice Semiconductor Qualification Procedure, Doc. 100164.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at Product Reliability Monitor Report.

Figure 2.0.1 Lattice Standard Product Qualification Process Flow

This diagram represents the standard qualification flow used by Lattice to qualify new Product Families. The target end market for the Product Family determines which flow options are used. The CrossLinkPlus Product Family was qualified using the Commercial / Industrial Qualification Option.



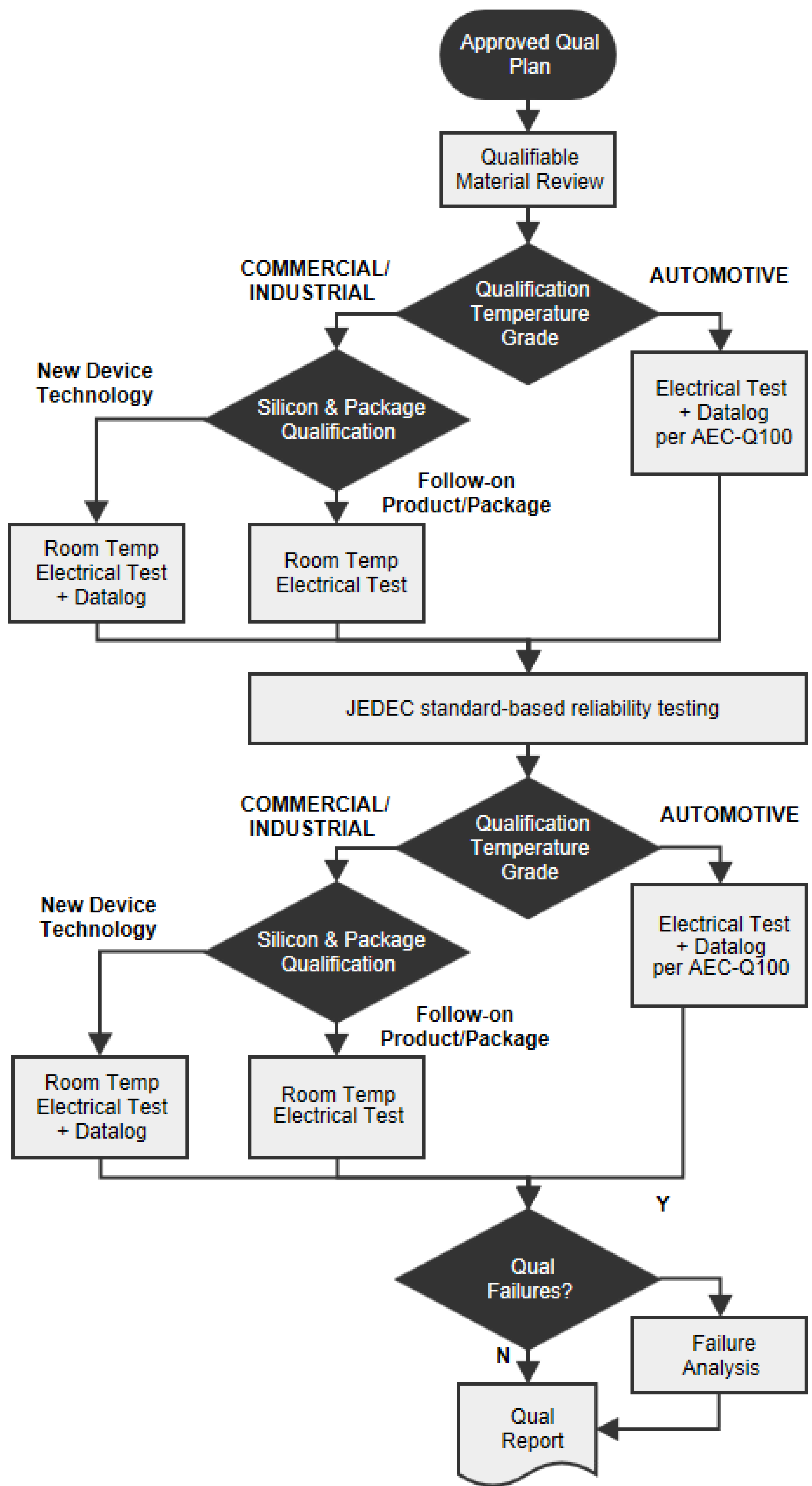

Approved Qual Plan
Qualifiable Material Review
COMMERCIAL/ INDUSTRIAL
Qualification Temperature Grade
AUTOMOTIVE
New Device Technology
Silicon & Package Qualification
Electrical Test + Datalog per AEC-Q100
Follow-on Product/Package
Room Temp Electrical Test + Datalog
Room Temp Electrical Test
JEDEC standard-based reliability testing
COMMERCIAL/ INDUSTRIAL
Qualification Temperature Grade
AUTOMOTIVE
New Device Technology
Silicon & Package Qualification
Electrical Test + Datalog per AEC-Q100
Follow-on Product/Package
Room Temp Electrical Test + Datalog
Room Temp Electrical Test
Y
Qual Failures?
N
Failure Analysis
Qual Report

Table 2.0.1 Typical Qualification Tests for Components in Non-Hermetic Packages

TEST	STANDARD	TEST CONDITIONS
High Temperature Operating Life (HTOL)	JESD22-A108	≥125°C Tj and max operating supplies
Non-Volatile Low Temperature Data Retention (LTDR)	JESD22-A117	Max Spec Cycles + Dynamic Read Accesses
Non-Volatile Post-Cycle High Temperature Data Retention (PCHTDR)		Max Spec Cycles + 125C Bake
ESD: Human Body Model (HBM)	JS-001-2014	25°C (Technology/Device dependent Performance Targets)
ESD: Charged Device Model (CDM)	JS-002-2014	25°C (Technology/Device dependent Performance Targets)
Latch-Up (LU)	JESD78	Class II, +/-100mA trigger current and AMR operating supplies
Accelerated Soft Error Testing (ASER)	JESD89	25°C, Nominal operating supplies
Surface Mount Pre-conditioning (SMPC)	IPC/JEDEC J-STD-020 JESD-A113	Per appropriate MSL level per J-STD-020
High Temp Storage Life (HTSL)	JESD22-A103	Condition B
Temperature Cycling (TC)	JESD22-A104	Condition B, soak mode 2 (typical)
Temperature Humidity Bias, THB (85/85)	JESD22-A101	85°C/85%RH, max operating supplies
Unbiased Temperature/Humidity (TH)	JESD22-A101 JESD22-A118	85°C/85%RH

3.0 QUALIFICATION DATA CROSSLINKPLUS PRODUCT FAMILY

CrosslinkPlus is fabricated at USJC using 40nm technology and assembled/tested at Advanced Semiconductor Engineering, Kaohsiung (ASEK). The LIF-MDF6000-UMG64 is the lead product qualification vehicle for this family.

Product Family: LIF-MDF6000
Packages offered: ucfBGA
Process Technology Node: 40 nm

3.1 CrossLinkPlus Product Family Life (HTOL) Data

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with EIA/JESD22-A108E "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

CrossLinkPlus Life Test (HTOL) Conditions:
Stress Duration: 1000 hours
Stress Conditions:

- Lots #1-2
  - HTOL Pattern, Vcc=1.26V, Vccio=2.625/3.465V, VccAux=3.465V, $T_{JUNCTION}$ = $\geq$125°C
- Lots #3-4
  - HTOL Pattern, Vcc=1.32V, Vccio=2.75/3.63V, VccAux=3.63V, $T_{JUNCTION}$ = $\geq$125°C

Method: EIA/JESD22-A108E

Table 3.1.1 CrossLinkPlus Product Family Life Results

Product Name	Foundry	Lot #	Qty	0 Hrs Result	0.5 Hrs Result	1000 Hrs Result	Cumulative Hours
LIF-MDF6000	USJC	1	100	0	0	0	100,000
		2	100	0	0	0	100,000
		3	99	0	0	0	99,000
		4	100	0	0	0	100,000
		Total	399	0	0	0	399,000

3.2 CrossLinkPlus Product Family – ESD and Latch Up Data

Electrostatic Discharge-Human Body Model

CrossLinkPlus product family was tested per the JS-001-2014 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure.

All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.1 CrossLinkPlus ESD-HBM Data

Product	64 ucfBGA (3.5.5x.3.5mm^2, 0.4mm pitch)
LIF-MDF6000	HBM ≥ 2kV Class 2

HBM classification for Commercial/Industrial products per JS-001-2014.
All HBM levels indicated are dual-polarity (±).

Electrostatic Discharge-Charged Device Model:

CrossLinkPlus product family was tested per the JESD22-C101F, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure.

All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.2 CrossLinkPlus ESD-CDM Data

Product	64 ucfBGA (3.5.5x.3.5mm^2, 0.4mm pitch)
LIF-MDF6000	CDM ≥1kV Class C3

CDM classification for Commercial/Industrial products, per (A) EIA/JESD22-C101E, (B) also passing 750V on corner pins, 500V on all other pins per AEC-Q100-011C1 C4B; All others, passing per EIA/JESD22-C101F.
All CDM levels indicated are dual-polarity (±).

Latch-Up:

CrossLinkPlus product family was tested per the JESD78D IC Latch-up Test procedure.

All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.3 CrossLinkPlus I/O Latch Up >100mA @ HOT (105°C) Data

Product	64 ucfBGA (3.5.5x.3.5mm^2, 0.4mm pitch)
LIF-MDF6000	> ±100mA ClassII

I-Test LU classification for Commercial/Industrial products, per JESD78D.
All IO-LU levels indicated are dual-polarity (±).
IO-LU worst-case performance is the package with access to the most IOs. All other packages for a given product are qualified-by-similarity (QBS).

Table 3.2.4 CrossLinkPlus Vcc Latch Up >1.5X @ HOT (105°C) Data

Product	64 ucfBGA (3.5.5x.3.5mm^2, 0.4mm pitch)
LIF-MDF6000	> 1.5x Vcc ClassII

Vsupply Over-voltage Test LU classification for Commercial/Industrial products, per JESD78D.
Vcc-LU worst-case performance is the package with access to the most individual power rails. All other packages for a given product are qualified-by-similarity (QBS).

3.3 Non-Volatile Low Temperature Data Retention (LTDR)

Non-Volatile Cycling Endurance (NVCE) + Low Temperature Data Retention (LTDR) are used to assess the electrical lifetime of the device's non-volatile memory array. NVCE performs program/erase cycles up to specification max cycles. LTDR performs a dynamic read-access and verify of cycled memory elements to check for charge loss associated with read conditions or mechanisms that may recover at high-temperature.

CrossLinkPlus NVCE+LTDR Conditions:

Program/Erase Cycle Count: 250

Program/Erase Temperature: Room Ambient
Stress Duration: 500 hours
Stress Conditions: Functional Pattern Read & Verify, $T_{Ambient}$ = ~25°C
Method: JESD22-A117

Table 3.3.1 CrossLinkPlus LTDR Results

<table>
<tr><th>Product Name</th><th>Foundry</th><th>Lot #</th><th>Qty</th><th>NVCE Result</th><th>500 Hrs Result</th><th>Cumulative Hours</th></tr>
<tr><td rowspan="5">LIF-MDF6000</td><td rowspan="5">USJC</td><td>1</td><td>37</td><td>0</td><td>0</td><td>18,500</td></tr>
<tr><td>2</td><td>40</td><td>0</td><td>0</td><td>20,000</td></tr>
<tr><td>3</td><td>39</td><td>0</td><td>0</td><td>19,500</td></tr>
<tr><td>4</td><td>40</td><td colspan="3">Q2, 2021</td></tr>
<tr><td>Total</td><td>116</td><td>0</td><td>0</td><td>58,000</td></tr>
</table>

3.4 Non-Volatile Post-Cycle High Temperature Data Retention (PCHTDR)

Non-Volatile Cycling Endurance (NVCE) + Post-Cycle High Temperature Data Retention (PCHTDR) are used to assess the electrical lifetime of the device's non-volatile memory array. NVCE performs program/erase cycles up to specification max cycles. PCHTDR checks the retention of cycled memory elements following temperature accelerated bakes to check for charge loss.

CrossLinkPlus NVCE+PCHTDR Conditions:

Program/Erase Cycle Count: 250

Program/Erase Temperature: $T_{Ambient}$ >= 85°C
Stress Duration: 100 hours
Stress Conditions: $T_{Ambient}$ >= 125°C
Method: JESD22-A117

Table 3.3.1 CrossLinkPlus PCHTDR Results

Product Name	Foundry	Lot #	Qty	NVCE Result	10 Hrs Result	100 Hrs Result	Cumulative Hours
LIF-MDF6000	USJC	1	38	0	0	0	3,800
		2	40	0	0	0	4,000
		3	40	0	0	0	4,000
		4	40	Q2, 2021			
		Total	118	0	0	0	11,800

3.5 Accelerated Soft Error Rate (ASER)

Soft Error Rate (SER) testing is conducted to characterize the sensitivity of SRAM memory elements to Atmospheric Neutron and Alpha Particle radiation. Charge induced by the impact of these particles can collect at sensitive nodes in the device and result in changes to the internal states of the device. While these changes do not cause physical damage to the device, they can cause errors in device operation.

Neutron SER – The normalized upset rate of Configuration RAM and Embedded Block RAM (EBR) memories due to neutron events. During testing, devices were configured with a memory pattern, exposed to an accelerated neutron environment, and the memory was read back from the device. Upset bits were identified through pattern comparison. Neutron testing results are normalized to the standard neutron flux for New York City at sea level: 14 n/cm^2/hr. The SER is represented in Failures in Time per million bits (FIT/Mb) to allow for translation across different device families and densities.

Alpha Particle SER – The normalized upset rate of Configuration RAM and Embedded Block RAM (EBR) memories due to alpha particle events. During testing, devices were configured with a memory pattern, exposed to a calibrated alpha source (Am-241), and the memory was read back from the device. Upset bits were identified through pattern comparison. Alpha particle testing results are normalized to a standard flux for Ultra Low Alpha (ULA) packaging materials: 0.001 alpha/cm^2/hr. The SER is represented in Failures in Time per million bits (FIT/Mb) to allow for translation across different device families and densities.

Table 3.3.1 40LP-SA (40nm) SER

Particle Type	Memory	SER (FIT/Mb)
Neutron	Configuration RAM	176.2
	EBR	262.9
Alpha Particle	Configuration RAM	152.8
	EBR	346.8

Note: Detailed SER reports are available upon request.

4.0 PACKAGE QUALIFICATION DATA FOR CROSSLINKPLUS PRODUCT FAMILY

The CrossLinkPlus devices are assembled and tested at Advanced Semiconductor Engineering, Kaohsiung Taiwan (ASEK). Package qualification tests include Surface Mount Pre-Conditioning (SMPC), Temperature Cycling (TC), Temperature-Humidity-Bias (THB), Unbiased Temperature-Humidity (TH), and High Temperature Storage Life (HTSL). Electrical test is performed pre- and post-stress. Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and Visual Package Inspection.

Table 4.0.1 Summary of Package Reliability Test Results

Assembly Site	Test	Test Vehicle	Package Type	Lot Quantity	Cumulative Units/Hours/Cycles	# of Fails
ASEK	SMPC	LIF-MDF6000	64ucfBGA	3	836 units	0
ASEK	TC	LIF-MDF6000	64ucfBGA	3	209,000 cycles	0
ASEK	THB	LIF-MDF6000	64ucfBGA	3	208,000 hours	0
ASEK	TH	LIF-MDF6000	64ucfBGA	3	209,000 hours	0
ASEK	HTSL	LIF-MDF6000	64ucfBGA	3	207,000 hours	0

4.1 Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through High Temperature Storage Life, Temperature Cycling, TH, and THB were preconditioned. This preconditioning is consistent with J-STD-020D and JEDEC JESD22-A113F “Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing”.

Surface Mount Preconditioning: 5cyc TC Condition B; 24 Hour Bake @ 125°C; 30°C/60% RH Soak for 192 hours (MSL3); 3X passes of reflow simulation performed before all package stresses.

MSL3 Packages: ucfBGA

Method: J-STD-020D and JESD22-A113F

Table 4.1.1 Surface Mount Precondition Data

PRODUCT NAME	FOUNDRY	PACKAGE	ASSY SITE	LOT	MOISTURE SOAK LEVEL	3x REFLOW TEMP	QTY	FAIL
LIF-MDF6000	USJC	64UCFBGA	ASEK	1	3	260°C	280	0
				2			276	0
				3			280	0

4.2 Temperature Cycling (TC)

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104D "Temperature Cycling", Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: ucfBGA

Stress Duration: 1000 cycles

Stress Conditions: Temperature cycling between -55°C to 125°C

Method: JESD22-A104D, Condition B

Table 4.2.1 Temperature Cycling Data

PRODUCT NAME	FOUNDRY	PACKAGE	ASSY SITE	LOT	STRESS DURATION (cycles)	QTY	FAIL
LIF-MDF6000	USJC	64UCFBGA	ASEK	1	1000	69	0
				2		70	0
				3		70	0

4.3 Steady-State Temperature Humidity Bias Life Test (THB)

Steady-State Temperature Humidity Bias Life Test (THB) uses temperature, humidity and bias to accelerate the penetration of moisture through the external protective material or along the interface between the external protective material and the metallic conductors that pass through.

Prior to THB, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: ucfBGA

Stress Conditions: Supplies = Max operating condition, Temperature = 85°C, Humidity = 85% RH

Stress Duration: 1000 Hours

Method: JESD22-A110E

Table 4.3.1 THB Data

PRODUCT NAME	FOUNDRY	PACKAGE	ASSY SITE	LOT	STRESS DURATION (hours)	QTY	FAIL
LIF-MDF6000	USJC	64UCFBGA	ASEK	1	1000	70	0
				2		68	0
				3		70	0

4.4 Steady-State Unbiased Temperature Humidity Life Test (TH)

Steady-State Unbiased Temperature Humidity Life Test (TH) uses temperature and humidity to accelerate the penetration of moisture through the external protective material or along the interface between the external protective material and the metallic conductors that pass through.

Prior to TH, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: ucfBGA

Stress Conditions: Temperature = 85°C, Humidity = 85% RH

Stress Duration: 1000 Hours

Method: JESD22-A110E , JESD22-A118B

Table 4.4.1 TH Data

PRODUCT NAME	FOUNDRY	PACKAGE	ASSY SITE	LOT	STRESS DURATION (hours)	QTY	FAIL
LIF-MDF6000	USJC	64UCFBGA	ASEK	1	1000	69	0
				2		70	0
				3		70	0

4.5 High Temperature Storage Life (HTSL)

The High Temperature Storage Life test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms. Consistent with JEDEC JESD22-A103D, the devices are subjected to high temperature storage Condition B: +150 (-0/+10) °C for 1000 hours. Prior to High Temperature Storage, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: ucfBGA

Stress Duration: 1000 hours

Temperature: 150°C (ambient)

Method: JESD22-A-103D

Table 4.5.1 High Temperature Storage Life Data

PRODUCT NAME	FOUNDRY	PACKAGE	ASSY SITE	LOT	STRESS DURATION (hours)	QTY	FAIL
LIF-MDF6000	USJC	64UCFBGA	ASEK	1	1000	69	0
				2		68	0
				3		70	0

5.0 REVISION HISTORY

Table 6.0.1 CrossLinkPlus Product Family Qualification Summary Revisions

Date	Revision	Change Summary
January 2021	A	Initial document release

Lattice Semiconductor Corporation
5555 NE Moore Court
Hillsboro, Oregon 97124 U.S.A.
Telephone: (503) 268-8000
www.latticesemi.com

© 2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.
www.latticesemi.com