Crosslink-NX Product Family Qualification Summary

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1.0 INTRODUCTION

CrossLink™-NX family of low-power FPGAs can be used in a wide range of applications, and are optimized for bridging and processing needs in Embedded Vision applications – supporting a variety of high bandwidth sensor and display interfaces, video processing and machine learning inferencing. It is built on Lattice Nexus FPGA platform, using low-power 28 nm FD-SOI technology. It combines the extreme flexibility of an FPGA with the low power and high reliability (due to extremely low SER) of FD-SOI technology, and offers small footprint package options.

In addition to the high reliability inherent to FD-SOI technology (due to its extremely low SER), active reliability features such as built-in frame-based SED/SEC (for SRAM-based logic fabric), and ECC (for EBR and LRAM) are also supported. Built-in ADC is available in each device for system monitoring functions.

2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Lattice Semiconductor's Reliability Monitor Program Procedure (Doc. #101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office.

Failure rates in this reliability report are expressed in FITs. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

The Crosslink-NX family is fabricated at Samsung using a 28nm FDSOI technology node - 28FDS.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at Product Reliability Monitor Report.

3.0 QUALIFICATION DATA FOR CROSSLINK-NX PRODUCT FAMILY

The Lattice Nexus FPGA platform combines Lattice's long-standing low power FPGA expertise with leading 28nm FD-SOI semiconductor manufacturing technology. With this platform Lattice is enabling the rapid development of multiple device families that deliver low power, high performance, high reliability and small form factor.

The CROSSLINK-NX product family is used as the primary technology qualification vehicle.

Product Family: CROSSLINK-NX
Packages offered: csfBGA caBGA csBGA QFN
Process Technology Node: 28nm FDSOI

3.1 Product Family Life Data

The High Temperature Operating Life (HTOL) test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JESD22-A108 "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.
The Early Life Failure Rate (ELFR) test uses large samples sizes for a short duration (48hrs ≤ t ≤ 168 hrs) HTOL stress to determine the infant mortality rate of a device family.

CROSSLINK-NX Life Test (HTOL & ELFR) Conditions:
Stress Duration: (HTOL - 168, 500, 1000 Hours) & (ELFR – 48Hours)
Stress Conditions: CROSSLINK-NX (LIFCL-40) max operating supplies, $T_{JUNCTION}$ = 125°C
Method: JESD22-A108

Table 3.1.1 Product Family Life Results

Product Name	Foundry	Package	Lot #	Qty	48 Hrs Result	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LIFCL-40	Samsung	400caBGA	Lot #1	77	N/A	0	0	0	77,000
LIFCL-40	Samsung	400caBGA	Lot #2	77	N/A	0	0	0	77,000
LIFCL-40	Samsung	400caBGA	Lot #3	77	N/A	0	0	0	77,000
LIFCL-40	Samsung	400caBGA	Lot #1	1000	0	N/A	N/A	N/A	48,000
LIFCL-40	Samsung	400caBGA	Lot #2	1000	0	N/A	N/A	N/A	48,000
LIFCL-40	Samsung	400caBGA	Lot #3	1000	0	N/A	N/A	N/A	48,000

LIFCL-40 Cumulative Life Testing Device Hours = 231,000
LIFCL-40Cumulative Result / Sample Size = 0 / 3231
LIFCL-40 FIT Rate = 51 FIT;
FIT Assumptions: CL=60%, AE=0.7eV, TjStress = 125C, TjUse=55C

3.2 ESD and Latch-Up Data

Electrostatic Discharge-Human Body Model

The CROSSLINK-NX product family was tested per JS-001 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.1 ESD-HBM Data

Product	Classification
LIFCL-40	Class 1C (1000 to < 2000V)

HBM Classification for Commercial/Industrial products, per JS-001-2017.
All HBM levels indicated are dual polarity.

Electrostatic Discharge-Charged Device Model

The CROSSLINK-NX product family was tested per the JS-002, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.2 ESD-CDM Data

Product	Classification
LIFCL-40	Class C0b (125 to 250V)

HBM Classification for Commercial/Industrial products, per JS-002-2018.
All HBM levels indicated are dual polarity.

Latch-Up

The CROSSLINK-NX product family was tested per the JESD78E IC Latch-up Test procedure.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.3 Latch-up I-Test Data

Product	Classification
LIFCL-40	Class II (> +/- 100mA)

I-Test LU classification for Commercial/Industrial products per JESD78E.
All IO-LU levels indicated are dual-polarity.

Table 3.2.4 Latch-up VSupply Overvoltage Data

Product	Classification
LIFCL-40	Class II (> 1.5x Vcc)

VSupply over-voltage test LU classification for Commercial/Industrial products, per JESD78E.

3.3 Soft Error Rate Data

Soft Error Rate (SER) testing is conducted to characterize the sensitivity of SRAM memory elements to Atmospheric Neutron and Alpha Particle radiation. Charge induced by the impact of these particles can collect at sensitive nodes in the device and result in changes to the internal states of the device. While these changes do not cause physical damage to the device, they can cause errors in device operation.

The Nexus product family on 28FDSOI features adjustable power modes: Low Power (LP) and High Performance (HP). During characterization, these power modes were found to have a notable impact on Configuration RAM SER, so results are reported accordingly. The Embedded Block RAM (EBR) elements are not affected by these power modes.

Neutron SER – The normalized upset rate of Configuration RAM and Embedded Block RAM (EBR) memories due to neutron events. During testing, devices were configured with a memory pattern, exposed to an accelerated neutron environment, and the memory was read back from the device. Upset bits were identified through pattern comparison. Neutron testing results are normalized to the standard neutron flux for New York City at sea level: 14 n/cm^2/hr. The SER is represented in Failures in Time per million bits (FIT/Mb) to allow for translation across different device families and densities.

Alpha Particle SER – The normalized upset rate of Configuration RAM and Embedded Block RAM (EBR) memories due to alpha particle events. During testing, devices were configured with a memory pattern, exposed to a calibrated alpha source (Am-241), and the memory was read back from the device. Upset bits were identified through pattern comparison. Alpha particle testing results are normalized to a standard flux for Ultra Low Alpha (ULA) packaging materials: 0.001 alpha/cm^2/hr. The SER is represented in Failures in Time per million bits (FIT/Mb) to allow for translation across different device families and densities.

Table 3.3.1 28FDSOI (28nm) SER

Particle Type	Memory	Power Mode	SER (FIT/Mb)
Neutron	Configuration RAM	LP	2.7
		HP	3.4
	EBR	N/A	6.9
Alpha Particle	Configuration RAM	LP	0.4
		HP	0.8
	EBR	N/A	3.4

Note: Detailed SER reports are available upon request.

4.0 PACKAGE QUALIFICATION DATA

The CROSSLINK-NX product family is offered in csfBGA, caBGA, QFN and WLCS packages. This report details the package qualification results of the initial CROSSLINK-NX product introductions. Package qualification tests include Temperature Cycling (TC), Temperature Humidity (TH), Temperature Humidity Bias (THB), and High Temperature Storage (HTSL). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and visual package inspection.

The generation and use of generic data is applied across a family of products or packages emanating from one base wafer foundry or assembly process is a Family Qualification, or Qualification-by-Similarity. For the package stresses THB, TH, and HTSL, these are considered generic for a given Package Technology. Surface Mount Pre-Conditioning (SMPC) is considered generic up to an evaluated Peak Reflow temperature, for a given Package Technology. The following table demonstrates the package qualification matrix.

Table 4.0.1 Product-Package Qualification-By-Similarity Matrix

<table>
<tr><th></th><th></th><th colspan="7">Advanced Semiconductor Engineering, Kaohsiung (ASEK)</th></tr>
<tr><th>The LIFCL product/package combinations are Qualified by Similarity (QBS) using the qualification vehicles below.</th><th>Stress Tests</th><th colspan="2">caBGA</th><th>csBGA</th><th colspan="2">csfBGA</th><th>QFN</th><th>WLCS</th></tr>
<tr><td></td><td></td><td>400caBGA</td><td>256caBGA</td><td>289csBGA</td><td>196csfBGA</td><td>121csfBGA</td><td>72QFN</td><td>72WLSC</td></tr>
<tr><td rowspan="5">LIFCL-40</td><td>SMPC</td><td>MSL3</td><td rowspan="5">QBS (1)</td><td>MSL3</td><td>MSL3</td><td rowspan="5">QBS (3)</td><td>MSL3</td><td rowspan="5">PACKAGE NOT OFFERED</td></tr>
<tr><td>TC</td><td>700 Cycles</td><td>700 Cycles</td><td>700 Cycles</td><td>700 Cycles</td></tr>
<tr><td>TH</td><td>1000Hours</td><td>1000Hours</td><td>1000Hours</td><td>1000Hours</td></tr>
<tr><td>THB</td><td>1000Hours</td><td>1000Hours</td><td>1000Hours</td><td>1000Hours</td></tr>
<tr><td>HTSL</td><td>1000Hours</td><td>1000Hours</td><td>1000Hours</td><td>1000Hours</td></tr>
<tr><td rowspan="5">LIFCL-17</td><td>SMPC</td><td rowspan="5">PACKAGE NOT OFFERED</td><td rowspan="5">QBS (1)</td><td rowspan="5">QBS (2)</td><td rowspan="5">QBS (3)</td><td rowspan="5">QBS (3)</td><td rowspan="5">QBS (4)</td><td>MSL3 TBD (5)</td></tr>
<tr><td>TC</td><td>700 Cycles TBD (5)</td></tr>
<tr><td>TH</td><td>1000Hours TBD (5)</td></tr>
<tr><td>THB</td><td>1000Hours TBD (5)</td></tr>
<tr><td>HTSL</td><td>1000Hours TBD (5)</td></tr>
</table>

(1) QBS to LIFCL-40 400caBGA

(2) QBS to LIFCL-40 289csBGA

(3) QBS to LIFCL-40 196csfBGA

(4) QBS to LIFCL-40 400caBGA

(5) TBD Estimating completion end of Q1 2021

4.1 Surface Mount Preconditioning (SMPC) Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, HTSL, TH, and THB were preconditioned. This preconditioning is consistent with IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices" and JESD22-A113 "Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing", Moisture Sensitivity Level 3 (MSL3) package moisture sensitivity and dry-pack storage requirements.

Surface Mount Preconditioning (MSL3 Condition B)

The following steps are performed before all package tests:

Step 1: 5 Temperature Cycles -55C/125C,

Step 2: 24 Hours bake @ 125°C,

Step 3: Soak 192 hours, temperature 30°C & relative humidity 60%

Step 4: 260 °C Reflow Simulation, 3 passes

MSL3 Packages: csfBGA caBGA csBGA QFN

Method: J-STD-020 and JESD22-A113

Table 4.1.1 SMPC Data

Product Name	Foundry	Package	Assembly Site	Lot Number	Moisture Soak Level	3X Reflow Temperature	Qty	# of Fails
LIFCL-40	SAMSUNG	400caBGA	ASEK	Lot1	MSL3	260°C	308	0
LIFCL-40	SAMSUNG	400caBGA	ASEK	Lot2	MSL3	260°C	308	0
LIFCL-40	SAMSUNG	400caBGA	ASEK	Lot3	MSL3	260°C	308	0
LIFCL-40	SAMSUNG	196csfBGA	ASEK	Lot1	MSL3	260°C	308	0
LIFCL-40	SAMSUNG	196csfBGA	ASEK	Lot2	MSL3	260°C	308	0
LIFCL-40	SAMSUNG	196csfBGA	ASEK	Lot3	MSL3	260°C	308	0
LIFCL-40	SAMSUNG	72QFN	ASEK	Lot1	MSL3	260°C	308	0
LIFCL-40	SAMSUNG	72QFN	ASEK	Lot2	MSL3	260°C	308	0
LIFCL-40	SAMSUNG	72QFN	ASEK	Lot3	MSL3	260°C	308	0
LIFCL-40	SAMSUNG	289csBGA	ASEK	Lot1	MSL3	260°C	308	0
LIFCL-40	SAMSUNG	289csBGA	ASEK	Lot2	MSL3	260°C	308	0
LIFCL-40	SAMSUNG	289csBGA	ASEK	Lot3	MSL3	260°C	308	0

Cumulative SMPC Failure Rate LIFCL-40 = 0 / 3,696

4.2 Temperature Cycling (TC) Testing

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JESD22-A104 "Temperature Cycling", Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csfBGA caBGA csBGA QFN

Stress Duration: 700 cycles

Stress Conditions: Temperature cycling between -55°C to 125°C

Method: JESD22-A104 Condition B

Table 4.2.1 TC Data

Product Name	Foundry	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Qty	# of Fails
LIFCL-40	SAMSUNG	400caBGA	ASEK	Lot1	-55°C to 125°C	700 cycles	77	0
LIFCL-40	SAMSUNG	400caBGA	ASEK	Lot2	-55°C to 125°C	700 cycles	77	0
LIFCL-40	SAMSUNG	400caBGA	ASEK	Lot3	-55°C to 125°C	700 cycles	77	0
LIFCL-40	SAMSUNG	196csfBGA	ASEK	Lot1	-55°C to 125°C	700 cycles	77	0
LIFCL-40	SAMSUNG	196csfBGA	ASEK	Lot2	-55°C to 125°C	700 cycles	77	0
LIFCL-40	SAMSUNG	196csfBGA	ASEK	Lot3	-55°C to 125°C	700 cycles	77	0
LIFCL-40	SAMSUNG	72QFN	ASEK	Lot1	-55°C to 125°C	700 cycles	77	0
LIFCL-40	SAMSUNG	72QFN	ASEK	Lot2	-55°C to 125°C	700 cycles	77	0
LIFCL-40	SAMSUNG	72QFN	ASEK	Lot3	-55°C to 125°C	700 cycles	77	0
LIFCL-40	SAMSUNG	289csBGA	ASEK	Lot1	-55°C to 125°C	700 cycles	77	0
LIFCL-40	SAMSUNG	289csBGA	ASEK	Lot2	-55°C to 125°C	700 cycles	77	0
LIFCL-40	SAMSUNG	289csBGA	ASEK	Lot3	-55°C to 125°C	700 cycles	77	0

Cumulative Temp Cycle Failure Rate LIFCL-40 = 0 / 924

4.3 Temperature Humidity (TH) Testing

Steady-State Temperature Humidity Life Test (TH) uses temperature, humidity, to accelerate the penetration of moisture through the external protective material or along the interface between the external protective material and the metallic conductors that pass through. The stress usually activates the same failure mechanism as UHAST but with a lower acceleration factor, hence, units are subjected to a longer stress time of 1000 hours at 85°C and 85% relative humidity, consistent with JEDEC JESD22-A101 “Steady-State Temperature Humidity Bias Life Test”.

MSL3 Packages: csfBGA caBGA csBGA QFN

Stress Duration: 1000 Hours

Stress Conditions: Temperature 85°C with Relative Humidity 85%

Method: JESD22-A101

Table 4.3.1 TH Data

Product Name	Foundry	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Qty	# of Fails
LIFCL-40	SAMSUNG	400caBGA	ASEK	Lot1	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	400caBGA	ASEK	Lot2	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	400caBGA	ASEK	Lot3	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	196csfBGA	ASEK	Lot1	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	196csfBGA	ASEK	Lot2	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	196csfBGA	ASEK	Lot3	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	72QFN	ASEK	Lot1	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	72QFN	ASEK	Lot2	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	72QFN	ASEK	Lot3	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	289csBGA	ASEK	Lot1	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	289csBGA	ASEK	Lot2	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	289csBGA	ASEK	Lot3	85°C	1000 hours	77	0

Cumulative Temp Humidity Failure Rate LIFCL-40 = 0 / 924

4.4 Temperature Humidity Bias (THB) Testing

Steady-State Temperature Humidity Bias Life Test (THB) uses temperature, humidity and bias, to accelerate the penetration of moisture through the external protective material or along the interface between the external protective material and the metallic conductors that pass through. The stress usually activates the same failure mechanism as BHAST but with a lower acceleration factor, hence, units are subjected to a longer stress time of 1000 hours at 85°C and 85% relative humidity, consistent with JEDEC JESD22-A101 "Steady-State Temperature Humidity Bias Life Test".

MSL3 Packages: csfBGA caBGA csBGA QFN

Stress Conditions: Max Operating Voltage on Supplies, Temperature 85°C with Relative Humidity 85%

Stress Duration: 1000 hours

Method: JESD22-A101

Table 4.4.1 THB Data

Product Name	Foundry	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Qty	# of Fails
LIFCL-40	SAMSUNG	400caBGA	ASEK	Lot1	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	400caBGA	ASEK	Lot2	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	400caBGA	ASEK	Lot3	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	196csfBGA	ASEK	Lot1	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	196csfBGA	ASEK	Lot2	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	196csfBGA	ASEK	Lot3	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	72QFN	ASEK	Lot1	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	72QFN	ASEK	Lot2	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	72QFN	ASEK	Lot3	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	289csBGA	ASEK	Lot1	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	289csBGA	ASEK	Lot2	85°C	1000 hours	77	0
LIFCL-40	SAMSUNG	289csBGA	ASEK	Lot3	85°C	1000 hours	77	0

Cumulative Temp Humidity Bias Failure Rate LIFCL-40 = 0 /

4.5 High Temperature Storage Life (HTSL) Testing

The High Temperature Storage Life test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms. Consistent with JESD22-A103, the devices are subjected to high temperature storage Condition B: +150 (-0/+10) °C for 1000 hours. Prior to High Temperature Storage, all CROSSLINK-NX devices are subjected to Surface Mount Preconditioning as mentioned in Table 4.1.1.

MSL3 Packages: csfBGA caBGA csBGA QFN

Stress Duration: 1000 hours

Temperature: 150°C (ambient)

Method: JESD22-A103

Table 4.5.1 HTSL Data

Product Name	Foundry	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Qty	# of Fails
LIFCL-40	SAMSUNG	400caBGA	ASEK	Lot1	150°C	1000 hours	77	0
LIFCL-40	SAMSUNG	400caBGA	ASEK	Lot2	150°C	1000 hours	77	0
LIFCL-40	SAMSUNG	400caBGA	ASEK	Lot3	150°C	1000 hours	77	0
LIFCL-40	SAMSUNG	196csfBGA	ASEK	Lot1	150°C	1000 hours	77	0
LIFCL-40	SAMSUNG	196csfBGA	ASEK	Lot2	150°C	1000 hours	77	0
LIFCL-40	SAMSUNG	196csfBGA	ASEK	Lot3	150°C	1000 hours	77	0
LIFCL-40	SAMSUNG	72QFN	ASEK	Lot1	150°C	1000 hours	77	0
LIFCL-40	SAMSUNG	72QFN	ASEK	Lot2	150°C	1000 hours	77	0
LIFCL-40	SAMSUNG	72QFN	ASEK	Lot3	150°C	1000 hours	77	0
LIFCL-40	SAMSUNG	289csBGA	ASEK	Lot1	150°C	1000 hours	77	0
LIFCL-40	SAMSUNG	289csBGA	ASEK	Lot2	150°C	1000 hours	77	0
LIFCL-40	SAMSUNG	289csBGA	ASEK	Lot3	150°C	1000 hours	77	0

Cumulative HTSL LIFCL-40 Failure Rate = 0 / 924

5.0 REVISION HISTORY

Table 5.0.1 CROSSLINK-NX Product Family Qualification Summary Revisions

Date	Revision	Change Summary
January 2021	A	New release using LIFCL-40 qualification data on 400caBGA 196csfBGA, 72QFN, 289csBGA.

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