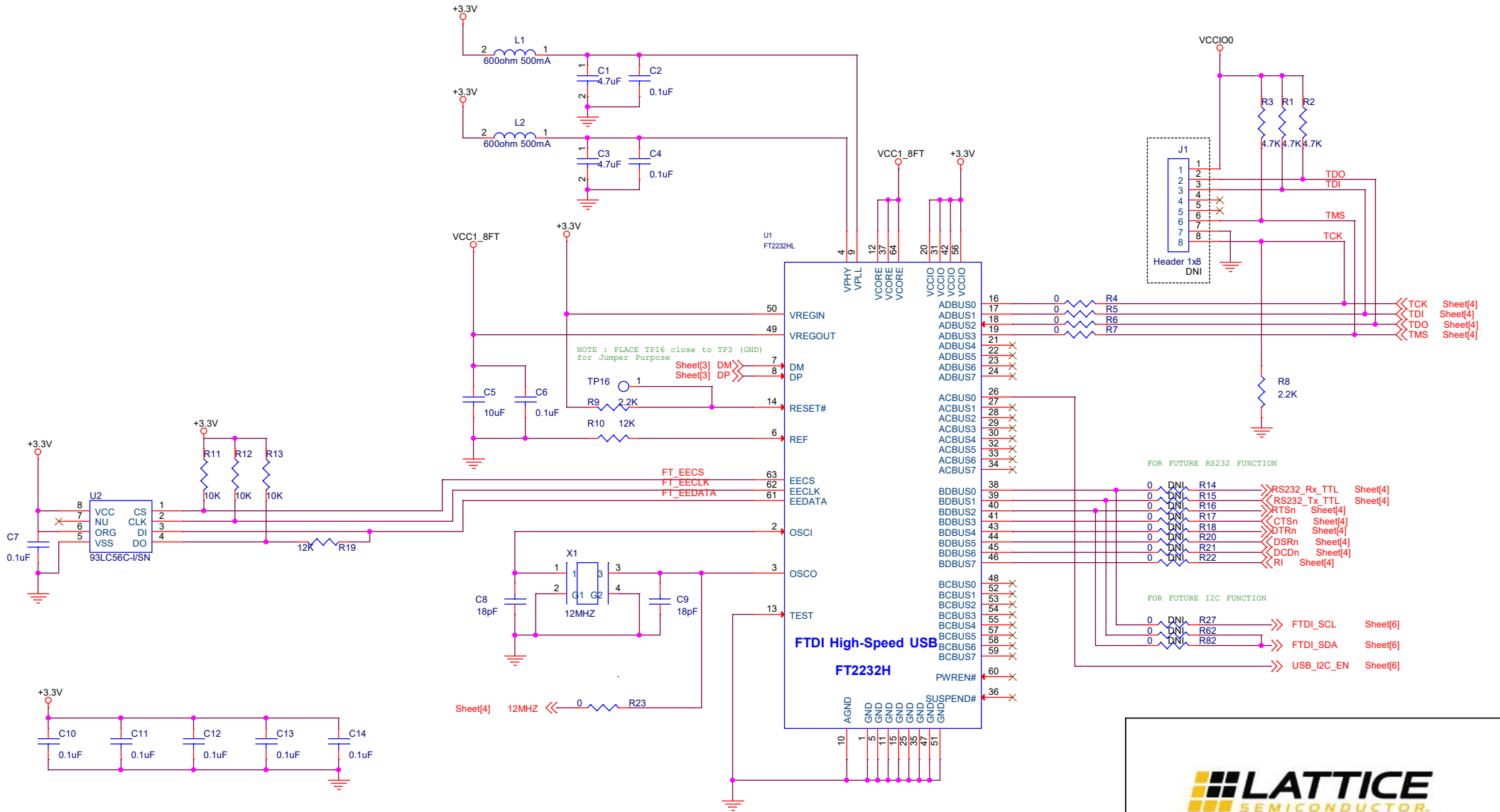



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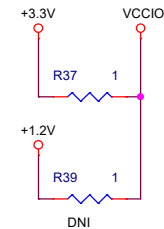
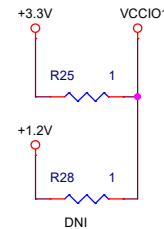
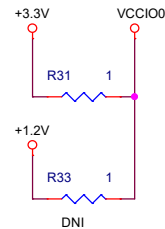
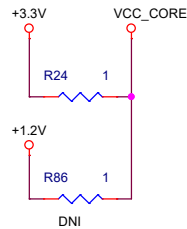
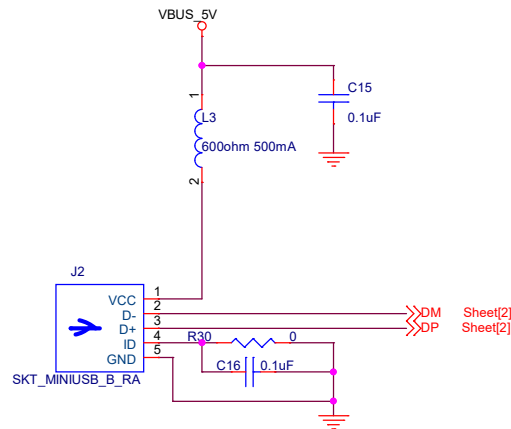
Title MachXO3D Breakout Board- BLOCK DIAGRAM		
Size B	Project MachXO3D Breakout Board	Schematic Rev 1.0 Board Rev A
Date: 15-APR-19	Sheet	1 of 8



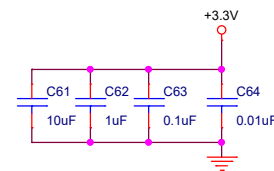
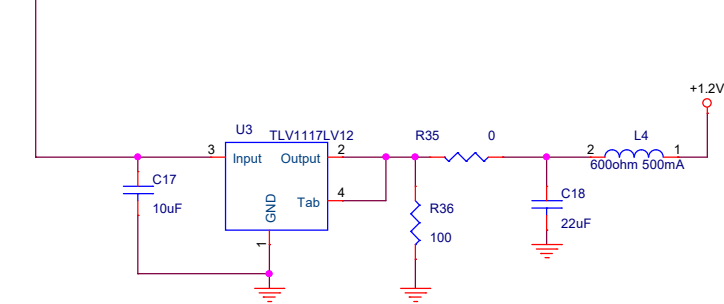
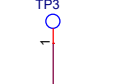
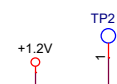
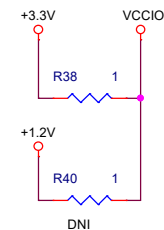
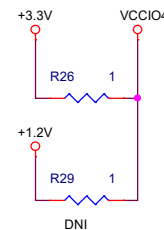
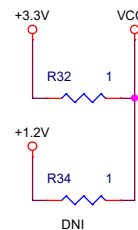
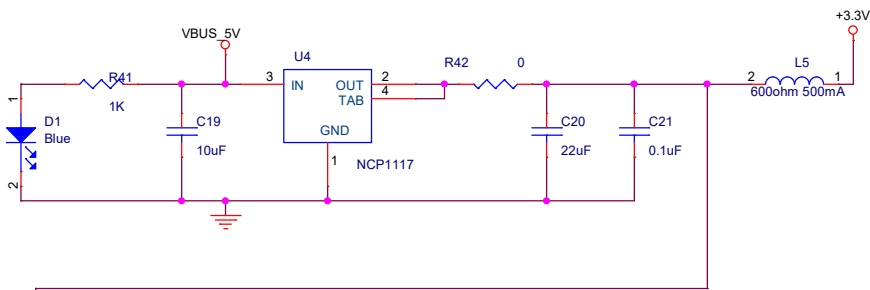


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Title		USB to JTAG I/F
Size B	Project	Schematic Rev 1.0
	MachXO3D Breakout Board	
Date:	15-APR-19	Sheet 2 of 8

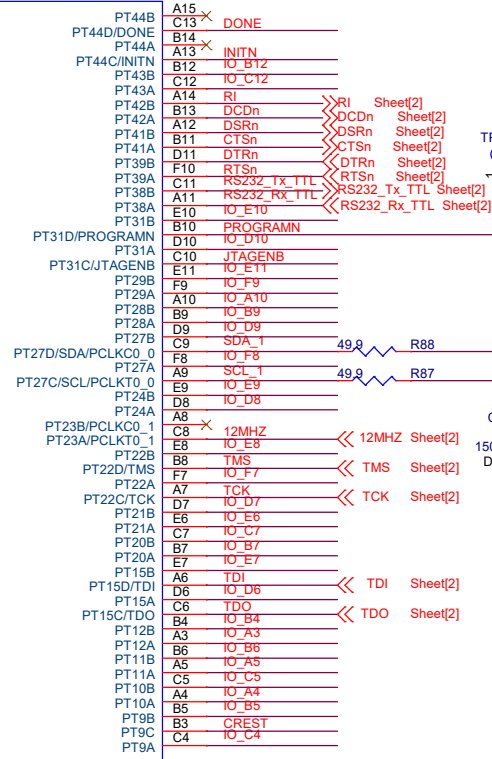
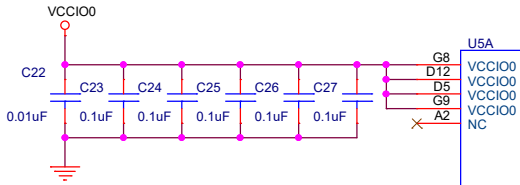


NOTE : Boot from external SPI Flash (U6) requires VCCIO2 set to 3.3V. Use caution when setting VCCIO2 to any other voltage.



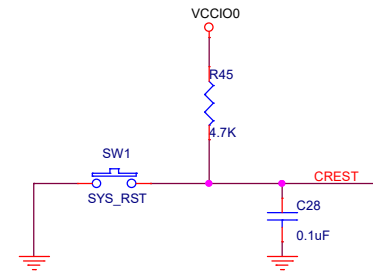
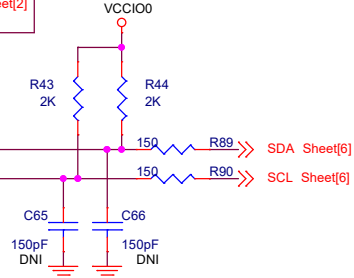
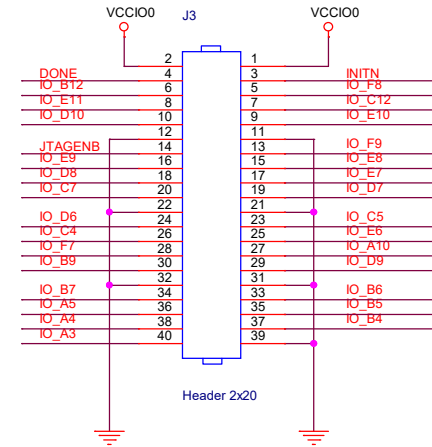
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Title		
POWER REGULATORS		
Size	Project	Schematic Rev 1.0
B	MachXO3D Breakout Board	Board Rev A
Date:	15-APR-19	Sheet 3 of 8



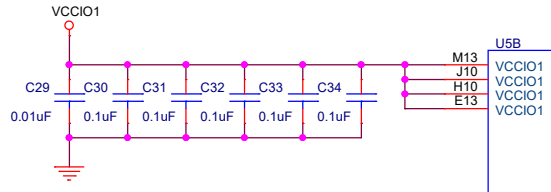
LCMXO3D-9400HC-5BG256C

NOTE : MAKE PWR TRACES
CAPABLE OF 1A



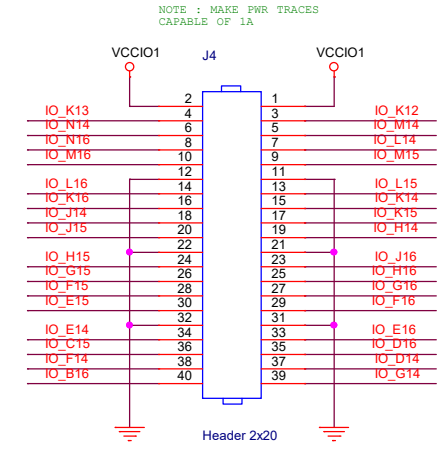
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Title BANK0 I/O		
Size B	Project MachXO3D Breakout Board	Schematic Rev 1.0 Board Rev A
Date: 15-APR-19	Sheet 4 of 8	



Component	Pin	Signal	Notes
PR30D	P15	X	
PR30C	N14	X	IO_N14
PR29B	N16	X	IO_N16
PR29A	P16	X	LED7 Sheet[8]
PR28D	M15	X	IO_M15
PR28B	N15	X	LED6 Sheet[8]
PR28C	M14	X	IO_M14
PR28A	L13	X	LED5 Sheet[8]
PR25D	M16	X	IO_M16
PR25B	K11	X	LED4 Sheet[8]
PR25C	L15	X	IO_L15
PR25A	K12	X	IO_K12
PR24D	K13	X	IO_K13
PR24C	L14	X	IO_L14
PR21B	L16	X	IO_L16
PR21A	L12	X	LED3 Sheet[8]
PR20D	K15	X	IO_K15
PR20B	J11	X	LED2 Sheet[8]
PR20C	K14	X	IO_K14
PR20A	J13	X	LED1 Sheet[8]
PR19D	K16	X	IO_K16
PR19B	H11	X	LED0 Sheet[8]
PR19C	J15	X	IO_J15
PR19A	J14	X	IO_J14
PR18B	J16	X	IO_J16
PR18A	H16	X	IO_H16
PR17B/PCLKC1_0	H14	X	IO_H14
PR17A/PCLKT1_0	J12	X	
PR16D	H15	X	IO_H15
PR16B	H13	X	
PR16C	G16	X	IO_G16
PR16A	H12	X	
PR14D	G11	X	
PR14C	K13	X	IO_K13
PR12B	G14	X	IO_G14
PR12A	G15	X	IO_G15
PR12A	G13	X	
PR10D	F12	X	
PR10C	F16	X	IO_F16
PR7B	F14	X	IO_F14
PR7A	G12	X	
PR6D	F13	X	
PR6C	F15	X	IO_F15
PR5B	E16	X	IO_E16
PR5A	D15	X	
PR4D	C16	X	
PR4C	E14	X	IO_E14
PR3B/R_GPLL_C_IN	D16	X	IO_D16
PR3A/R_GPLL_T_IN	B16	X	IO_B16
PR2D	E15	X	IO_E15
PR2B/R_GPLL_C_FB	C15	X	IO_C15
PR2C	D14	X	IO_D14
PR2A/R_GPLL_T_FB			

LCMXO3D-9400HC-5BG256C



Proto Type Area, Holes on 0.1 inch Centers
DNI

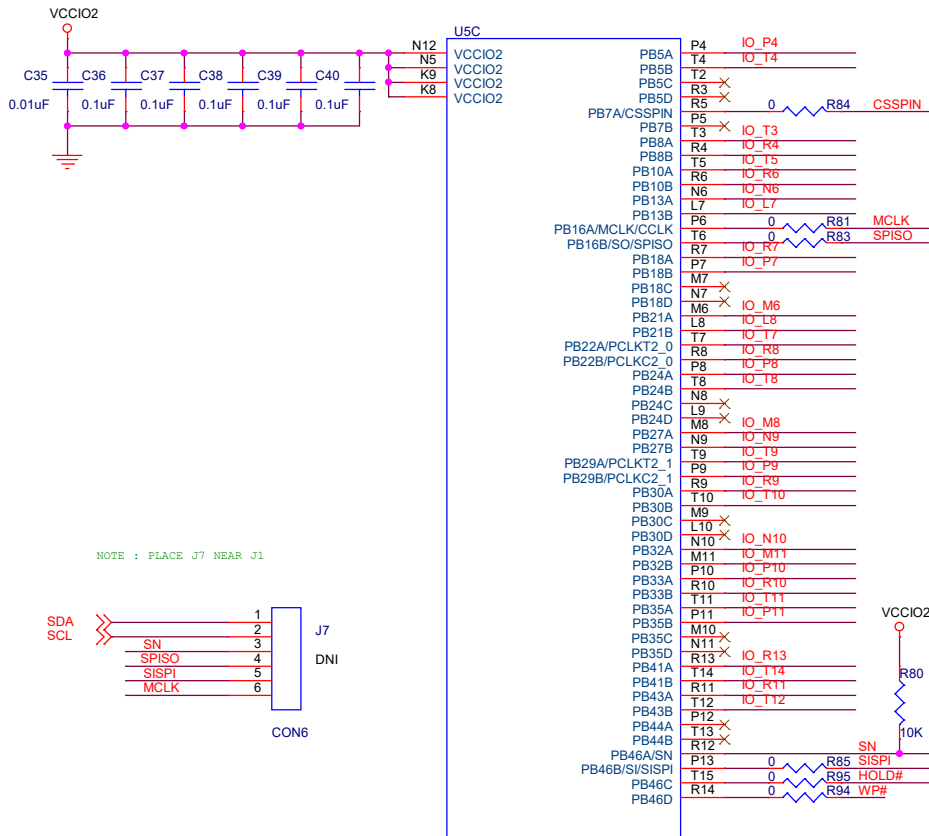
PROTOTYPE AREA
FILL AVAILABLE AREA



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Title		
BANK1 I/O		
Size	Project	Schematic Rev
B	MachXO3D Breakout Board	1.0
Date:	15-APR-19	Sheet 5 of 8

NOTE : PLACE R84,R81,R83,R85 CLOSE TO U5



NOTE : MAKE PWR TRACES CAPABLE OF 1A

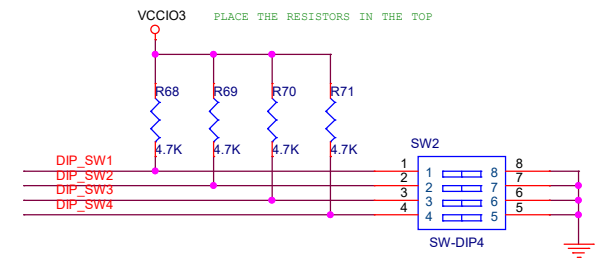
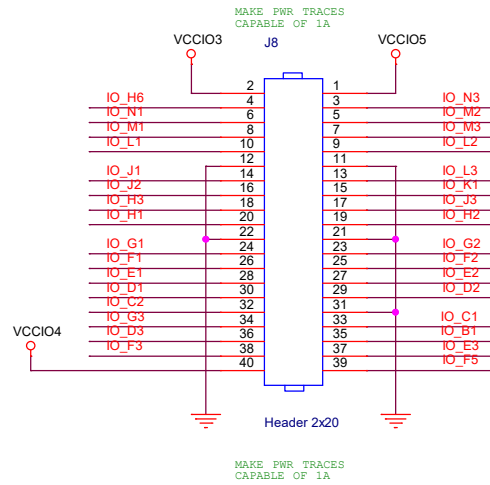
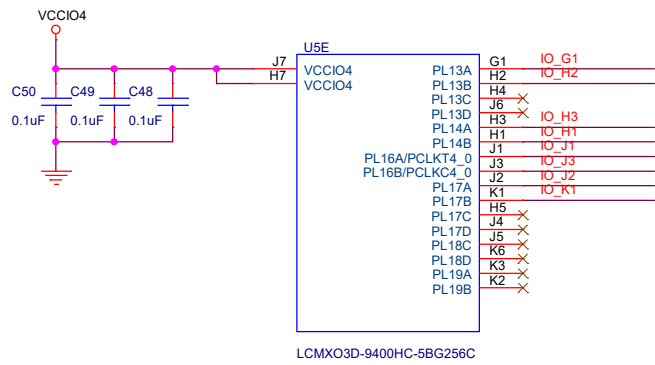
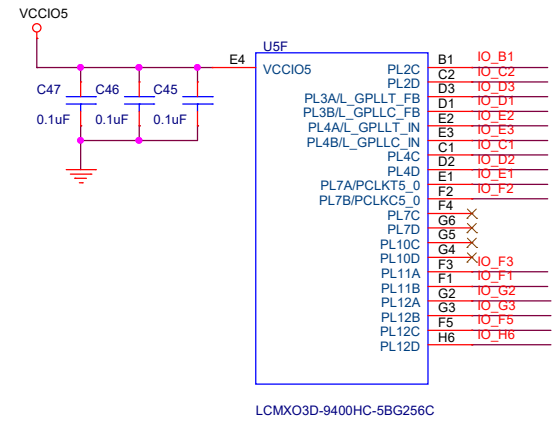
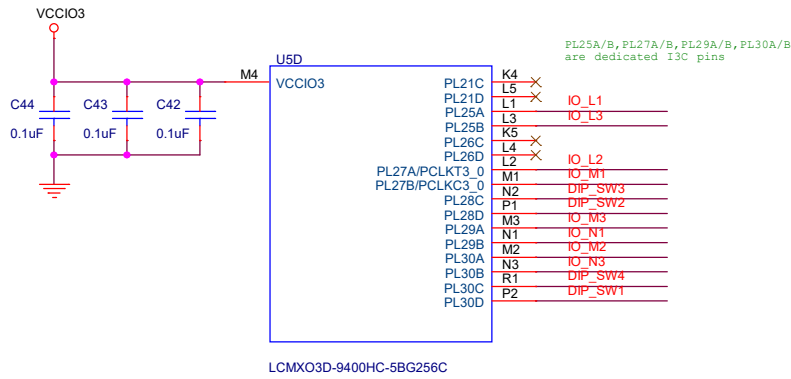
NOTE : ROUTE J6 TRACES AS 100OHMS, LENGTH MATCHED DIFFERENTIAL PAIRS

NOTE : PLACE ALL THE LVDS DIFF TERMINATION RESISTORS IN TOP AND CLOSE TO U5



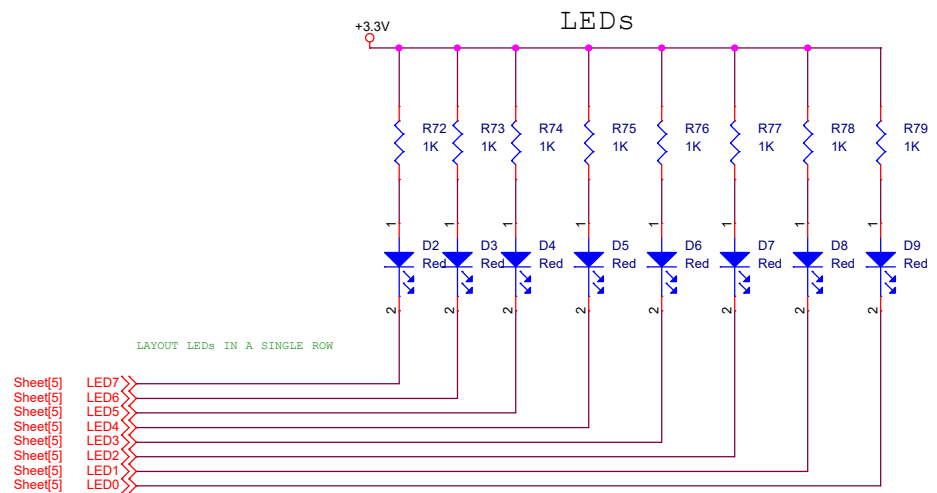
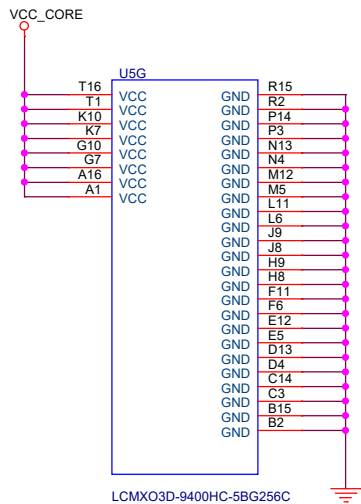
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Title		BANK2 I/O
Size	Project	Schematic Rev 1.0
B	MachXO3D Breakout Board	Board Rev A
Date:	15-APR-19	Sheet 6 of 8

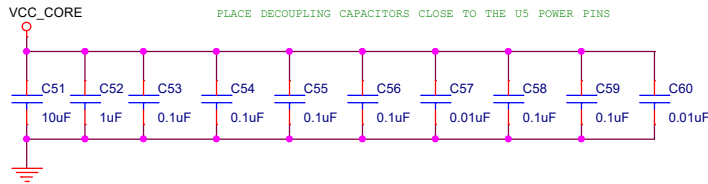


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Title			BANK3,4,5 I/O
Size	Project	Schematic Rev 1.0	
B	MachXO3D Breakout Board	Board Rev A	
Date:	15-APR-19	Sheet	7 of 8



Note : LEDs are controlled by XO3D I/O Bank 1. When VCCIO1 is set to a voltage less than 3.3V, observe all I/O overdrive requirements. Refer to Lattice Technical Note "MachXO3D sysIO Usage Guide" for more information.



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Title			POWER DECOUPLING AND LED'S
Size B	Project	MachXO3D Breakout Board	
	Schematic	Rev	1.0
Date:	15-APR-19	Sheet	8 of 8