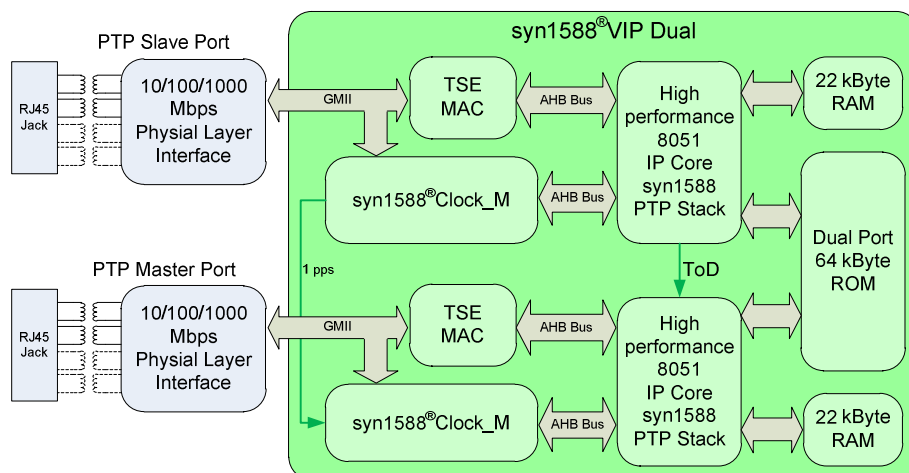


## Features

- 2 independent PTP ports with shared local oscillator
- Configurable role per port
- Configurable profile per port
- 10/100/1000 Mbps Ethernet MAC, (IEEE802.3-2000)
- IEEE1588-2008 hardware timestamping
- 2 IEEE1588 hardware clocks
- IEEE1588-2008 Layer 2 compliant
- IEEE1588-2008 Layer 3 compliant (UDP, ARP, DHCP)
- Clocks accuracy better than 50 ns
- syn1588<sup>®</sup> PTP stack binary included (running on integrated 8-bit CPU core)
- Shared program ROM
- 2x 1pps outputs
- 2x Frequency outputs
- 2x Event input
- In layer-3 mode each node may be controlled remotely via IEEE1588 management messages
- Optional analog PLL using VXCOs

## Options

- Serial interface to external CPU upon request



### syn1588<sup>®</sup> Versatile IP Dual - Fully integrated 2-port clock synchronization solution

The syn1588<sup>®</sup> VIP Dual SoC IP core offers unparalleled integration density, providing the end user with a versatile 2-port PTP node. Each port may operate in any PTP role using either the default, the power, or the telecom profile. The combination of all necessary hard- and software module into one single chip enables a cost effective and highly integrated single chip dual port PTP solution. Only a single external Ethernet PHY for every port is required to create an IEEE1588 node.

Every port will generate an accurate high precision 1-pps signal together with a user programmable frequency output phase locked to the synchronized local clock of the respective port. Additionally, time stamps are generated in case an external event occurs on a dedicated pin.

Every port may be configured separately according to IEEE1588. The syn1588<sup>®</sup> VIP Dual supports a variety of possible implementation scenarios

- **Slave-Master:** One port is configured as a slave-only node attached to an external grand master thus maintaining the connection to an external network. While the other port will run in master mode supplying the local network with accurate time information. The time information will be transferred internally between the two ports.
- **Hot-Stand-by:** Both ports, if configured as slaves, may be connected to different external masters and will be generating 1-pps signals together with phased locked output frequencies

to be fed to their host system. In case one master fails, the 1 pps feed can be switched over.

- **Different-Profiles:** One port may be run in slave mode being connected to an external multicast master, while the other port will run in unicast master mode supporting the telecom profile. Alternatively the second port may be operated in power profile using the peer-delay mechanism, transmitting messages at a pre-defined rate.
- **Redundant-Master:** Both ports may be connected to an external GPS timing receiver via their respective 1 pps input pins and a common shared serial input stream. Such a configuration allows building redundant masters structures. Thus it is possible to build a split network topology, if the ports are connected to distinct LANs.
- **GPS-Connectivity:** Each port may be configured to either accept NMEA formatted Time-of-Day data from a standard GPS timing receiver. In combination with a 1 pps input signal it will synchronize to this time reference subsequently acting as a PTP master on the respective port. Using two GPS time sources a highly redundant grand master can be built.

The syn1588<sup>®</sup> VIP is initially available on LatticeECP3 and LatticeECP2M FPGAs. As the IP is designed to be completely technology independent, it can be easily retargeted to other FPGAs or any ASIC technology.

Version 1.1 – April 2011

Technical Specifications	
Standards	IEEE802.3-2000 IEEE1588-2008
Supported functions	IEEE1588 hardware timestamping IEEE1588 hardware clock 1 one pulse per second output per port 1 synchronous frequency output per port 1 event timestamp input per port NMEA compatible data stream on serial interface Boundary Clock with fixed port assignment Profile selectable per port Serial Control interface
Operating temperature	N/A (depending on target technology)
Humidity	N/A
Driver support	N/A



Mohsgasse 1  
A-1030 Vienna  
Austria  
<http://oregano.at>  
[contact@oregano.at](mailto:contact@oregano.at)

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