Description

The GAL20XV10 combines a high performance CMOS process with electrically erasable (E²) floating gate technology to provide the highest speed Exclusive-OR PLD available in the market. At 90mA maximum Icc (75mA typical Icc), the GAL20XV10 provides a substantial savings in power when compared to bipolar counterparts. E²CMOS technology offers high speed (<100ms) erase times providing the ability to reprogram, reconfigure or test the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL20XV10 are the PAL® architectures listed in the macrocell description section of this document. The GAL20XV10 is capable of emulating these PAL architectures with full function and parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacturing. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

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July 1997
GAL20XV10 Ordering Information

Commercial Grade Specifications

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<th>Tsu (ns)</th>
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<th>Icc (mA)</th>
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<th>Package</th>
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<td>6</td>
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<td>90</td>
<td>GAL20XV10B-10LP</td>
<td>24-Pin Plastic DIP</td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td>GAL20XV10B-10LJ</td>
<td>28-Lead PLCC</td>
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<td>8</td>
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<td>GAL20XV10B-20LP</td>
<td>24-Pin Plastic DIP</td>
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<td></td>
<td>GAL20XV10B-20LJ</td>
<td>28-Lead PLCC</td>
</tr>
</tbody>
</table>

Part Number Description

GAL20XV10B  Device Name

Speed (ns)

L = Low Power  Power

Grade  Blank = Commercial

Package

P = Plastic DIP

J = PLCC

Discontinued Product (PCN #02-06). Contact Rochester Electronics for Availability.

www.latticesemi.com/sales/discontinueddevicessales.cfm
Output Logic Macrocell (OLMC)

The following discussion pertains to configuring the Output Logic Macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

The GAL20XV10 has two global architecture configurations that allow it to emulate PAL architectures. The input mode emulates combinational PAL devices, with the I/CLK and I/OE pins used as inputs. The Feedback mode emulates registered PAL devices with the I/CLK pin used as the register clock and the I/OE pin as an output enable for all registers. The following is a list of PAL architectures that the GAL20XV10 can emulate. It also shows the global architecture mode used to emulate the PAL architecture.

<table>
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<th>PAL Architectures Emulated by GAL20XV10</th>
<th>GAL20XV10 Global OLMC Mode</th>
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<tr>
<td>PAL12L10</td>
<td>input mode</td>
</tr>
<tr>
<td>PAL20L10</td>
<td>input mode</td>
</tr>
<tr>
<td>PAL20X10</td>
<td>feedback mode</td>
</tr>
<tr>
<td>PAL20X8</td>
<td>feedback mode</td>
</tr>
<tr>
<td>PAL20X4</td>
<td>feedback mode</td>
</tr>
</tbody>
</table>

**INPUT MODE**
The Input mode architecture is defined when the global architecture bit SYN = 1. In this mode, the I/CLK pin becomes an input to the AND array and also provides the clock source for all registers. The I/OE pin becomes an input into the AND array and provides the output enable control for any macrocell configured as an Exclusive-OR function. Feedback into the AND array is provided from macrocells 2 through 9 only. In this mode, macrocells 1 and 10 have no feedback into the AND array.

**FEEDBACK MODE**
The Feedback mode architecture is defined when the global architecture bit SYN = 0. In this mode the I/CLK pin becomes a dedicated clock source for all registers. The I/OE pin is a dedicated output enable control for any macrocell configured as an Exclusive-OR function. The I/CLK and I/OE pins are not available to the AND array in this mode. Feedback into the AND array is provided on all macrocells 1 through 10.

**FEATURES**
Each Output Logic Macrocell has four possible logic function configurations controlled by architecture control bits AC0 and AC1. Four product terms are fed into each macrocell.

**XOR REGISTERED CONFIGURATION**
The Macrocell is set to the Exclusive-OR Registered configuration when AC0 = 0 and AC1 = 1. The four product terms are segmented into two OR-sums of two product terms each, which are then combined by an Exclusive-OR gate and fed into a D-type register. The register is clocked by the low-to-high transition of the I/CLK pin. The inverting output buffer is enabled by the I/OE pin, which is an active low output enable common to all Exclusive-OR macrocells. In Feedback mode, the state of the register is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the register is available to the AND array via an internal feedback path on macrocells 2 through 9 only, macrocells 1 and 10 have no feedback into the AND array.

**REGISTERED CONFIGURATION**
The Macrocell is set to Registered configuration when AC0 = 1 and AC1 = 0. Three of the four product terms are used as sum-of-product terms for the D input of the register. The inverting output buffer is enabled by the fourth product term. The output is enabled while this product term is true. The XOR bit controls the polarity of the output. The register is clocked by the low-to-high transition of the I/CLK. In Feedback mode, the state of the register is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the register is available to the AND array via an internal feedback path on macrocells 2 through 9 only, macrocells 1 and 10 have no feedback into the AND array.

**XOR COMBINATORIAL CONFIGURATION**
The Macrocell is set to the Exclusive-OR Combinatorial configuration when AC0 = 1 and AC1 = 1. The four product terms are segmented into two OR-sums of two product terms each, which are then combined by an Exclusive-OR gate and fed to an output buffer. The inverting output buffer is enabled by the I/OE pin, which is an active low output enable that is common to all XOR macrocells. In Feedback mode, the state of the I/O pin is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the I/O pin is available to the AND array via an input buffer path on macrocells 2 through 9 only, macrocells 1 and 10 have no input into the AND array.

**COMBINATORIAL CONFIGURATION**
The Macrocell is set to Combinatorial mode when AC0 = 0 and AC1 = 1. The four product terms are used as sum-of-product terms for the combinatorial output. The XOR bit controls the polarity of the output. The inverting output buffer is enabled by the fourth product term. The output is enabled while this product term is true. In Feedback mode, the state of the I/O pin is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the I/O pin is available to the AND array via an input buffer path on macrocells 2 through 9 only, macrocells 1 and 10 have no input into the AND array.
Specifications **GAL20XV10**

**Input Mode**

### XOR Registered Configuration
- SYN = 1.
- AC0 = 0.
- AC1 = 0.
- OLMC 1 and OLMC10 do not have the feedback path.
- Pin 1(2) can be CLK and/or Input.
- Pin 13(16) can be OE and/or Input.

### Registered Configuration
- SYN = 1.
- AC0 = 1.
- AC1 = 0.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- OLMC 1 and OLMC10 do not have the feedback path.
- Pin 1(2) can be CLK and/or Input.
- OE controlled by product term.

### XOR Combinatorial Configuration
- SYN = 1.
- AC0 = 0.
- AC1 = 1.
- OLMC 1 and OLMC10 do not have the feedback path.
- Pin 13(16) can be OE and/or Input.

### Combinatorial Configuration
- SYN = 1.
- AC0 = 1.
- AC1 = 1.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- OLMC 1 and OLMC10 do not have the feedback path.
- OE controlled by product term.

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Specifications GAL20XV10

DIP (PLCC) Package Pinouts

**OLMC**
- XOR - 1600
- AC0 - 1610
- AC1 - 1620

**OLMC**
- XOR - 1601
- AC0 - 1611
- AC1 - 1621

**OLMC**
- XOR - 1602
- AC0 - 1612
- AC1 - 1622

**OLMC**
- XOR - 1603
- AC0 - 1613
- AC1 - 1623

**OLMC**
- XOR - 1604
- AC0 - 1614
- AC1 - 1624

**OLMC**
- XOR - 1605
- AC0 - 1615
- AC1 - 1625

**OLMC**
- XOR - 1606
- AC0 - 1616
- AC1 - 1626

**OLMC**
- XOR - 1607
- AC0 - 1617
- AC1 - 1627

**OLMC**
- XOR - 1608
- AC0 - 1618
- AC1 - 1628

**OLMC**
- XOR - 1609
- AC0 - 1619
- AC1 - 1629

**OLMC**
- XOR - 1610
- AC0 - 1620
- AC1 - 1630

**OLMC**
- XOR - 1611
- AC0 - 1621
- AC1 - 1631

**OLMC**
- XOR - 1612
- AC0 - 1622
- AC1 - 1632

**OLMC**
- XOR - 1613
- AC0 - 1623
- AC1 - 1633

**OLMC**
- XOR - 1614
- AC0 - 1624
- AC1 - 1634

**OLMC**
- XOR - 1615
- AC0 - 1625
- AC1 - 1635

**OLMC**
- XOR - 1616
- AC0 - 1626
- AC1 - 1636

**OLMC**
- XOR - 1617
- AC0 - 1627
- AC1 - 1637

**OLMC**
- XOR - 1618
- AC0 - 1628
- AC1 - 1638

**OLMC**
- XOR - 1619
- AC0 - 1629
- AC1 - 1639

**OLMC**
- XOR - 1620
- AC0 - 1630
- AC1 - 1640

**OLMC**
- XOR - 1621
- AC0 - 1631
- AC1 - 1641

**OLMC**
- XOR - 1622
- AC0 - 1632
- AC1 - 1642

**OLMC**
- XOR - 1623
- AC0 - 1633
- AC1 - 1643

**OLMC**
- XOR - 1624
- AC0 - 1634
- AC1 - 1644

**OLMC**
- XOR - 1625
- AC0 - 1635
- AC1 - 1645

**OLMC**
- XOR - 1626
- AC0 - 1636
- AC1 - 1646

**OLMC**
- XOR - 1627
- AC0 - 1637
- AC1 - 1647

**OLMC**
- XOR - 1628
- AC0 - 1638
- AC1 - 1648

**OLMC**
- XOR - 1629
- AC0 - 1639
- AC1 - 1649

**OLMC**
- XOR - 1630
- AC0 - 1640
- AC1 - 1650

40-USER ELECTRONIC SIGNATURE FUSES

<table>
<thead>
<tr>
<th>Byte4</th>
<th>Byte3</th>
<th>...</th>
<th>Byte1</th>
<th>Byte0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1631, 1632, ...</td>
<td>....</td>
<td>1669, 1670</td>
<td>SYN - 1630</td>
<td></td>
</tr>
</tbody>
</table>
Specifications **GAL20XV10**

**Feedback Mode**

### XOR Registered Configuration
- SYN = 0.
- AC0 = 0.
- AC1 = 0.
- Dedicated CLK input on Pin 1(2).
- Dedicated OE input on Pin 13(16).

### Registered Configuration
- SYN = 0.
- AC0 = 1.
- AC1 = 0.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- Dedicated CLK input on Pin 1(2).
- OE controlled by product term.
- Pin 13(16) is not connected to this configuration.

### XOR Combinatorial Configuration
- SYN = 0.
- AC0 = 0.
- AC1 = 1.
- Dedicated OE input on Pin 13(16).
- Pin 1(2) is not connected to this configuration.

### Combinatorial Configuration
- SYN = 0.
- AC0 = 1.
- AC1 = 1.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- OE controlled by product term.
- Both pin 1(2) and pin 13(16) are not connected to this configuration.

Discontinued Product (PCN #02-06). Contact Rochester Electronics for Availability. [www.latticesemi.com/sales/discontinueddevicessales.cfm](http://www.latticesemi.com/sales/discontinueddevicessales.cfm)
Feedback Mode Logic Diagram

DIP (PLCC) Package Pinouts

- OLMC
- XOR - 1600
- AC0 - 1610
- AC1 - 1620
- 23(27)

- OLMC
- XOR - 1601
- AC0 - 1611
- AC1 - 1621
- 22(26)

- OLMC
- XOR - 1602
- AC0 - 1612
- AC1 - 1622
- 21(25)

- OLMC
- XOR - 1603
- AC0 - 1613
- AC1 - 1623
- 20(24)

- OLMC
- XOR - 1604
- AC0 - 1614
- AC1 - 1624
- 19(23)

- OLMC
- XOR - 1605
- AC0 - 1615
- AC1 - 1625
- 18(21)

- OLMC
- XOR - 1606
- AC0 - 1616
- AC1 - 1626
- 17(20)

- OLMC
- XOR - 1607
- AC0 - 1617
- AC1 - 1627
- 16(19)

- OLMC
- XOR - 1608
- AC0 - 1618
- AC1 - 1628
- 15(18)

- OLMC
- XOR - 1609
- AC0 - 1619
- AC1 - 1629
- 14(17)

- OLMC
- XOR - 1610
- AC0 - 1611
- AC1 - 1621
- 13(16)

40-USER ELECTRONIC SIGNATURE FUSES

1631, 1632, .... 1669, 1670

Byte4 Byte3 .... Byte1 Byte0

SYN - 1630

Discontinued Product (PCN #02-06). Contact Rochester Electronics for Availability.

www.latticesemi.com/sales/discontinueddevicessales.cfm
## Specifications GAL20XV10

### Absolute Maximum Ratings

- Supply voltage $V_{cc}$: $-0.5$ to $+7$ V
- Input voltage applied: $-2.5$ to $V_{cc} + 1.0$ V
- Off-state output voltage applied: $-2.5$ to $V_{cc} + 1.0$ V
- Storage Temperature: $-65$ to $150$°C

### Recommended Operating Conditions

#### Commercial Devices:
- Ambient Temperature ($T_A$): $0$ to $+75$°C
- Supply voltage ($V_{cc}$) with respect to ground: $+4.75$ to $+5.25$ V

### DC Electrical Characteristics

#### Over Recommended Operating Conditions (Unless Otherwise Specified)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>$V_{SS} - 0.5$</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>$V_{CC} + 1$</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input or I/O Low Leakage Current</td>
<td>$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$</td>
<td>—</td>
<td>—</td>
<td>$-100$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input or I/O High Leakage Current</td>
<td>$3.5V \leq V_{IN} \leq V_{CC}$</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>$I_{OL} = \text{MAX.}$, $V_{IN} = V_{IL}$ or $V_{IH}$</td>
<td>—</td>
<td>—</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td>$I_{OH} = \text{MAX.}$, $V_{IN} = V_{IL}$ or $V_{IH}$</td>
<td>2.4</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td>Low Level Output Current</td>
<td></td>
<td>—</td>
<td>—</td>
<td>16</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OH}$</td>
<td>High Level Output Current</td>
<td></td>
<td>—</td>
<td>—</td>
<td>$-3.2$</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Output Short Circuit Current</td>
<td>$V_{CC} = 5$V, $V_{OUT} = 0.5$ V, $T_A = 25$°C</td>
<td>$-50$</td>
<td>—</td>
<td>$-150$</td>
<td>mA</td>
</tr>
</tbody>
</table>

#### Commercial

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>$V_{IL} = 0.5$ V, $V_{IH} = 3.0$ V, $f_{	ext{ripple}} = 15$ MHz Outputs Open</th>
<th>$L = -10$%/$-15$%/$-20$%</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>$I_{CC}$</td>
<td>Operating Power Supply Current</td>
<td></td>
<td></td>
<td>75</td>
<td>90</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

1) The leakage current is due to the internal pull-up on all input and I/O pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. $V_{out} = 0.5$ V was selected to avoid test problems by tester ground degradation. Characterized but not $100\%$ tested.
3) Typical values are at $V_{cc} = 5$ V and $T_A = 25$ °C
## AC Switching Characteristics

**Over Recommended Operating Conditions**

<table>
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<tr>
<th>PARAMETER</th>
<th>TEST COND.</th>
<th>DESCRIPTION</th>
<th>COM</th>
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<th>COM</th>
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<td></td>
<td></td>
<td></td>
<td>MIN.</td>
<td>MAX.</td>
<td>MIN.</td>
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<tr>
<td>tpd</td>
<td>A</td>
<td>Input or I/O to Combinatorial Output</td>
<td>3</td>
<td>10</td>
<td>3</td>
</tr>
<tr>
<td>tco</td>
<td>A</td>
<td>Clock to Output Delay</td>
<td>2</td>
<td>7</td>
<td>2</td>
</tr>
<tr>
<td>tfcf</td>
<td>—</td>
<td>Clock to Feedback Delay</td>
<td>—</td>
<td>4</td>
<td>—</td>
</tr>
<tr>
<td>tsu</td>
<td>—</td>
<td>Setup Time, Input or Feedback before Clock↑</td>
<td>6</td>
<td>—</td>
<td>8</td>
</tr>
<tr>
<td>th</td>
<td>—</td>
<td>Hold Time, Input or Feedback after Clock↑</td>
<td>0</td>
<td>—</td>
<td>0</td>
</tr>
<tr>
<td>fmax³</td>
<td>A</td>
<td>Maximum Clock Frequency with External Feedback, 1/(tsu + tco)</td>
<td>76.9</td>
<td>—</td>
<td>62.5</td>
</tr>
<tr>
<td></td>
<td>A</td>
<td>Maximum Clock Frequency with Internal Feedback, 1/(tsu + tfcf)</td>
<td>100</td>
<td>—</td>
<td>83.3</td>
</tr>
<tr>
<td></td>
<td>A</td>
<td>Maximum Clock Frequency with No Feedback</td>
<td>100</td>
<td>—</td>
<td>83.3</td>
</tr>
<tr>
<td>twh</td>
<td>—</td>
<td>Clock Pulse Duration, High</td>
<td>4</td>
<td>—</td>
<td>6</td>
</tr>
<tr>
<td>twl</td>
<td>—</td>
<td>Clock Pulse Duration, Low</td>
<td>4</td>
<td>—</td>
<td>6</td>
</tr>
<tr>
<td>ten</td>
<td>B</td>
<td>Input or I/O to Output Enabled</td>
<td>3</td>
<td>10</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>OE to Output Enabled</td>
<td>2</td>
<td>9</td>
<td>2</td>
</tr>
<tr>
<td>tdis</td>
<td>C</td>
<td>Input or I/O to Output Disabled</td>
<td>3</td>
<td>9</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>C</td>
<td>OE to Output Disabled</td>
<td>2</td>
<td>9</td>
<td>2</td>
</tr>
</tbody>
</table>

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

---

### Capacitance (TA = 25°C, f = 1.0 MHz)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MAXIMUM*</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ci</td>
<td>Input Capacitance</td>
<td>8</td>
<td>pF</td>
<td>VCC = 5.0V, VI = 2.0V</td>
</tr>
<tr>
<td>C1O</td>
<td>I/O Capacitance</td>
<td>8</td>
<td>pF</td>
<td>VCC = 5.0V, VO = 2.0V</td>
</tr>
</tbody>
</table>

*Characterized but not 100% tested
Specifications GAL20XV10

Switching Waveforms

<table>
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<tr>
<th>INPUT or I/O FEEDBACK</th>
<th>INPUT or I/O FEEDBACK</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>COMBINATORIAL OUTPUT</strong></td>
<td><strong>VALID INPUT</strong></td>
</tr>
<tr>
<td></td>
<td>tpd</td>
</tr>
<tr>
<td></td>
<td>Combinatorial Output</td>
</tr>
<tr>
<td><strong>INPUT or I/O FEEDBACK</strong></td>
<td><strong>OUTPUT</strong></td>
</tr>
<tr>
<td></td>
<td>tds teN</td>
</tr>
<tr>
<td></td>
<td>Output or I/O Feedback to Enable/Disable</td>
</tr>
<tr>
<td><strong>CLK</strong></td>
<td><strong>INPUT or I/O FEEDBACK</strong></td>
</tr>
<tr>
<td></td>
<td>tsu th</td>
</tr>
<tr>
<td></td>
<td>Registered Output</td>
</tr>
<tr>
<td><strong>OE</strong></td>
<td><strong>OUTPUT</strong></td>
</tr>
<tr>
<td></td>
<td>tdis ten</td>
</tr>
<tr>
<td></td>
<td>OE to Output Enable/Disable</td>
</tr>
<tr>
<td><strong>CLK</strong></td>
<td><strong>REGISTERED FEEDBACK</strong></td>
</tr>
<tr>
<td></td>
<td>1/fmax (internal fdbk)</td>
</tr>
<tr>
<td></td>
<td>fmax with Feedback</td>
</tr>
</tbody>
</table>

Clock Width

**Input/Output Equivalent Schematics**

Typical Input

Typical Output
Specifications **GAL20XV10**

**fmax Descriptions**

### fmax with External Feedback 1/(tsu+tco)

- **Note:** \( f_{max} \) with external feedback is calculated from measured \( tsu \) and \( tco \).

### fmax with Internal Feedback 1/(tsu+tcf)

- **Note:** \( tcf \) is a calculated value, derived by subtracting \( tsu \) from the period of \( f_{max} \) w/internal feedback (\( tcf = 1/f_{max} - tsu \)). The value of \( tcf \) is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to \( tcf + tpd \).

### fmax with No Feedback

- **Note:** \( f_{max} \) with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.

**Switching Test Conditions**

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>GND to 3.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise and Fall Times</td>
<td>3ns 10% – 90%</td>
</tr>
<tr>
<td>Input Timing Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Timing Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Load</td>
<td>See Figure</td>
</tr>
</tbody>
</table>

3-state levels are measured 0.5V from steady-state active level.

**Output Load Conditions (see figure)**

<table>
<thead>
<tr>
<th>Test Condition</th>
<th>( R_1 )</th>
<th>( R_2 )</th>
<th>( C_L )</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>300Ω</td>
<td>390Ω</td>
<td>50pF</td>
</tr>
<tr>
<td>B</td>
<td></td>
<td>390Ω</td>
<td>50pF</td>
</tr>
<tr>
<td>C</td>
<td></td>
<td>390Ω</td>
<td>5pF</td>
</tr>
</tbody>
</table>

Active High

Active Low

\( *C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE * \)

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Electronic Signature

An electronic signature word is provided in every GAL20XV10 device. It contains 40 bits of reprogrammable memory that contains user defined data. Some uses include user ID codes, revision numbers, pattern identification or inventory control codes. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature bits, if programmed to any value other then zero(0) will alter the checksum of the device.

Security Cell

A security cell is provided in every GAL20XV10 device as a deterrent to unauthorized copying of the device pattern. Once programmed, this cell prevents further read access of the device pattern information. This cell can be only be reset by reprogramming the device. The original pattern can never be examined once this cell is programmed. The Electronic Signature is always available regardless of the security cell state.

Device Programming

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes less than a second. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Latch-Up Protection

GAL20XV10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

Input Buffers

GAL20XV10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

GAL20XV10 input buffers have active pull-ups within their input structure. This pull-up will cause any un-terminated input or I/O to float to a TTL high (logical 1). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce Icc for the device.

Power-Up Reset

Circuitry within the GAL20XV10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the GAL20XV10. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.
Specifications GAL20XV10

Typical AC and DC Characteristic Diagrams

Normalized Tpd vs Vcc

Normalized Tco vs Vcc

Normalized Tsu vs Vcc

Normalized Tpd vs Temp

Normalized Tco vs Temp

Normalized Tsu vs Temp

Delta Tpd vs # of Outputs Switching

Delta Tco vs # of Outputs Switching

Delta Tpd vs Output Loading

Delta Tco vs Output Loading

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