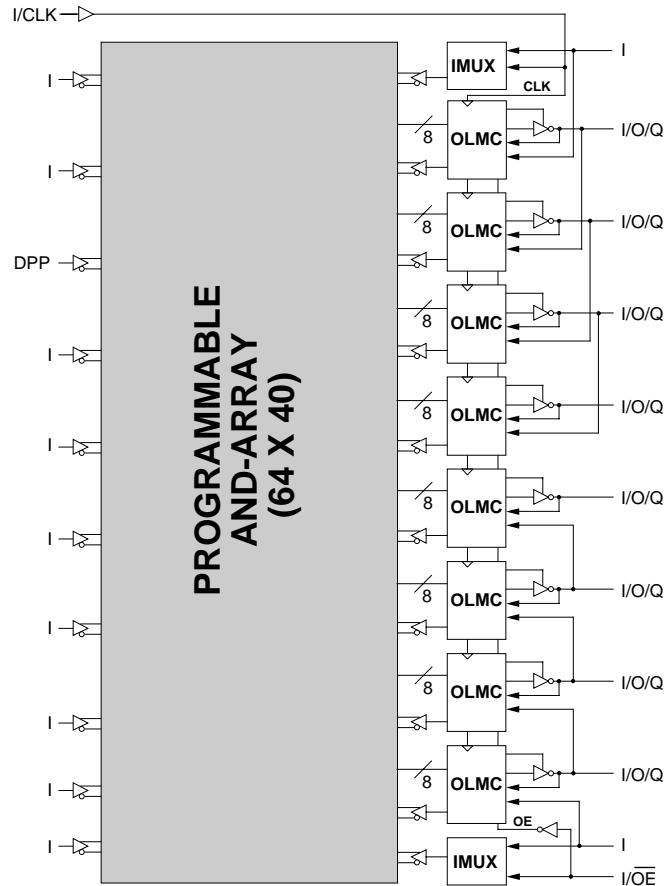


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## Features

- **3.3V LOW VOLTAGE, ZERO POWER OPERATION**
  - JEDEC Compatible 3.3V Interface Standard
  - Interfaces with Standard 5V TTL Devices
  - 50µA Typical Standby Current (100µA Max.)
  - 45mA Typical Active Current (55mA Max.)
  - Dedicated Power-down Pin
- **HIGH PERFORMANCE E<sup>2</sup>CMOS TECHNOLOGY**
  - TTL Compatible Balanced 8 mA Output Drive
  - 15 ns Maximum Propagation Delay
  - F<sub>max</sub> = 62.5 MHz
  - 10 ns Maximum from Clock Input to Data Output
  - UltraMOS<sup>®</sup> Advanced CMOS Technology
- **E<sup>2</sup> CELL TECHNOLOGY**
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
  - Glue Logic for 3.3V Systems
  - Ideal for Mixed 3.3V and 5V Systems
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

## Functional Block Diagram



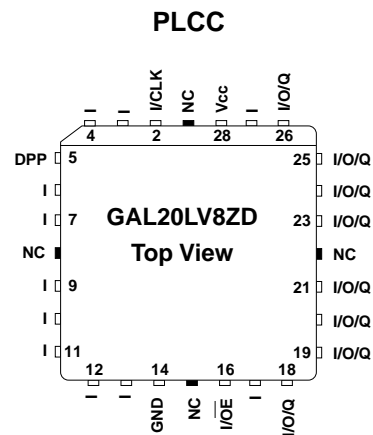
## Description

The GAL20LV8ZD, at 100 µA standby current and 15ns propagation delay provides the highest speed low-voltage PLD available in the market. The GAL20LV8ZD is manufactured using Lattice Semiconductor's advanced 3.3V E<sup>2</sup>CMOS process, which combines CMOS with Electrically Erasable (E<sup>2</sup>) floating gate technology.

The GAL20LV8ZD utilizes a dedicated power-down pin (DPP) to put the device into standby mode. It has 19 inputs available to the AND array and is capable of interfacing with both 3.3V and standard 5V devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

## Pin Configuration



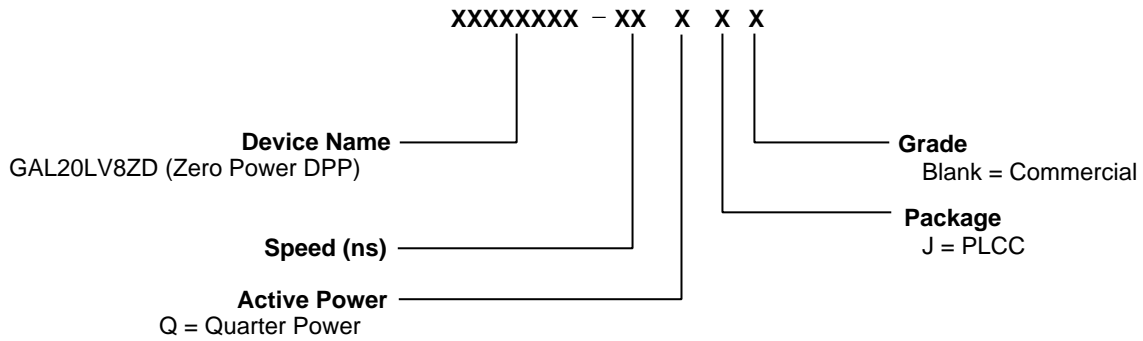
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**GAL20LV8ZD Ordering Information**

**Commercial Grade Specifications**

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	I <sub>sb</sub> (μA)	Ordering #	Package
15	12	10	55	100	GAL20LV8ZD-15QJ	28-Lead PLCC
25	15	15	55	100	GAL20LV8ZD-25QJ	28-Lead PLCC

**Part Number Description**



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## Output Logic Macrocell (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of

each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL20LV8ZD. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

## Compiler Support for OLMC

Software compilers support the three different global OLMC modes as different device types. Most compilers also have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 2 and pin 16 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 2 and pin 16 become dedicated inputs and use the feedback paths of pin 26 and pin 18 respectively. Because of this feedback path usage, pin 26 and pin 18 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins ( pins 21 and 23) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

When using the standard GAL20V8 JEDEC fuse pattern generated by the logic compilers for the GAL20LV8ZD, special attention must be given to pin 5 (DPP) to make sure that it is not used as one of the functional inputs.

**Registered Mode**

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 20R8 and 20RP4 devices with various permutations of polarity, I/O and register placement.

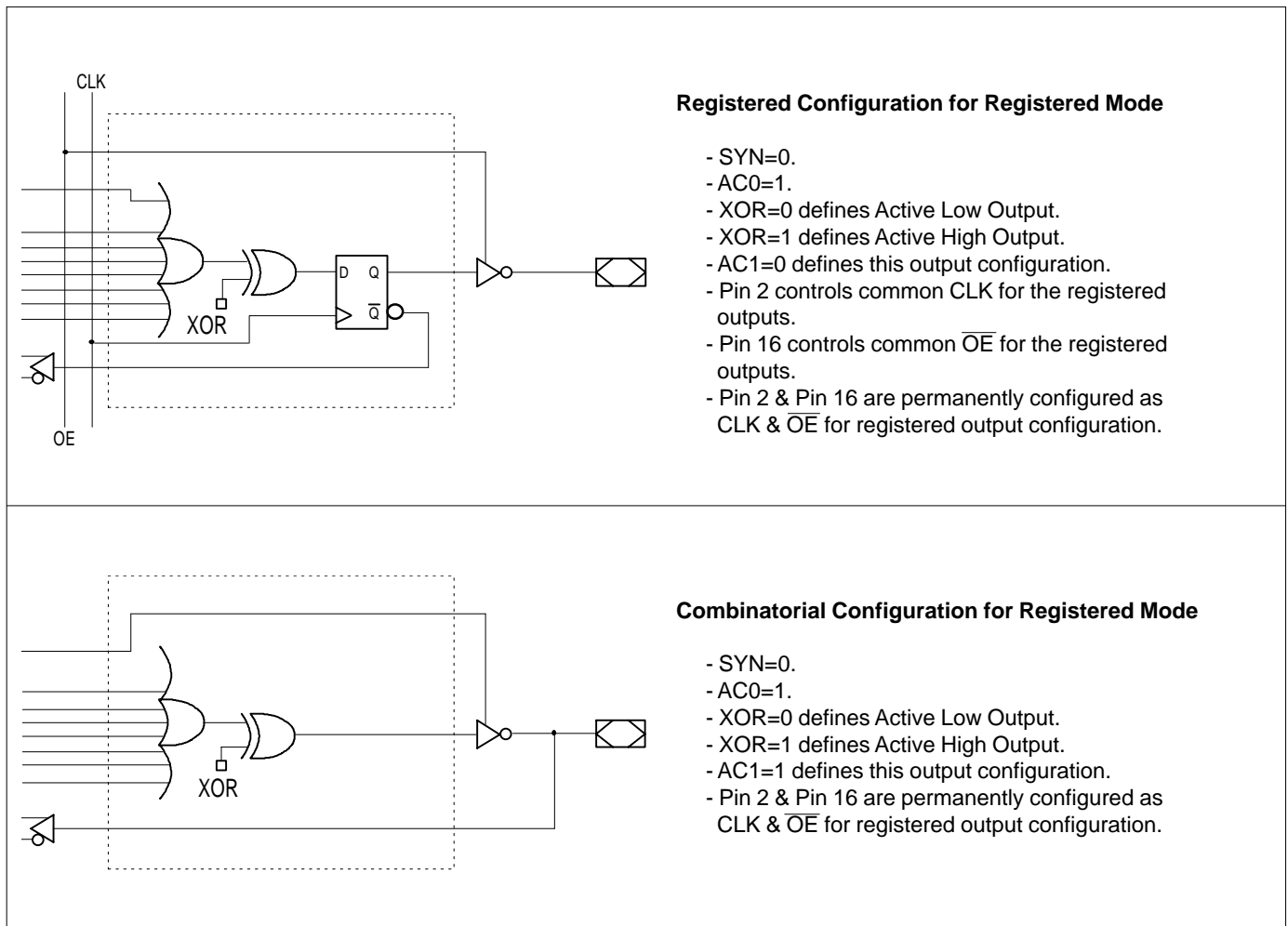
All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/Os are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

Registered outputs have eight product terms per output. I/Os have seven product terms per output.

Pin 5 is used as dedicated power-down pin on GAL20LV8ZD. It cannot be used as functional input.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.

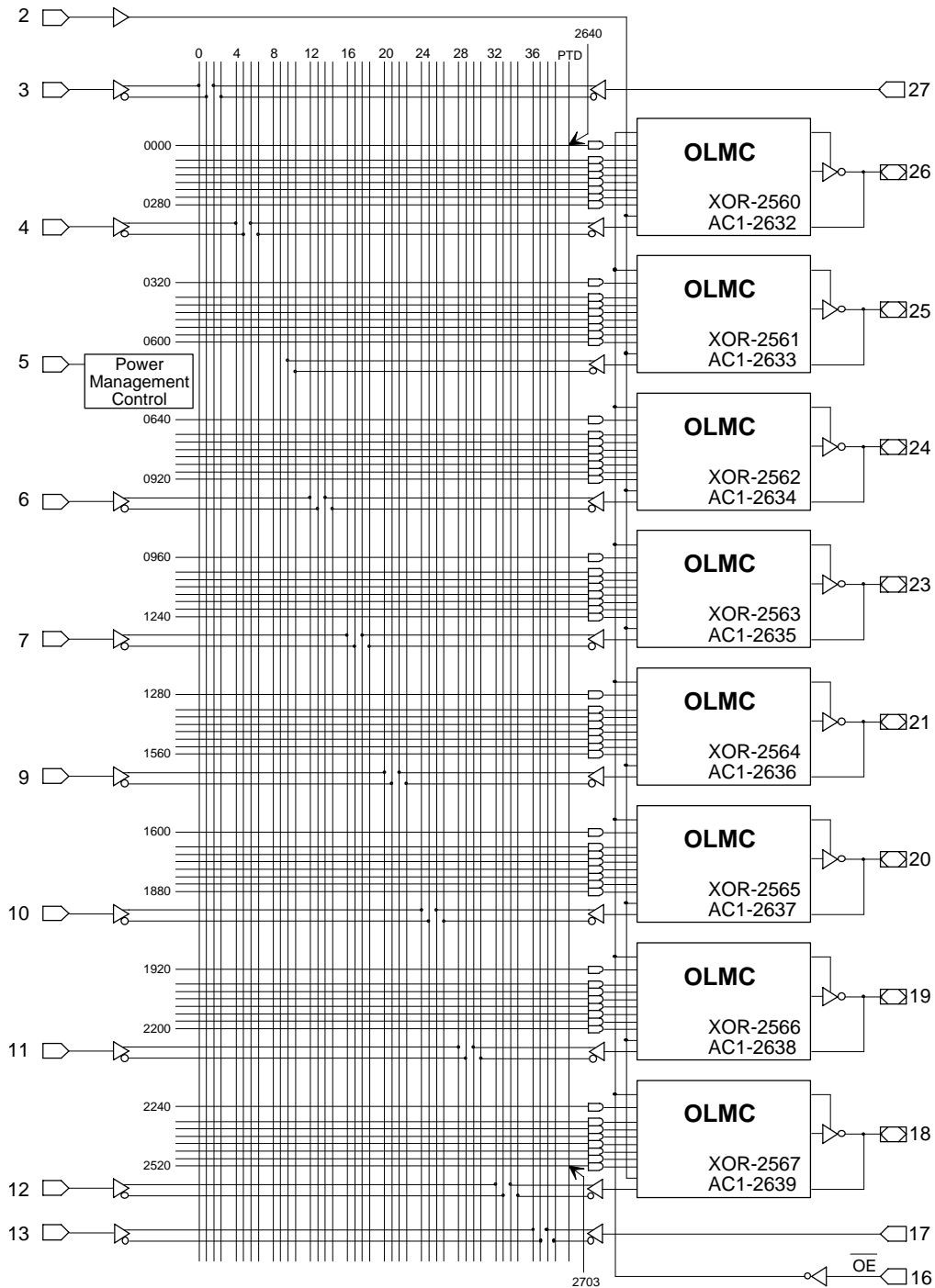
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Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

**Registered Mode Logic Diagram**

PLCC Package Pinout



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ....	.... 2630, 2631
Byte7   Byte6   ....	.... Byte1   Byte0

MSB      LSB

SYN-2704  
AC0-2705

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**Complex Mode**

In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 20L8 and 20P8 devices with programmable polarity in each macrocell.

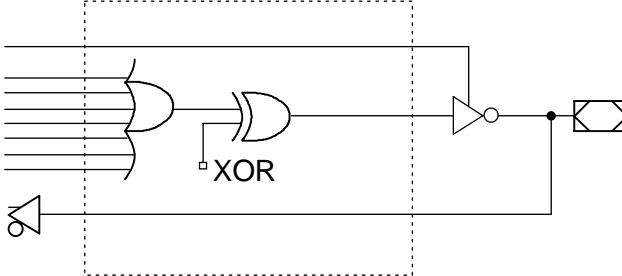
Up to six I/Os are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 18 & 26) do not have input capability. Designs requiring eight I/Os can be implemented in the Registered mode.

All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 2 and 16 are always available as data inputs into the AND array.

Pin 5 is used as dedicated power-down pin on GAL20LV8ZD. It cannot be used as functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.

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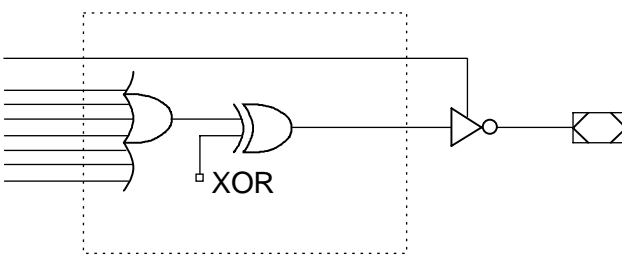


The diagram shows a macrocell with a 7-input OR gate, a 2-input AND gate, and an XOR gate. The OR gate has 7 inputs, one of which is inverted. The AND gate has 2 inputs, one of which is inverted. The XOR gate has 2 inputs, one of which is inverted. The output of the AND gate is connected to the output of the OR gate. The output of the OR gate is connected to an output buffer. The output of the XOR gate is connected to the output buffer. The output buffer is connected to a pin.

**Combinatorial I/O Configuration for Complex Mode**

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 19 through Pin 25 are configured to this function.

---



The diagram shows a macrocell with a 7-input OR gate, a 2-input AND gate, and an XOR gate. The OR gate has 7 inputs, one of which is inverted. The AND gate has 2 inputs, one of which is inverted. The XOR gate has 2 inputs, one of which is inverted. The output of the AND gate is connected to the output of the OR gate. The output of the OR gate is connected to an output buffer. The output of the XOR gate is connected to the output buffer. The output buffer is connected to a pin.

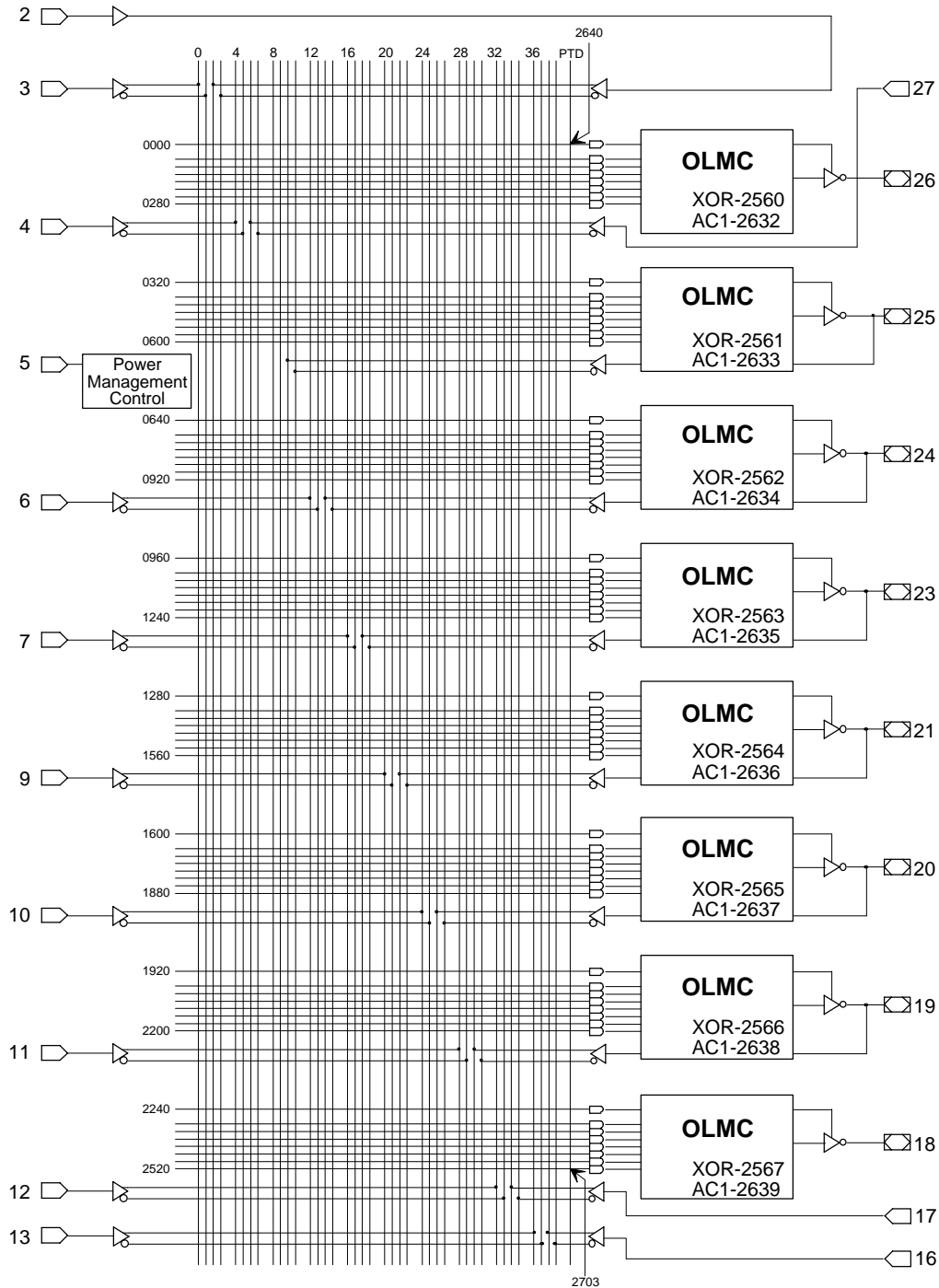
**Combinatorial Output Configuration for Complex Mode**

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 18 and Pin 26 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

**Complex Mode Logic Diagram**

PLCC Package Pinout



64-USER ELECTRONIC SIGNATURE FUSES			
2568, 2569, ....	....	2630, 2631	
Byte7	Byte6	....	Byte1   Byte0
MSB	LSB		

SYN-2704  
AC0-2705

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## Simple Mode

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 14L8 and 16P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

Pins 2 and 16 are always available as data inputs into the AND array. The center two macrocells (pins 21 & 23) cannot be used in the input configuration.

Pin 5 is used as dedicated power-down pin on GAL20LV8ZD. It cannot be used as functional input.

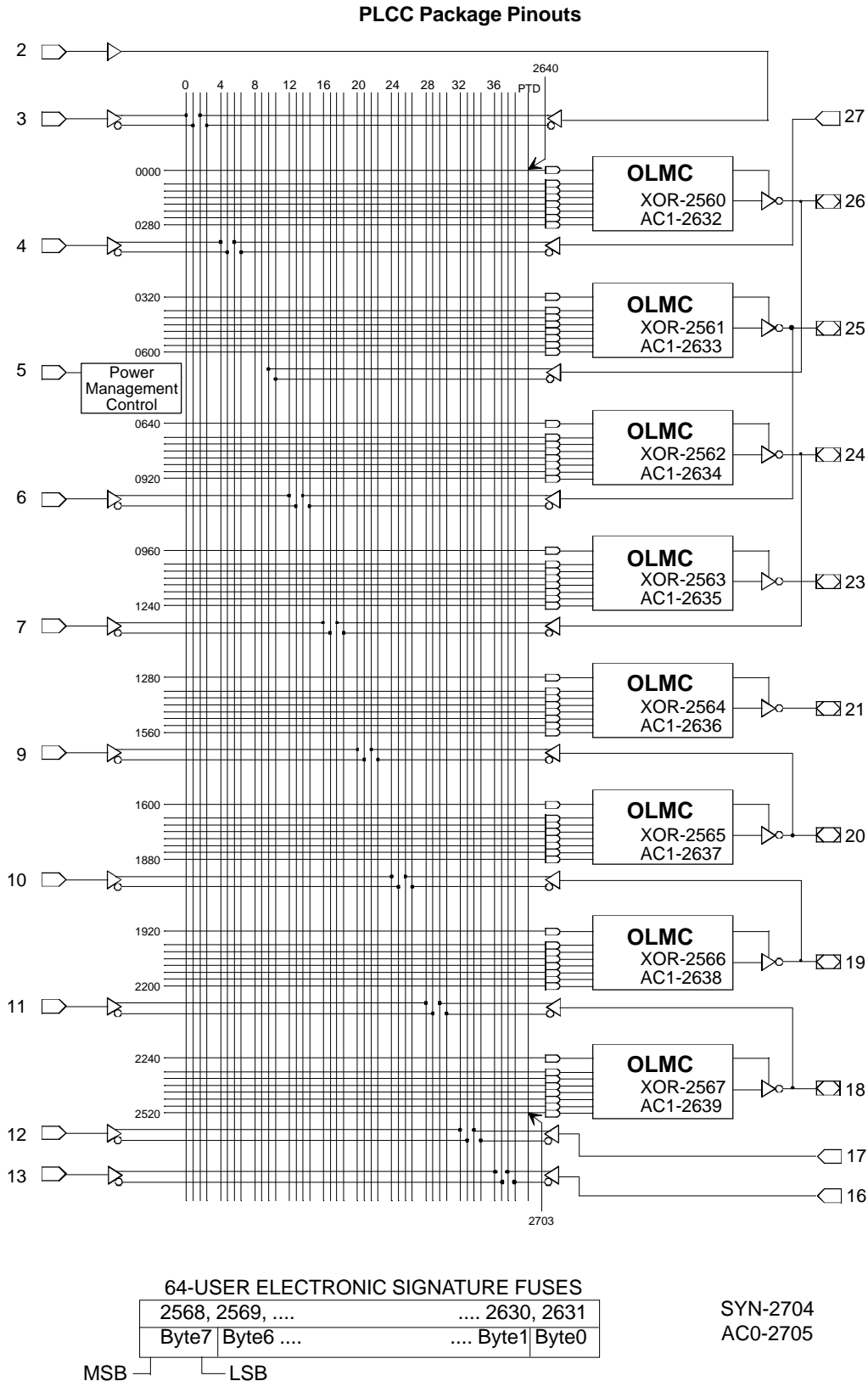
The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.

	<p><b>Combinatorial Output with Feedback Configuration for Simple Mode</b></p> <ul style="list-style-type: none"> <li>- SYN=1.</li> <li>- AC0=0.</li> <li>- XOR=0 defines Active Low Output.</li> <li>- XOR=1 defines Active High Output.</li> <li>- AC1=0 defines this configuration.</li> <li>- All OLMC <b>except</b> pins 21 &amp; 23 can be configured to this function.</li> </ul>
	<p><b>Combinatorial Output Configuration for Simple Mode</b></p> <ul style="list-style-type: none"> <li>- SYN=1.</li> <li>- AC0=0.</li> <li>- XOR=0 defines Active Low Output.</li> <li>- XOR=1 defines Active High Output.</li> <li>- AC1=0 defines this configuration.</li> <li>- Pins 21 &amp; 23 are permanently configured to this function.</li> </ul>
	<p><b>Dedicated Input Configuration for Simple Mode</b></p> <ul style="list-style-type: none"> <li>- SYN=1.</li> <li>- AC0=0.</li> <li>- XOR=0 defines Active Low Output.</li> <li>- XOR=1 defines Active High Output.</li> <li>- AC1=1 defines this configuration.</li> <li>- All OLMC <b>except</b> pins 21 &amp; 23 can be configured to this function.</li> </ul>

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.



**Simple Mode Logic Diagram**



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## Absolute Maximum Ratings<sup>(1)</sup>

Supply voltage $V_{CC}$ .....	-0.5 to +5.6V
Input voltage applied .....	-0.5 to +5.6V
Off-state output voltage applied .....	-0.5 to +5.6V
Storage Temperature .....	-65 to 150°C
Ambient Temperature with Power Applied .....	-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

## Recommended Operating Conditions

<b>Commercial Devices:</b>	
Ambient Temperature ( $T_A$ ) .....	0 to +75°C
Supply voltage ( $V_{CC}$ ) with Respect to Ground .....	+3.0 to +3.6V

## DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. <sup>2</sup>	MAX.	UNITS
$V_{IL}$	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
$V_{IH}$	Input High Voltage		2.0	—	5.25	V
$I_{IL}$	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-10	$\mu A$
$I_{IH}$	Input or I/O High Leakage Current	$(V_{CC}-0.2)V \leq V_{IN} \leq V_{CC}$	—	—	10	$\mu A$
		$V_{CC} \leq V_{IN} \leq 5.25V$	—	—	1	mA
$V_{OL}$	Output Low Voltage	$I_{OL} = MAX. \quad V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
		$I_{OL} = 0.5 \text{ mA} \quad V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.2	V
$V_{OH}$	Output High Voltage	$I_{OH} = MAX. \quad V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
		$I_{OH} = -0.5 \text{ mA} \quad V_{in} = V_{IL} \text{ or } V_{IH}$	$V_{CC}-0.45$	—	—	V
		$I_{OH} = -100\mu A \quad V_{in} = V_{IL} \text{ or } V_{IH}$	$V_{CC}-0.2$	—	—	V
$I_{OL}$	Low Level Output Current		—	—	8	mA
$I_{OH}$	High Level Output Current		—	—	-8	mA
$I_{OS}^1$	Output Short Circuit Current	$V_{CC} = 3.3V \quad V_{OUT} = GND \quad T_A = 25^\circ C$	-30	—	-130	mA

## COMMERCIAL

$I_{SB}$	Stand-by Power Supply Current	$V_{IL} = GND \quad V_{IH} = V_{CC} \quad \text{Outputs Open}$	ZD -15/-25	—	50	100	$\mu A$
$I_{CC}$	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15 \text{ MHz} \quad \text{Outputs Open}$	ZD -15/-25	—	45	55	mA

1) One output at a time for a maximum duration of one second.  $V_{out} = 0.5V$  was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.

2) Typical values are at  $V_{CC} = 3.3V$  and  $T_A = 25^\circ C$

## AC Switching Characteristics

Over Recommended Operating Conditions

PARAM	TEST COND. <sup>1</sup>	DESCRIPTION	COM		COM		UNITS
			-15		-25		
			MIN.	MAX.	MIN.	MAX.	
<b>t<sub>pd</sub></b>	A	Input or I/O to Combinatorial Output	3	15	3	25	ns
<b>t<sub>co</sub></b>	A	Clock to Output Delay	2	10	2	15	ns
<b>t<sub>cf</sub><sup>2</sup></b>	—	Clock to Feedback Delay	—	8	—	10	ns
<b>t<sub>su</sub></b>	—	Setup Time, Input or Fdbk before Clk↑	12	—	15	—	ns
<b>t<sub>h</sub></b>	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	ns
<b>f<sub>max</sub><sup>3</sup></b>	A	Maximum Clock Frequency with External Feedback, 1/(t <sub>su</sub> + t <sub>co</sub> )	45.5	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t <sub>su</sub> + t <sub>cf</sub> )	50	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback	62.5	—	41.6	—	MHz
<b>t<sub>wh</sub></b>	—	Clock Pulse Duration, High	8	—	12	—	ns
<b>t<sub>wl</sub></b>	—	Clock Pulse Duration, Low	8	—	12	—	ns
<b>t<sub>en</sub></b>	B	Input or I/O to Output Enabled	—	17	—	25	ns
	B	OE↓ to Output Enabled	—	16	—	20	ns
<b>t<sub>dis</sub></b>	C	Input or I/O to Output Disabled	—	18	—	25	ns
	C	OE↑ to Output Disabled	—	17	—	20	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f<sub>max</sub> with internal feedback. Refer to **f<sub>max</sub> Description** section.

3) Refer to **f<sub>max</sub> Description** section.

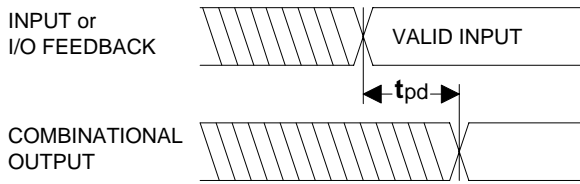
## Capacitance (T<sub>A</sub> = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C <sub>I</sub>	Input Capacitance	8	pF	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V
C <sub>I/O</sub>	I/O Capacitance	8	pF	V <sub>CC</sub> = 3.3V, V <sub>I/O</sub> = 0V

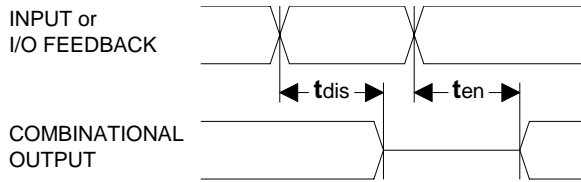
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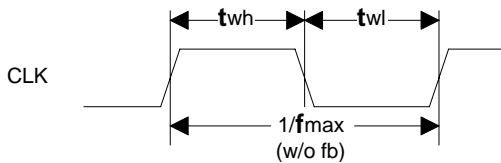
**Switching Waveforms**



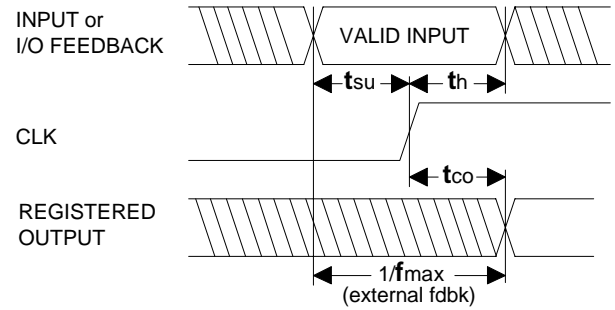
**Combinatorial Output**



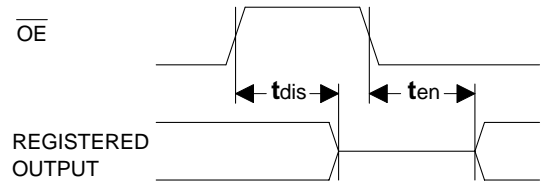
**Input or I/O to Output Enable/Disable**



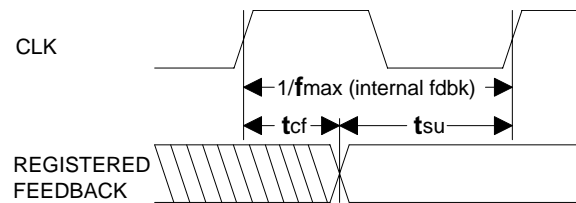
**Clock Width**



**Registered Output**



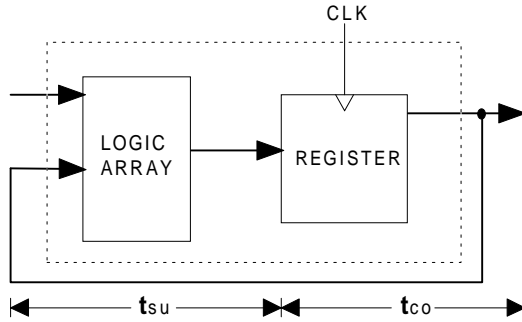
**OE to Output Enable/Disable**



**fmax with Feedback**

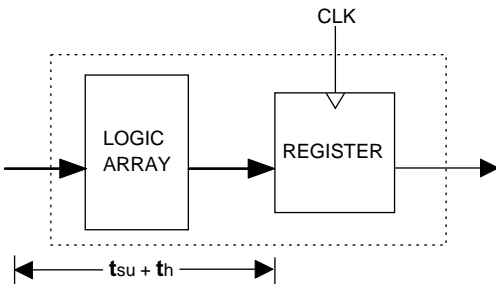
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**fmax Descriptions**



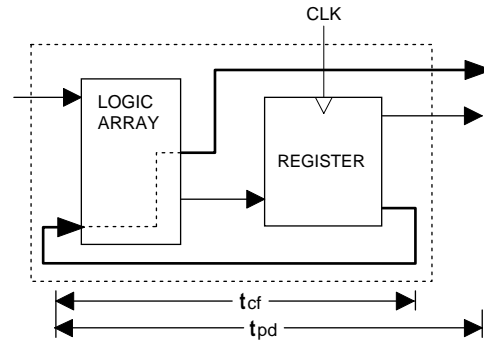
**fmax with External Feedback  $1/(tsu+tco)$**

**Note:** fmax with external feedback is calculated from measured tsu and tco.



**fmax with No Feedback**

**Note:** fmax with no feedback may be less than  $1/(twh + twl)$ . This is to allow for a clock duty cycle of other than 50%.



**fmax with Internal Feedback  $1/(tsu+tcf)$**

**Note:** tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback ( $tcf = 1/fmax - tsu$ ). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to  $tcf + tpd$ .

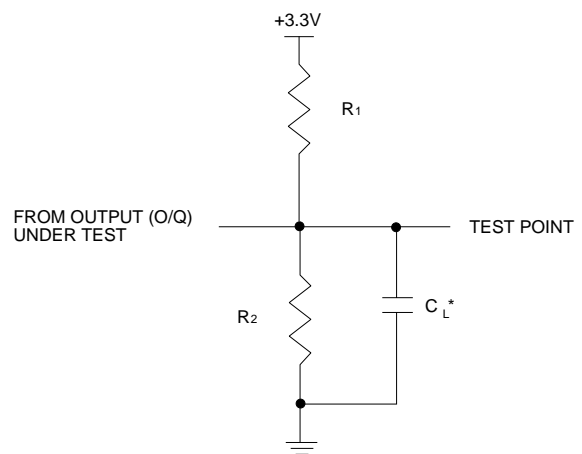
**Switching Test Conditions**

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	2ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level. 3-state to active transitions are measured at  $(Voh - 0.5)$  V and  $(Vol + 0.5)$  V.

**Output Load Conditions (see figure)**

Test Condition	R1	R2	CL
A	270Ω	220Ω	35pF
B	270Ω	220Ω	Active High 35pF
			Active Low 35pF
C	270Ω	220Ω	Active High 5pF
			Active Low 5pF



\*CL INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

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## Electronic Signature

An electronic signature word is provided in every GAL20LV8ZD device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter checksum.

## Security Cell

A security cell is provided in the GAL20LV8ZD devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The electronic signature data is always available to the user, regardless of the state of this security cell.

## Device Programming

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

## Output Register Preload

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

The GAL20LV8ZD devices includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

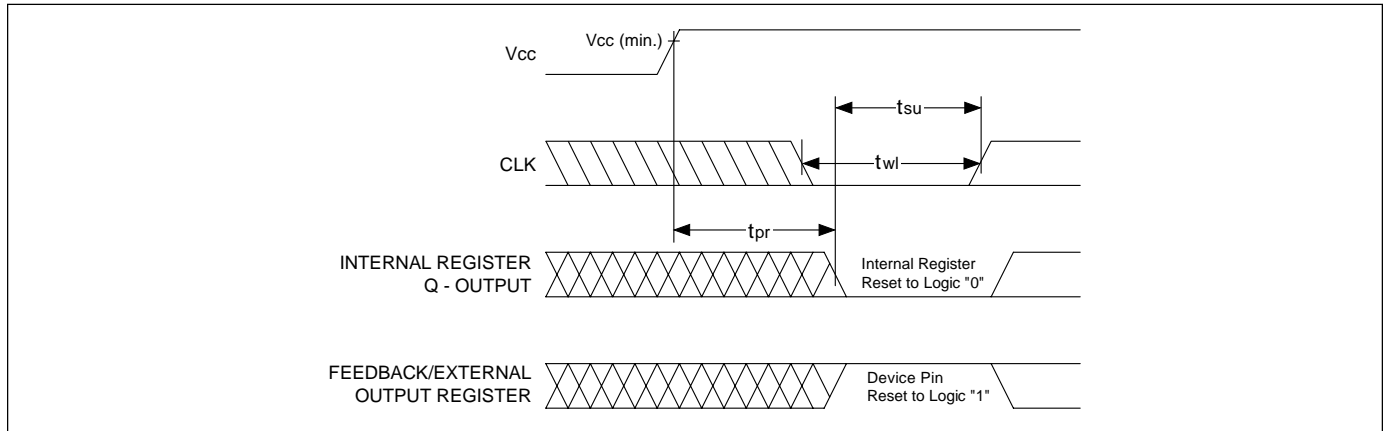
## Input Buffers

GAL20LV8ZD devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

## Dedicated Power-Down Pin

The GAL20LV8ZD uses pin 5 as the dedicated power-down signal to put the device in to the power-down state. DPP is an active high signal where a logic high driven on this signal puts the device into power-down state. Input pin 5 cannot be used as a logic function input on this device.

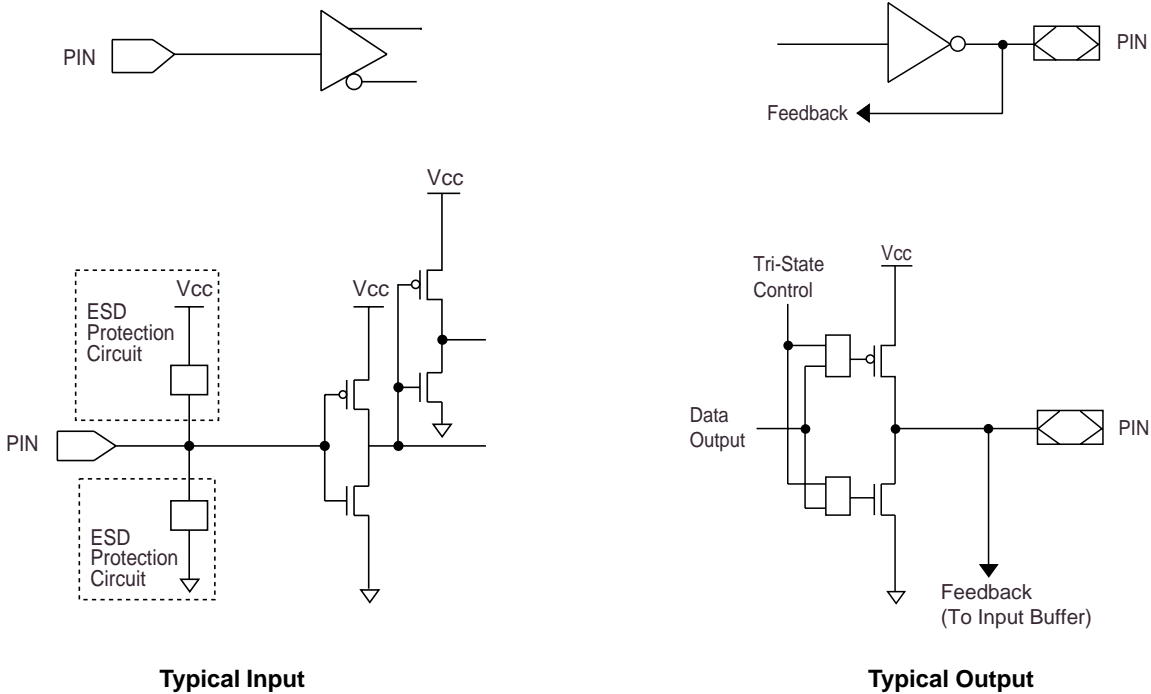
**Power-Up Reset**



Circuitry within the GAL20LV8ZD provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t<sub>pr</sub>, 10μs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the

asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the GAL20LV8ZD. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t<sub>pr</sub> time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

**Input/Output Equivalent Schematic**



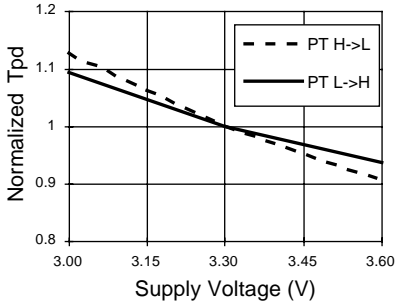
Discontinued Product (PCN #02-06). Contact Rochester Electronics for Availability. [www.latticesemi.com/sales/discontinueddevicesales.cfm](http://www.latticesemi.com/sales/discontinueddevicesales.cfm)



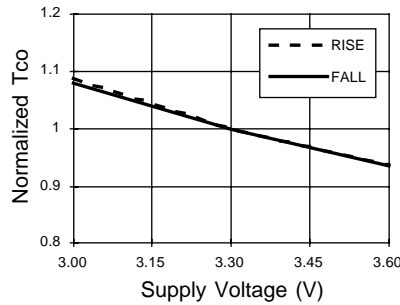
**Typical AC and DC Characteristics**

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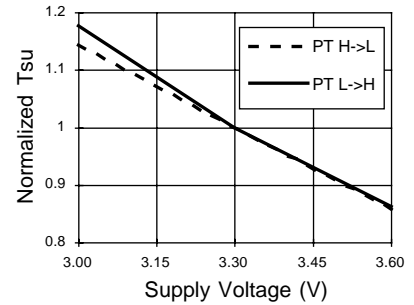
**Normalized Tpd vs Vcc**



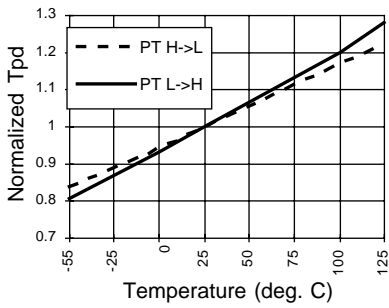
**Normalized Tco vs Vcc**



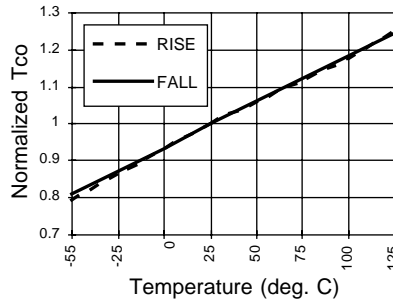
**Normalized Tsu vs Vcc**



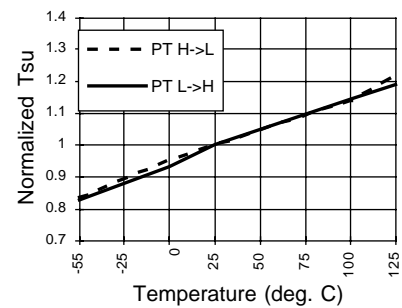
**Normalized Tpd vs Temp**



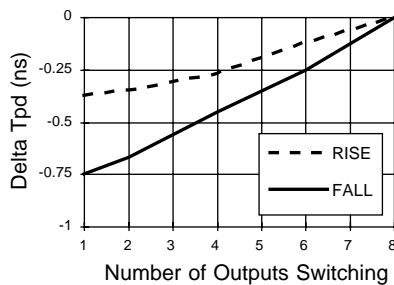
**Normalized Tco vs Temp**



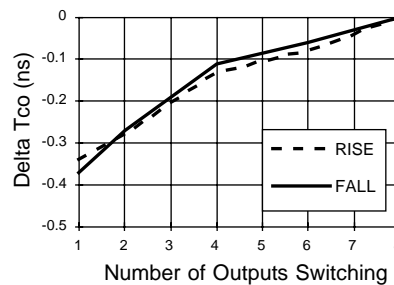
**Normalized Tsu vs Temp**



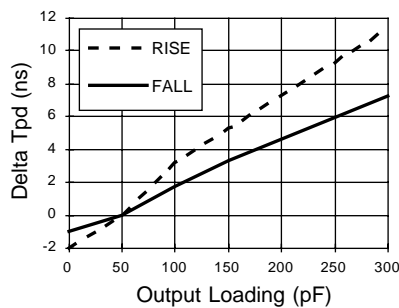
**Delta Tpd vs # of Outputs Switching**



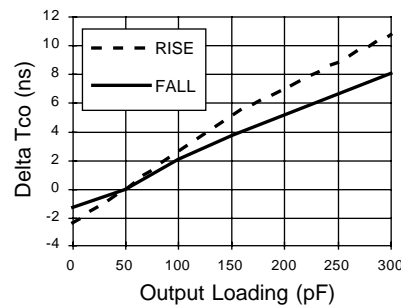
**Delta Tco vs # of Outputs Switching**



**Delta Tpd vs Output Loading**

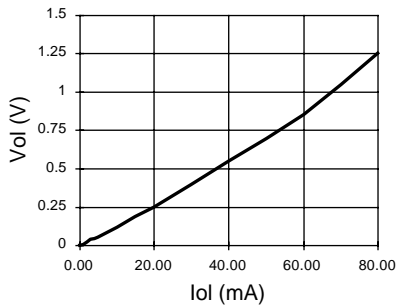


**Delta Tco vs Output Loading**

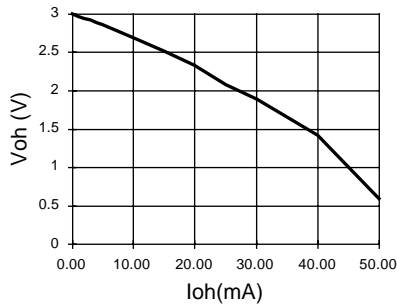


**Typical AC and DC Characteristics**

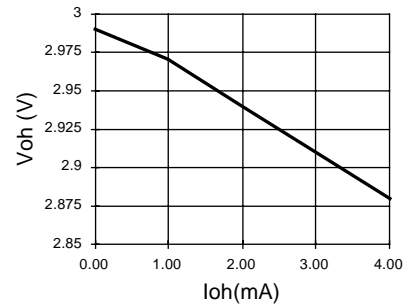
**Vol vs Iol**



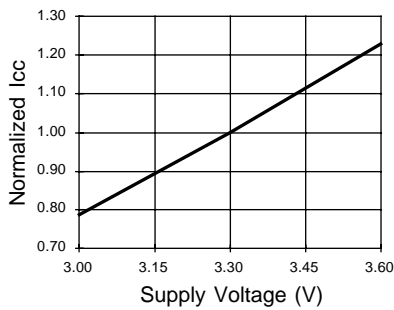
**Voh vs Ioh**



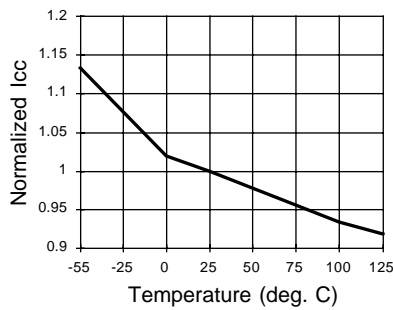
**Voh vs Ioh**



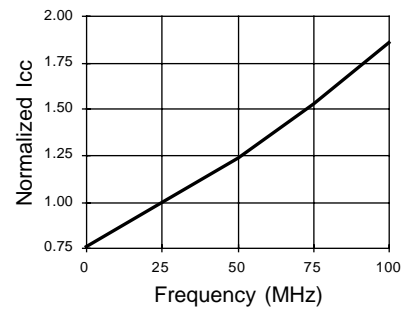
**Normalized Icc vs Vcc**



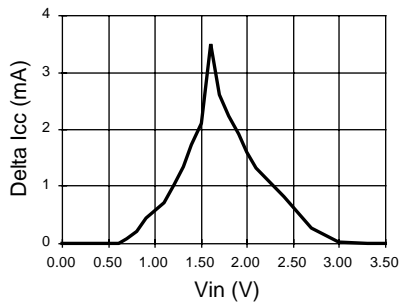
**Normalized Icc vs Temp**



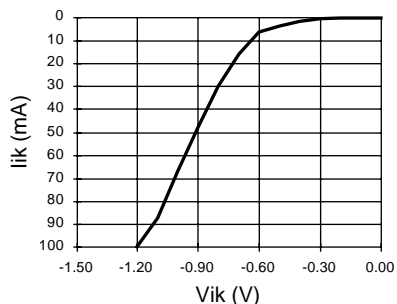
**Normalized Icc vs Freq.**



**Delta Icc vs Vin (1 input)**



**Input Clamp (Iik)**



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