Features

- **3.3V LOW VOLTAGE, ZERO POWER OPERATION**
  - JEDEC Compatible 3.3V Interface Standard
  - Interfaces with Standard 5V TTL Devices
  - 50μA Typical Standby Current (100μA Max.)
  - 45mA Typical Active Current (55mA Max.)
  - Dedicated Power-down Pin

- **HIGH PERFORMANCE E2CMOS TECHNOLOGY**
  - TTL Compatible Balanced 8 mA Output Drive
  - Fmax = 62.5 MHz
  - 10 ns Maximum from Clock Input to Data Output
  - UltraMOS® Advanced CMOS Technology

- **E2 CELL TECHNOLOGY**
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention

- **EIGHT OUTPUT LOGIC MACROCELLS**
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity

- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - 100% Functional Testability

- **APPLICATIONS INCLUDE:**
  - Glue Logic for 3.3V Systems
  - Ideal for Mixed 3.3V and 5V Systems

- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

Description

The GAL20LV8ZD, at 100 μA standby current and 15 ns propagation delay provides the highest speed low-voltage PLD available in the market. The GAL20LV8ZD is manufactured using Lattice Semiconductor’s advanced 3.3V E2CMOS process, which combines CMOS with Electrically Erasable (E2) floating gate technology.

The GAL20LV8ZD utilizes a dedicated power-down pin (DPP) to put the device into standby mode. It has 19 inputs available to the AND array and is capable of interfacing with both 3.3V and standard 5V devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.
## Specifications GAL20LV8ZD

### GAL20LV8ZD Ordering Information

**Commercial Grade Specifications**

<table>
<thead>
<tr>
<th>Tpd (ns)</th>
<th>Tsu (ns)</th>
<th>Tco (ns)</th>
<th>Icc (mA)</th>
<th>Isb (µA)</th>
<th>Ordering #</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>12</td>
<td>10</td>
<td>55</td>
<td>100</td>
<td>GAL20LV8ZD-15QJ</td>
<td>28-Lead PLCC</td>
</tr>
<tr>
<td>25</td>
<td>15</td>
<td>15</td>
<td>55</td>
<td>100</td>
<td>GAL20LV8ZD-25QJ</td>
<td>28-Lead PLCC</td>
</tr>
</tbody>
</table>

### Part Number Description

**Device Name**
GAL20LV8ZD (Zero Power DPP)

**Speed (ns)**
Q = Quarter Power

**Active Power**

**Grade**
Blank = Commercial

**Package**
J = PLCC

Discontinued Product (PCN #02-06). Contact Rochester Electronics for Availability. www.latticesemi.com/sales/discontinueddevicessales.cfm
Specifications **GAL20LV8ZD**

### Output Logic Macrocell (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL20LV8ZD. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

### Compiler Support for OLMC

Software compilers support the three different global OLMC modes as different device types. Most compilers also have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 2 and pin 16 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 2 and pin 16 become dedicated inputs and use the feedback paths of pin 26 and pin 18 respectively. Because of this feedback path usage, pin 26 and pin 18 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 21 and 23) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

When using the standard GAL20V8 JEDEC fuse pattern generated by the logic compilers for the GAL20LV8ZD, special attention must be given to pin 5 (DPP) to make sure that it is not used as one of the functional inputs.
Registered Mode

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 20R8 and 20RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/Os are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

Registered outputs have eight product terms per output. I/Os have seven product terms per output.

Pin 5 is used as dedicated power-down pin on GAL20LV8ZD. It cannot be used as functional input.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.

Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 2 controls common CLK for the registered outputs.
- Pin 16 controls common OE for the registered outputs.
- Pin 2 & Pin 16 are permanently configured as CLK & OE for registered output configuration.

Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 2 & Pin 16 are permanently configured as CLK & OE for registered output configuration.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.
Specifications GAL20LV8ZD

Registered Mode Logic Diagram

PLCC Package Pinout

64-USER ELECTRONIC SIGNATURE FUSES

- 2568, 2569, ..., 2630, 2631
- Byte7, Byte6, ..., Byte1, Byte0

MSB  LSB

SYN-2704
AC0-2705

Discontinued Product (PCN #02-06). Contact Rochester Electronics for Availability.

www.latticesemi.com/sales/discontinueddevicessales.cfm
Complex Mode

In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 20L8 and 20P8 devices with programmable polarity in each macrocell.

Up to six I/Os are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 18 & 26) do not have input capability. Designs requiring eight I/Os can be implemented in the Registered mode.

All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 2 and 16 are always available as data inputs into the AND array.

Pin 5 is used as dedicated power-down pin on GAL20LV8ZD. It cannot be used as functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 19 through Pin 25 are configured to this function.

Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 18 and Pin 26 are configured to this function.
Complex Mode Logic Diagram

PLCC Package Pinout

64-USER ELECTRONIC SIGNATURE FUSES

<table>
<thead>
<tr>
<th>MSB</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte7</td>
<td>Byte6</td>
</tr>
<tr>
<td>....</td>
<td>....</td>
</tr>
<tr>
<td>2568, 2569, ....</td>
<td>.... 2630, 2631</td>
</tr>
</tbody>
</table>

SYN-2704
AC0-2705
**Simple Mode**

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 14L8 and 16P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

Pins 2 and 16 are always available as data inputs into the AND array. The center two macrocells (pins 21 & 23) cannot be used in the input configuration.

Pin 5 is used as dedicated power-down pin on GAL20LV8ZD. It cannot be used as functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.

---

**Combinatorial Output with Feedback Configuration for Simple Mode**

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC except pins 21 & 23 can be configured to this function.

**Combinatorial Output Configuration for Simple Mode**

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 21 & 23 are permanently configured to this function.

**Dedicated Input Configuration for Simple Mode**

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC except pins 21 & 23 can be configured to this function.

---

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.
Discontinued Product (PCN #02-06). Contact Rochester Electronics for Availability.
**Specifications GAL20LV8ZD**

### Absolute Maximum Ratings\(^{(1)}\)

- Supply voltage $V_{CC}$: -0.5 to 5.6V
- Input voltage applied: -0.5 to 5.6V
- Off-state output voltage applied: -0.5 to 5.6V
- Storage Temperature: -65 to 150°C
- Power Applied: -55 to 125°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

### Recommended Operating Conditions

**Commercial Devices:**

- Ambient Temperature ($T_A$): 0 to 75°C
- Supply voltage ($V_{CC}$) with Respect to Ground: +3.0 to +3.6V

### DC Electrical Characteristics

**Over Recommended Operating Conditions (Unless Otherwise Specified)**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN.</th>
<th>TYP.(^{2} )</th>
<th>MAX.</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>$V_{ss} - 0.5$</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>2.0</td>
<td>—</td>
<td>5.25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input or I/O Low Leakage Current</td>
<td>$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$</td>
<td>—</td>
<td>—</td>
<td>-10</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input or I/O High Leakage Current</td>
<td>$(V_{CC} - 0.2)V \leq V_{IN} \leq V_{CC}$</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>$I_{OL} = \text{MAX.}$, $V_{in} = V_{IL}$ or $V_{IH}$</td>
<td>—</td>
<td>—</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td>Low Level Output Current</td>
<td>—</td>
<td>—</td>
<td>8</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{OH}$</td>
<td>High Level Output Current</td>
<td>—</td>
<td>—</td>
<td>-8</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td>$I_{OH} = \text{MAX.}$, $V_{in} = V_{IL}$ or $V_{IH}$</td>
<td>2.4</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OH}$</td>
<td>—</td>
<td>$I_{OH} = -0.5\text{ mA}$, $V_{in} = V_{IL}$ or $V_{IH}$, $V_{CC} - 0.45$</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OS}$(^{1})</td>
<td>Output Short Circuit Current</td>
<td>$V_{CC} = 3.3V$, $V_{OUT} = \text{GND}$, $T_A = 25°C$</td>
<td>-30</td>
<td>—</td>
<td>-130</td>
<td>mA</td>
</tr>
</tbody>
</table>

### COMMERCIAL

| ISB | Stand-by Power Supply Current | $V_{IL} = \text{GND}$, $V_{IH} = V_{cc}$, Outputs Open | ZD -15/-25 | — | 100 | µA |
| ICC | Operating Power Supply Current | $V_{IL} = 0.5V$, $V_{IH} = 3.0V$, $f_{.toggle} = 15$ MHz, Outputs Open | ZD -15/-25 | — | 45 | 55 | mA |

1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.

2) Typical values are at $V_{cc} = 3.3V$ and $T_A = 25°C$.

---

Discontinued Product (PCN #02-06). Contact Rochester Electronics for Availability.

www.latticesemi.com/sales/discontinueddevicessales.cfm
### Specifications GAL20LV8ZD

#### AC Switching Characteristics

**Over Recommended Operating Conditions**

<table>
<thead>
<tr>
<th>PARAM</th>
<th>TEST COND.</th>
<th>DESCRIPTION</th>
<th>COM -15</th>
<th>COM -25</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>tpd</td>
<td>A</td>
<td>Input or I/O to Combinatorial Output</td>
<td>3</td>
<td>15</td>
<td>3</td>
</tr>
<tr>
<td>tco</td>
<td>A</td>
<td>Clock to Output Delay</td>
<td>2</td>
<td>10</td>
<td>2</td>
</tr>
<tr>
<td>tfp</td>
<td>—</td>
<td>Clock to Feedback Delay</td>
<td>—</td>
<td>8</td>
<td>—</td>
</tr>
<tr>
<td>tsu</td>
<td>—</td>
<td>Setup Time, Input or Fdbk before Clk↑</td>
<td>12</td>
<td>—</td>
<td>15</td>
</tr>
<tr>
<td>th</td>
<td>—</td>
<td>Hold Time, Input or Fdbk after Clk↑</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>fmax³</td>
<td>A</td>
<td>Maximum Clock Frequency with External Feedback, 1/(tsu + tco)</td>
<td>45.5</td>
<td>—</td>
<td>33.3</td>
</tr>
<tr>
<td></td>
<td>A</td>
<td>Maximum Clock Frequency with Internal Feedback, 1/(tsu + tfp)</td>
<td>50</td>
<td>—</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td>A</td>
<td>Maximum Clock Frequency with No Feedback</td>
<td>62.5</td>
<td>—</td>
<td>41.6</td>
</tr>
<tr>
<td>twh</td>
<td>—</td>
<td>Clock Pulse Duration, High</td>
<td>8</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>twl</td>
<td>—</td>
<td>Clock Pulse Duration, Low</td>
<td>8</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>ten</td>
<td>B</td>
<td>Input or I/O to Output Enabled</td>
<td>—</td>
<td>17</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>OE↓ to Output Enabled</td>
<td>—</td>
<td>16</td>
<td>—</td>
</tr>
<tr>
<td>tdis</td>
<td>C</td>
<td>Input or I/O to Output Disabled</td>
<td>—</td>
<td>18</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>C</td>
<td>OE↑ to Output Disabled</td>
<td>—</td>
<td>17</td>
<td>—</td>
</tr>
</tbody>
</table>

1) Refer to Switching Test Conditions section.
2) Calculated from fmax with internal feedback. Refer to fmax Description section.
3) Refer to fmax Description section.

### Capacitance ($T_A = 25°C$, $f = 1.0$ MHz)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TYPICAL</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_i$</td>
<td>Input Capacitance</td>
<td>8</td>
<td>pF</td>
<td>$V_{cc} = 3.3V, V_i = 0V$</td>
</tr>
<tr>
<td>$C_{IO}$</td>
<td>I/O Capacitance</td>
<td>8</td>
<td>pF</td>
<td>$V_{cc} = 3.3V, V_{sc} = 0V$</td>
</tr>
</tbody>
</table>

Discontinued Product (PCN #02-06). Contact Rochester Electronics for Availability. [www.latticesemi.com/sales/discontinueddevicessales.cfm](http://www.latticesemi.com/sales/discontinueddevicessales.cfm)
### Dedicated Power-Down Pin Specifications

#### Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST COND.</th>
<th>DESCRIPTION</th>
<th>COM -15</th>
<th>COM -25</th>
<th>MIN.</th>
<th>MAX.</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>twhd</td>
<td>—</td>
<td>DPP Pulse Duration High</td>
<td>40</td>
<td>40</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>twlld</td>
<td>—</td>
<td>DPP Pulse Duration Low</td>
<td>30</td>
<td>40</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### ACTIVE TO STANDBY

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST COND.</th>
<th>DESCRIPTION</th>
<th>COM -15</th>
<th>COM -25</th>
<th>MIN.</th>
<th>MAX.</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>tvdh</td>
<td>—</td>
<td>Valid Input before DPP High</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tgvdh</td>
<td>—</td>
<td>Valid OE before DPP High</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tcvdh</td>
<td>—</td>
<td>Valid Clock before DPP High</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tdhix</td>
<td>—</td>
<td>Input Don’t Care after DPP High</td>
<td>—</td>
<td>15</td>
<td>25 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tdhgx</td>
<td>—</td>
<td>OE Don’t Care after DPP High</td>
<td>—</td>
<td>15</td>
<td>25 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tdhcx</td>
<td>—</td>
<td>Clock Don’t Care after DPP High</td>
<td>—</td>
<td>15</td>
<td>25 ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### STANDBY TO ACTIVE

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST COND.</th>
<th>DESCRIPTION</th>
<th>COM -15</th>
<th>COM -25</th>
<th>MIN.</th>
<th>MAX.</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>txdl</td>
<td>—</td>
<td>Input Don’t Care before DPP Low</td>
<td>—</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tgxdl</td>
<td>—</td>
<td>OE Don’t Care before DPP Low</td>
<td>—</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tcxdl</td>
<td>—</td>
<td>Clock Don’t Care before DPP Low</td>
<td>—</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tdlv</td>
<td>—</td>
<td>DPP Low to Valid Input</td>
<td>20</td>
<td>25</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tdlgv</td>
<td>—</td>
<td>DPP Low to Valid OE</td>
<td>20</td>
<td>25</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tdlov</td>
<td>—</td>
<td>DPP Low to Valid Clock</td>
<td>30</td>
<td>35</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tdlov</td>
<td>A</td>
<td>DPP Low to Valid Output</td>
<td>5</td>
<td>45</td>
<td>45</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

1) Refer to Switching Test Conditions section.

### Dedicated Power-Down Pin Timing Waveforms

![DPP Timing Waveforms Diagram](image-url)
Specifications GAL20LV8ZD

Switching Waveforms

**COMBINATIONAL OUTPUT**

INPUT or I/O FEEDBACK

INPUT or I/O FEEDBACK

CONBINATIONAL OUTPUT

Combinatorial Output

**REGISTERED OUTPUT**

INPUT or I/O FEEDBACK

COMBINATIONAL OUTPUT

Input or I/O to Output Enable/Disable

OE

OE to Output Enable/Disable

**INPUT or I/O FEEDBACK**

VALID INPUT

VALID INPUT

**CLK**

**REGISTERED OUTPUT**

**1/f_{max}** (external fdbk)

**OE**

**REGISTERED FEEDBACK**

**1/f_{max}** (internal fdbk)

**f_{max} with Feedback**

Switching Waveforms

Discontinued Product (PCN #02-06). Contact Rochester Electronics for Availability.

www.latticesemi.com/sales/discontinueddevicessales.cfm
**Specifications GAL20LV8ZD**

### fmax Descriptions

- **fmax with External Feedback 1/(tsu+tco)**
  - **Note:** fmax with external feedback is calculated from measured tsu and tco.

- **fmax with Internal Feedback 1/(tsu+tcf)**
  - **Note:** tcf is a calculated value, derived by subtracting tsu from the period of fmax with internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to tcf + tpd.

### Switching Test Conditions

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>GND to 3.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise and Fall Times</td>
<td>2ns 10% – 90%</td>
</tr>
<tr>
<td>Input Timing Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Timing Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Load</td>
<td>See Figure</td>
</tr>
</tbody>
</table>

3-state levels are measured 0.5V from steady-state active level. 3-state to active transitions are measured at (Voh - 0.5) V and (Vol + 0.5) V.

<table>
<thead>
<tr>
<th>Output Load Conditions (see figure)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Test Condition</strong></td>
</tr>
<tr>
<td>A</td>
</tr>
<tr>
<td>B</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>C</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

*CL includes test fixture and probe capacitance.*
Electronic Signature

An electronic signature word is provided in every GAL20LV8ZD device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter checksum.

Security Cell

A security cell is provided in the GAL20LV8ZD devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The electronic signature data is always available to the user, regardless of the state of this security cell.

Device Programming

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Output Register Preload

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

The GAL20LV8ZD devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

Input Buffers

GAL20LV8ZD devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

Dedicated Power-Down Pin

The GAL20LV8ZD uses pin 5 as the dedicated power-down signal to put the device in the power-down state. DPP is an active high signal where a logic high driven on this signal puts the device into power-down state. Input pin 5 cannot be used as a logic function input on this device.

Discontinued Product (PCN #02-06). Contact Rochester Electronics for Availability.
Circuitry within the GAL20LV8ZD provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (\(t_{pr}\), 10\(\mu\)s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the GAL20LV8ZD. First, the VCC rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of \(t_{pr}\) time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

**Input/Output Equivalent Schematic**

![Typical Input and Output Diagrams](image-url)
Specifications GAL20LV8ZD

Typical AC and DC Characteristics

Normalized Tpd vs Vcc

Normalized Tco vs Vcc

Normalized Tsu vs Vcc

Normalized Tpd vs Temp

Normalized Tco vs Temp

Normalized Tsu vs Temp

Delta Tpd vs # of Outputs Switching

Delta Tco vs # of Outputs Switching

Delta Tpd vs Output Loading

Delta Tco vs Output Loading

Discontinued Product (PCN #02-06). Contact Rochester Electronics for Availability.

www.latticesemi.com/sales/discontinueddevicessales.cfm
Specifications GAL20LV8ZD

Typical AC and DC Characteristics

Vol vs Iol

Voh vs Ioh

V vs Iol

Voh vs Ioh

Normalized Icc vs Vcc

Normalized Icc vs Temp

Normalized Icc vs Freq.

Delta Icc vs Vin (1 input)

Input Clamp (Vik)

Typical AC and DC Characteristics

Discontinued Product (PCN #02-06). Contact Rochester Electronics for Availability.

www.latticesemi.com/sales/discontinueddevicessales.cfm