Lattice Nexus 2 Platform — Overview

Advance Data Sheet

FPGA-DS-02122-0.71

December 2024

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
DDR	Double Data Rate
DDRPHY	DDR Physical Layer
DLLDEL	DLL Delay
DSP	Digital Signal Processing
EBR	Embedded Block RAM
ECC	Error Correction Coding
ECLK	Edge Clock
FIFO	First In First Out
GCLK	Global Clock
LPDDR	Low Power DDR
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor Interface Signaling
LVDS	Low-Voltage Differential Signaling
LUT	Look Up Table
MPPCS	Multi-Protocol PCS
MPPHY	Multi-Protocol PHY
PCIe	Peripheral Component Interconnect Express
PCS	Physical Coding Sublayer
PCLK	Primary Clock
PDP	Pseudo Dual Port
PFU	Programmable Functional Unit
PIC	Programmable I/O Cells
PIO	Programmable I/O
PLL	Phase Locked Loops
RCLK	Regional Clock
SEU	Single Event Upset
SLC	System Logic Cell
SLVS	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface
SP	Single Port
SRAM	Static Random-Access Memory

1. General Description

Lattice Nexus™ 2 is a low-power small FPGA platform optimized for a wide range of applications across multiple markets – optimized for edge computing workloads requiring large memories and DSP resources and delivering a variety of high bandwidth interfaces ideal for video processing, communications, and machine learning inferencing. A platform is built upon a programmable FPGA fabric optimized for a specific range of logic densities coupled with a collection of features that are assembled into unique device families utilizing varying amounts of features and I/O. The Lattice Nexus 2 platform enables logic capacities up to 220k System Logic Cells and capable of delivering up to 16Gb multi-protocol SERDES, hardened PCIe Gen 4, DDR4/LPDDR4, and DDR3L memory interfaces, advanced security, and small packages.

The Lattice Nexus 2 platform delivers best-in-class power efficiency while meeting performance requirements for a wide range of applications. The following families are available in the Lattice Nexus 2 Platform.

Lattice Certus™-N2 family is a general-purpose FPGA. Optimized for edge compute workloads and featuring fast and flexible I/O (with support for 3.3 V I/O), it features 16G SERDES supporting multiple popular protocols including 10G Ethernet and PCIe Gen 4.

Lattice Nexus 2 platform-based devices are supported by the Lattice Radiant™ integrated design software environment. Synthesis library support for Lattice Nexus 2 devices is available for popular logic synthesis tools. Radiant uses synthesis tool output along with constraints from its floor planning tools to place and route the user design in Lattice Nexus 2 devices. The tool extracts timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for Lattice Nexus 2 families. By using these configurable soft IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing productivity.

1.1. Features

Table 1.1 shows the key features of the Lattice Nexus 2 platform.

Table 1.1. Lattice Nexus 2 Platform Key Features

Programmable Architecture	**System Performance**
• 65k to 220k system logic cells • 120 to 520 multipliers (18 × 18) in sysDSP™ blocks • 4 to 12 Mb of embedded memory (EBR)	• Improved low power performance • Timing closure for a typical design of up to 350 MHz • EBR/DSP/Clocks up to 625 MHz
External Memory Interface Support	**SERDES and Hardened Interface**
• DDR4/LPDDR4 up to 2400 Mbps data rate • DDR3L up to 1866 Mbps data rate • Hardened DFI (DDR PHY Interface) training layer	• 16G SERDES and hardened PCIe Gen 1/2/3/4 • 2-8 SERDES • Up to 4.5 Gbps per lane hardened MIPI D-PHY • Up to 3.5 Gsps or 7.98 Gbps per trio hardened MIPI C-PHY
Device Security	**High-speed and Flexible Programmable I/O**
• AES-256-GCM encryption • Up to ECDSA-521 and RSA4096 authentication • Anti-tamper and PUF/Unique ID • User data encryption • Side channel resistance • TRNG (True Random Number Generator)	Up to 349 programmable sysI/O – High Performance (HP) and Wide Range (WR) • 1.8 Gbps Soft MIPI D-PHY • 1.6 Gbps LVDS • 3.3 V support

Table 1.2. Lattice Nexus 2 Families

Name		Certus-N2 LN2-CT
Features		
Fabric	**LCs, DSP, EBR**	Yes
Protocol	**Max Speed**	16G[1]
	PCIe Gen 1/2/3/4	2.5G, 5G, 8G, 16G
	Ethernet to 10G	Yes
	Multi-protocol SERDES	Yes
Memory	**DDR3L**	Yes
	LPDDR4/DDR4	Yes
Security	**Bitstream Security**	Yes
	User Mode Security	No
Other	**Soft Error Detection/Soft Error Correction**	Yes
	JTAG, x1/x2/x4 SPI Config	Yes
	xSPI Config	Yes
	Internal Flash Memory	No

Note:

1. Protocol Performance speeds met with LFG and CBG Packages. Other packages are limited to 10G.

Table 1.3. Certus-N2 Family Selection Guide

Device	CT06	CT10	CT16	CT20
System Logic Cells (k)	65	100	160	220
LUTs (k)	40	61	98	135
Embedded Memory (EBR) Blocks (36 kb)	114	153	228	306
Embedded Memory (Mb)	4	5.5	8	12
Distributed RAM Bits (kb)	416	636	1041	1272
DSP (18 × 18 Multipliers)	120	240	360	520
High Frequency Oscillator	1	1	1	1
GPLL	4	4	7	7
Packages (Type, Size, Ball Pitch)[1]	**Total I/O (WR – Wide Range, HP – High Performance) SERDES**			
ASG187 (FOWLP, 6 × 9.5 mm, 0.5 mm)[2]	87 (27,60)	87 (27,60)	—	—
ASG273 (FOWLP, 9 × 9 mm, 0.5 mm)[2]	112 (27, 85) 4	112 (27, 85) 4	—	—
ASG410 (FOWLP, 11 × 9 mm, 0.5 mm)[2]	—	—	247 (94,153)[3]	247 (94,153)[3]
			196 (43, 153) 4	196 (43, 153) 4
CBG256 (FCCSP, 14 × 14 mm, 0.8 mm)	153 (51, 102) 2	153 (51, 102) 2	—	—
CBG484 (FCCSP, 18 × 18 mm, 0.8 mm)	196 (94,102) 4	196 (94,102) 4	247(94,153) 4	247(94,153) 4
LFG672 (FCBGA, 27 × 27 mm, 1.0 mm)	—	—	349 (94,255) 8	349 (94,255) 8

Notes:

1. Refer to Ordering Information for more package details.
2. Protocol Performance speeds met with LFG and CBG Packages. Other packages are limited to 10G.
3. Package option available in CT20E and CT16E only.

2. Architecture

2.1. Overview

Each Lattice Nexus 2 device contains arrays of logic blocks, arranged into Clock Regions (CKR). Each CKR comprises blocks such as PFUs, EBRs, DSPs, and a Clock Network that clocks synchronous elements in the CKR. Each CKR is associated with an I/O bank. An I/O bank may be a group of high-speed SERDES I/O blocks, a High-Performance I/O (HPIO) bank or a Wide-Range I/O (WRIO) bank. The Clock Regions are arranged in two rows and multiple columns depending on the density of the device and vary in size from 11k up to 22k system logic cells.

The top and bottom periphery of the device contain Programmable I/O Cells (PIC) and SERDES I/O blocks. Interspersed within the arrays are sysMEM Embedded Block RAM (EBR) blocks and sysDSP Digital Signal Processing blocks.

In addition, Lattice Nexus 2 devices provide various system level hard IP functional and interface blocks such as PCIe, Multiple Protocol PCS, and Security blocks. The PCIe hard IP supports PCIe Generation 4.0. The Lattice Nexus 2 platform also provide security and tamper detection features to help protect user designs, and cryptographic functions to help secure user data. Lattice Nexus 2 devices deliver more robust reliability by offering enhanced frame based Soft Error Detection/ Soft Error Correction (SED/SEC) functions.

The sysMEM EBR blocks are large, dedicated 36 kb fast memory blocks with built-in ECC and FIFO support. Each sysMEM block can be configured to a single, pseudo dual or true dual port memory in a variety of depths and widths as RAM or ROM. The DSP block supports a variety of multiplier and adder configurations, up to 54 × 54 MULT and 48-bit accumulator, which are the building blocks for complex signal processing capabilities.

The Lattice Nexus 2 device's sysI/O buffers contain two types of I/O blocks, Wide-Range and High-Performance I/O (WRIO and HPIO). The sysI/O buffers of the Lattice Nexus 2 devices are arranged in up to 15 banks allowing the implementation of a wide variety of I/O standards. The WRIO are in the top banks, providing flexible ranges of general purpose I/O configurations up to 3.3 V VCCIO. The banks located on the bottom side of the device are dedicated to High Performance (HP) interfaces such as LVDS, MIPI, DDR4/LPDDR4, and DDR3L supporting up to 1.8 V VCCIOs.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM, and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Lattice Nexus 2 delivers a much higher FPGA LC capacity and performance than previous Lattice product families and is optimized for increased routability and utilization performance. The Lattice Nexus 2 fabric is based on LUT4s, which minimize power consumption due to its area efficiency. The registers in the PFU and sysI/O blocks in Lattice Nexus 2 devices can be configured to be SET or RESET, allowing the device to power up in a known state for predictable system function.

Other blocks provided include PLLs, DLLs, and configuration functions. There is one PLL per HPIO bank and one PLL per WRIO bank group throughout the device. Lattice Nexus 2 devices also include Lattice Memory Mapped Interface (LMMI) which is a Lattice standard to support simple read and write dynamic control register operations for select internal IP.

Every device in the family has a JTAG port. This family also provides a High Frequency on-chip oscillator, and soft error detect capability. The Lattice Nexus 2 devices use 0.82 V as their core voltage.

Figure 2.1 to Figure 2.4 show the high-level device floorplan of LN2-CT20, LN2-CT16, LN2-CT10, and LN2-CT06 respectively.

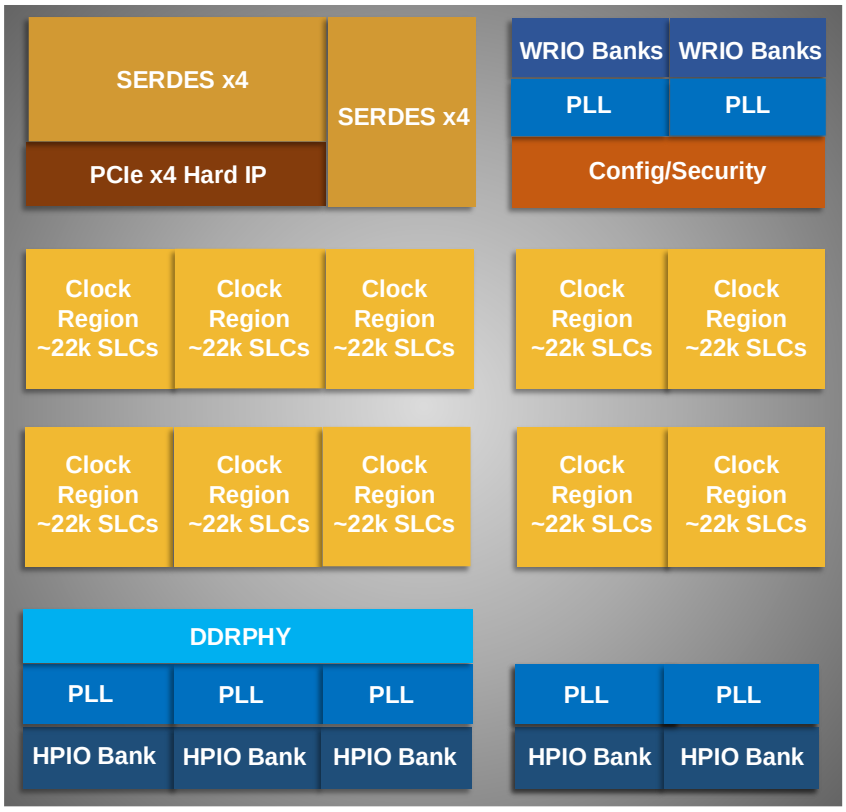


Figure 2.1. High-level Device Floorplan (LN2-CT20 Device)

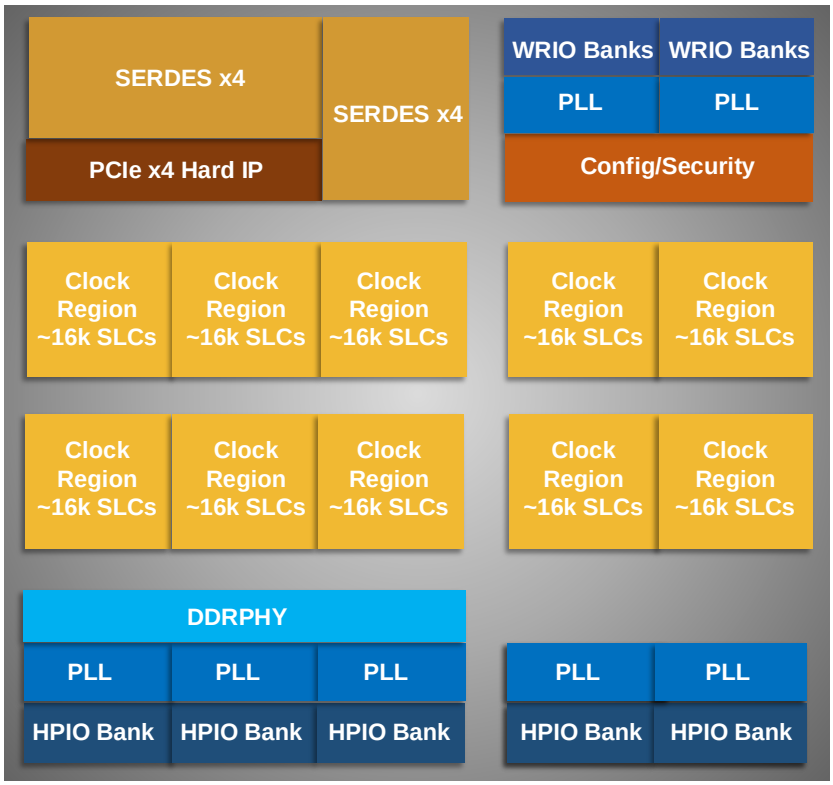


Figure 2.2. High-level Device Floorplan (LN2-CT16 Device)

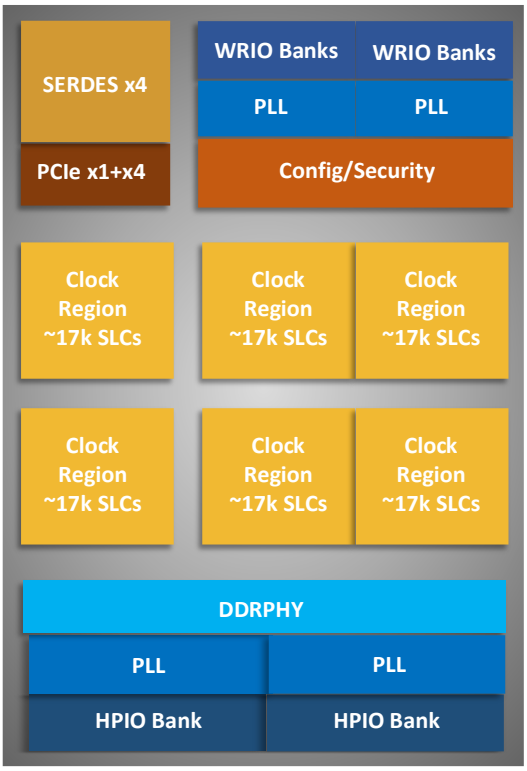


Figure 2.3. High-level Device Floorplan (LN2-CT10 Device)

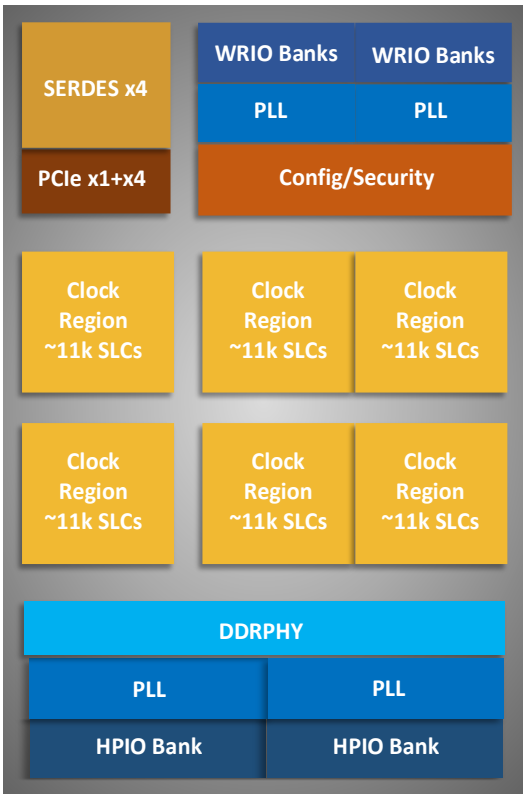


Figure 2.4. High-level Device Floorplan (LN2-CT06 Device)

2.2. Programmable Functional Unit (PFU) Blocks

Lattice Nexus 2 platform delivers a higher FPGA Logic Count capability and performance compared to previous Lattice product families. It is optimized for Best-in-Class routability and utilization performance. The core of the Lattice Nexus 2 device consist of Programmable Functional Unit (PFU) blocks and each block can be used to perform Logical, Arithmetic, RAM, or ROM functions. The PFU blocks are made up of LUTs and registers. The Lattice Nexus 2 fabric leverages its LUT4 area efficiency to generate its low power differentiation.

Each Lattice Nexus 2 PFU block includes the following resources:

- 12 LUT4+FF pairs (arranged as six slices, two LUT+FF per slice)
- Fast LUT4 input to output delay path
- Dedicated MUX to enable LUT5 support
- S44 Fast LUT-to-LUT connection
- Single port and pseudo dual port distributed RAM support
- Single Port Distributed RAM: 16 × 4, 16 × 8, 32 × 2, 32 × 4
- Pseudo Dual Port Distribute RAM: 16 × 4, 16 × 8, 32 × 2, 32 × 4
- Two 16 x 4 Distributed RAMs can fit into one PFU to get 16 x 8
- Two 32 x 2 Distributed RAMs can fit into one PFU to get 32 x 4

2.2.1. Slices

Each PFU contains six slices, and each slice contains two LUT4s and two FFs. All slices have 16 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six from routing and one to carry-chain (to the adjacent PFU).

2.2.2. Modes of Operation

Slices 0-5 of the PFU have up to four potential modes of operation: Logic, Ripple, RAM, and ROM.

Logic Mode

The LUTs in each slice are configured as 4-input combinatorial lookup tables in logic mode. A LUT4 can have 16 possible input combinations. Any 4-input logic functions can be generated by programming this lookup table. A LUT5 can be constructed within one slice.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. Ripple mode also includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2C mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In RAM mode, two sets of 16 × 4-bits or 32 x 2-bits of distributed single port RAM or pseudo dual port RAM can be constructed within one PFU. Slices 0, 1, and 2 make up one distributed RAM block and Slices 3, 4 and 5 make up the 2nd distributed RAM block. The RAM data is stored in Slices 0 and 1 of the first block and Slices 3 and 4 of the second block. Slice 2 is used to provide memory address and control signals for the first block while Slice 5 is for the 2nd block. Lattice Nexus 2 device also supports distributed memory initialization.

The Lattice design tools support the creation of a variety of different sized memories. Where appropriate, the software constructs these using distributed memory primitives that represent the capabilities of the PFU. Table 2.1 lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in Lattice Nexus 2 devices, refer to *Lattice Nexus 2 Embedded Memory User Guide (FPGA-TN-02366)*.

Table 2.1. Number of Slices Required to Implement Distributed RAM

	SP 16 × 4	SP 32 × 2	PDP 16 × 4	PDP 32 × 4
Number of slices	3	3	3	3

Note: SP = Single Port, PDP = Pseudo Dual Port

ROM Mode

ROM mode uses the LUT logic; hence, Slice 0 through 5 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to *Lattice Nexus 2 Embedded Memory User Guide (FPGA-TN-02366)*.

2.3. Routing

There are many resources provided in the Lattice Nexus 2 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers, and metal interconnect (routing) segments.

The Lattice Nexus 2 platform has an enhanced routing architecture that produces a compact design. The Radiant software tool takes the output of the synthesis tool and places and routes the design.

2.4. Clocking Structure

The Lattice Nexus 2 device core architecture is constructed of several similar sized Clock Regions (CKR). Each CKR comprises blocks such as PFUs, EBRs, DSPs, and a Regional Clock Network. For the LN2-CT20 device, each CKR is about 22k System Logic Cells (SLCs). Each CKR is also associated with an I/O bank. An I/O bank may be a group of high speed SERDES I/O, a High-Performance I/O (HPIO) bank or a Wide-Range I/O (WRIO) bank. The Clock Regions are arranged in two rows and multiple columns depending on the density of the device.

The Lattice Nexus 2 clocking structure consists of clock synthesis blocks (PLLs), clock tree networks (GCLK, ECLK, RCLK, and PHYCLK), on-chip oscillators, and clock modules: Clock Synchronizers and Dividers (ECLKSYNCA/ECLKDIVA), Dynamic Clock Selection (DCS), Dynamic Clock Control (DCC), and DLLDEL delay elements. Each of these functions is described as follows.

An overview of the Clocking Network is shown in Figure 2.5 for the Lattice Nexus 2 device.

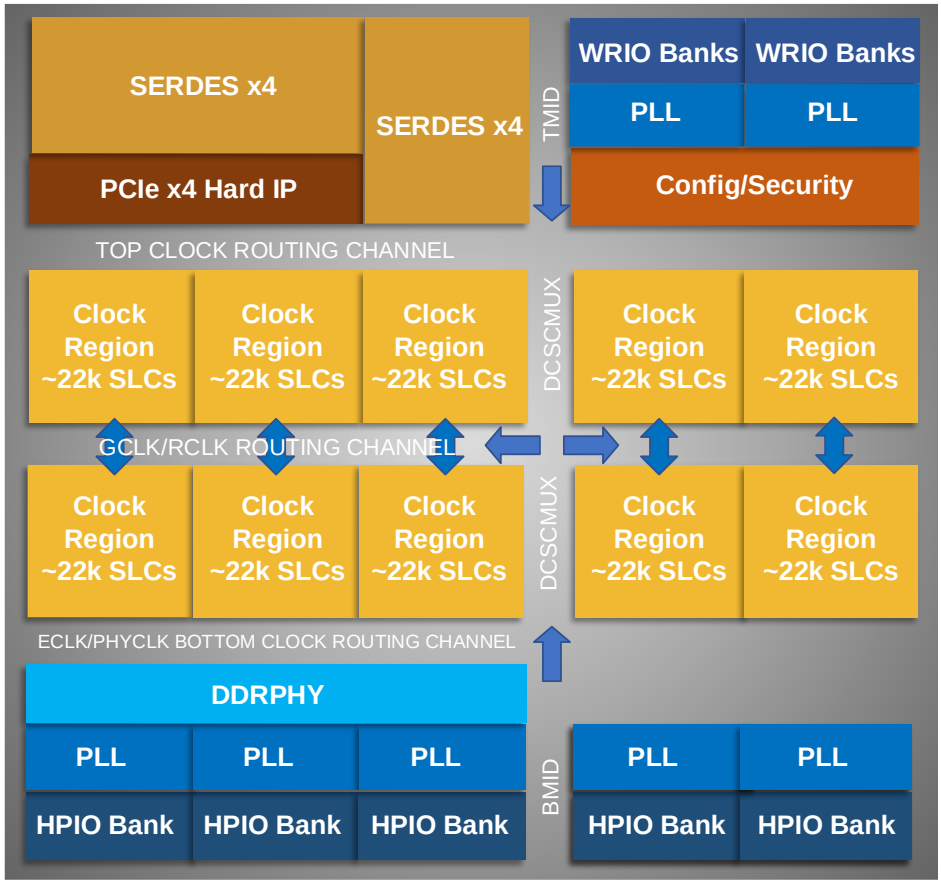


Figure 2.5. High-Level View of Clock Networks and Elements (LN2-CT20 Device)

2.4.1. On-Chip Oscillator

The Lattice Nexus 2 device offers on board oscillator, which provides various clocks for the FPGA clock tree, Configuration block, and the system monitoring/ATM (anti-tampering) block. First, the OSC generates the user clock that drives the FPGA clock tree; this user clock is dynamically selectable between 400 MHz or 320 MHz, with 1-256 programmable divider options. Secondly, the OSC generates separate clocks for Configuration block with different frequencies of 400 and 320 MHz to support SPI interface. Lastly, the OSC generates a hardened 100 MHz clock for system monitoring/ATM block.

2.4.2. PLL

The Lattice Nexus 2 PLL IP can be used for a variety of clock management applications such as frequency synthesis (multiplication and division of a clock), clock injection delay removal, clock phase adjustment and clock timing adjustment. The Lattice Nexus 2 PLL supports frequency synthesis by enabling the input reference clock to be multiplied up or divided down. The reference clock and feedback clock can come from various sources. The PLL (WRIO) supports six output clock selections, with each output clock having a different frequency. Each clock output can then be dynamically enabled or disabled by the user. The PLL (HPIO) supports seven output clock selections, six of which are similar to the PLL (WRIO) and an additional high-speed PHYCLK output for high-speed I/O interfaces. The Lattice Nexus 2 PLL also supports the clock injection delay removal feature where delays associated with the PLL, and clock tree are removed. This feature is typically used to reduce clock path delays and is performed by aligning the PLL input clock with a feedback clock from the clock tree. The Lattice Nexus 2 PLL further supports a clock phase adjustment feature. This feature provides the ability to set a specific phase offset between the outputs of the PLL. Each clock output can support an independent phase shift value.

The PLL IP supports the following key features:

- Frequency clock synthesis
- Clock tree delay cancellation
- Multiple reference and feedback clock selections
- Multiple and independent output clock controls
- Reference clock divider values – 1 to 64
- Integer Feedback divider values – 2 to 4095
- Output divider values – 1 to 256
- Supports Fractional-N divider
- Supports Spread Spectrum Clock Generation
  - Spreading rate adjustment range 15 kHz – 4 MHz
  - Spreading depth 0% to -10%
- VCO phase shift – 8 VCO phases
- Post Divider phase shift
- Dynamic VCO and divider phase shift
- Output clock bypass
- Programmable bandwidth
- Output synchronization to one main clock output (CLKOP)
- Dynamic programmability of PLL registers through the LMMI interface
- Dynamic reset GPLL operation
- Glitchless Dynamic output phase selections, controlled through fabric ports
- CLKOPHY with output up to 2400 MHz

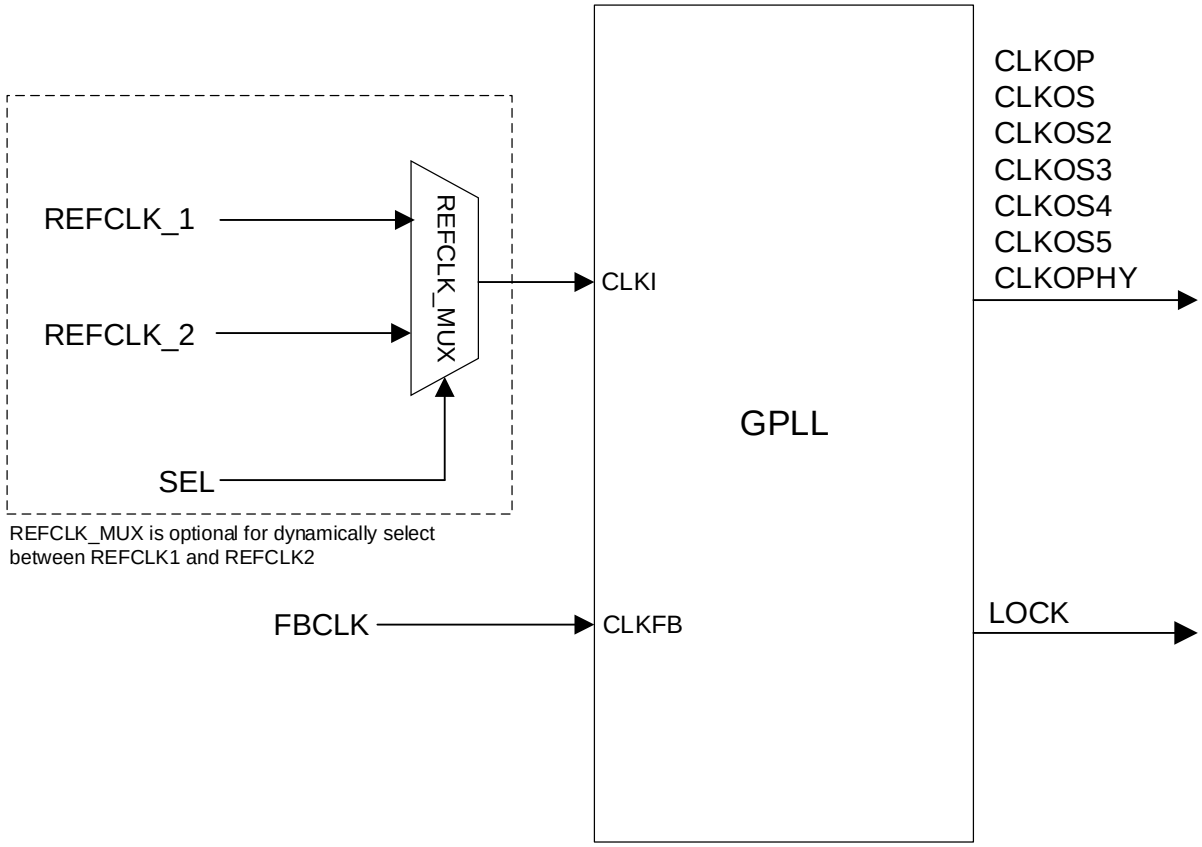


Figure 2.6. Lattice Nexus 2 PLL Block Diagram

For more details on the PLL, refer to the Lattice Nexus 2 sysCLOCK PLL Design and User Guide (FPGA-TN-02364).

2.4.3. Global Clock (GCLK)

The Global Clock Network (GCLK) provides the main clock sources in the Lattice Nexus 2 devices. The GCLK network drives the Regional Clock Networks (RCLK) of all Clock Regions (CKRs) in the device. The GCLK structure has two clock domains for all device densities, left half and right half. Each domain takes all available Global Clock sources and generates 24 independent GCLKs. These 24 GCLKs, combined with other Regional Clock sources provide 16 clocks to drive each row within a Clock Region.

Lattice Nexus 2 supports glitchless Dynamic Clock Control (DCC) feature which enables the GCLKs to be enabled or disabled to save dynamic power. There are also Dynamic Clock Selection (DCS) logic to allow glitchless selection between two clocks for the GCLK network.

2.4.4. Regional Clocks (RCLK)

The Regional Clock Network (RCLK) is the main clock network within a Clock Region. It is driven by the Global Clock Network and provides clock sources to all blocks (PFU, EBR, and DSP) within a Clock Region.

The RCLK network can bridge to adjacent Clock Regions to form Multi-Region Clock Networks. Specifically, it can bridge to one other Clock Region either to the left, right, top or bottom of the current Clock Region. The multi-region clock can be formed in the following topology: 1 × 1, 1 × 2, 2 × 1, 2 × 2, or 3 × 2 (column × row).

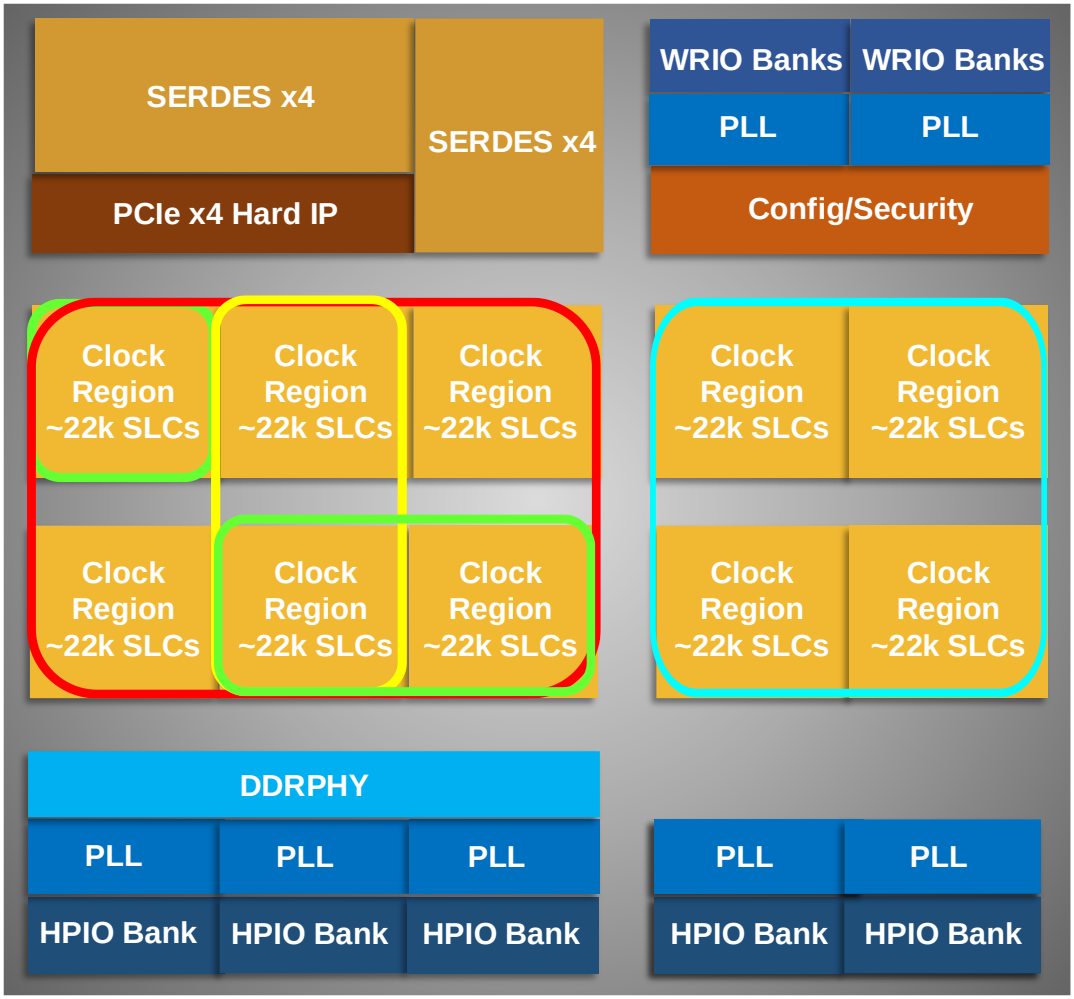


Figure 2.7. Multi-Region Clock Formation (LN2-CT20 Device)

The RCLKs are sourced from multiple inputs, referred to as Regional Clock sources. The Regional Clock sources that can drive the RCLKs are:

- Dedicated Clock Pins (PCLKT pins)
- GCLKs
- SERDES Clocks
- PLL (HPIO) outputs (CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, CLKOS5)
- PLL (WRIO) outputs (CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, CLKOS5)
- Clocks from neighboring regions, which is Regional Bridge clocks (RSBRG_* [0:3])
- Internally generated clocks (Fabric_CLK)

2.4.5. Edge Clock (ECLK)

Lattice Nexus 2 FPGAs have a number of high-speed Edge Clocks that are intended for use with the PIO in the implementation of high-speed DDR I/O interfaces. These clocks, which have low injection time and skew, are suitable to drive the high-speed I/O interfaces with high fan-out capability, such as DDR Memory or Generic DDR interfaces. The Lattice Nexus 2 device has Edge Clocks (ECLK) at the bottom of the device where the HPIO banks are located. Each HPIO bank has four Edge Clocks supporting each Clock Region (CKR). The ECLK network is also able to bridge to adjacent left or right Clock Regions to form a wider ECLK network.

Each Edge Clock can be sourced from the following:

- Dedicated Clock Pins (PCLKT pins)
- DLLDEL outputs
- PLL (HPIO) outputs (CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, CLKOS5)
- ECLK Bridge clocks (EBRG_*[0:3])
- Internally generated clocks (Fabric_CLK)

For detailed information on Edge Clock connections, refer to Lattice Nexus 2 sysCLOCK PLL Design and User Guide (FPGA-TN-02364).

2.4.6. PHYCLK

The PHYCLK network is a special high frequency clock network that is used to support high frequency clocks for interface protocols for Fmax up to 2.4 GHz. The PHYCLK is driven only by a special output of the PLL (HPIO) and there is one PHYCLK per I/O bank. The PHYCLK drives the High-Speed I/O interfaces and the DDRPHY hard IP at the same time. The DDRPHY hard IP spans three HPIO sectors and the full rate PHYCLK drives the DDRPHY full-rate clock port located at the center HPIO sector. The PHYCLK also drives ECLKDIV module to provide a quad-rate clock, divided by 4, frequency clock.

2.4.7. Clock Synchronizers and Dividers

Edge Clock Synchronizer (ECLKSYNCA) and Divider (ECLKDIVA) provide clock synchronization and clock divider functions in Lattice Nexus 2 devices.

For further information, refer to Lattice Nexus 2 sysCLOCK PLL Design and User Guide (FPGA-TN-02364).

2.4.8. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the global clock network. It switches between two independent input clock sources. Depending on the operational mode, it switches between two (2) independent input clock sources either with or without any glitches. This is achieved regardless of when the select signal is toggled. Both input clocks must be running to achieve a functioning glitchless DCS output clock, but running clocks are not required when used as a non-glitchless normal clock multiplexer.

There are four dynamic clock select blocks in the Lattice Nexus 2 devices. The DCS block allows dynamic and glitchless selection between two GCLK clock sources. The output of the DCS drives the GCLKs.

For more information about the DCS, refer to Lattice Nexus 2 sysCLOCK PLL Design and User Guide (FPGA-TN-02364).

2.4.9. Dynamic Clock Control

The Lattice Nexus 2 device has a power-saving feature known as Dynamic Clock Control. This feature allows internal logic to dynamically enable or disable the GCLKs, thus enabling overall dynamic power consumption of the device. This gating function does not create glitches or increase the clock latency to the Global Clock network. There is a DCC element associated with each 48 GCLKs.

For more information about the DCC, refer to Lattice Nexus 2 sysCLOCK PLL Design and User Guide (FPGA-TN-02364).

2.4.10. DLL Delay (DLLDEL)

DLLDEL is a passive delay component to provide necessary clock phase shift for the dedicated clock pins before driving the GCLK and ECLK network. The adjusted phase can be dynamic or static controlled. In dynamic control mode, the delay code comes from the associated DDRDLL available on the device. In static control mode, the delay control is set by software. The delay element inside the DLLDEL can be bypassed if it is not used.

There are four DLLDEL elements for each HPIO bank. Each associate with one ECLK. There is only one DLLDEL code common to all DLLDEL modules, provided by one DDRDLL within each HPIO section.

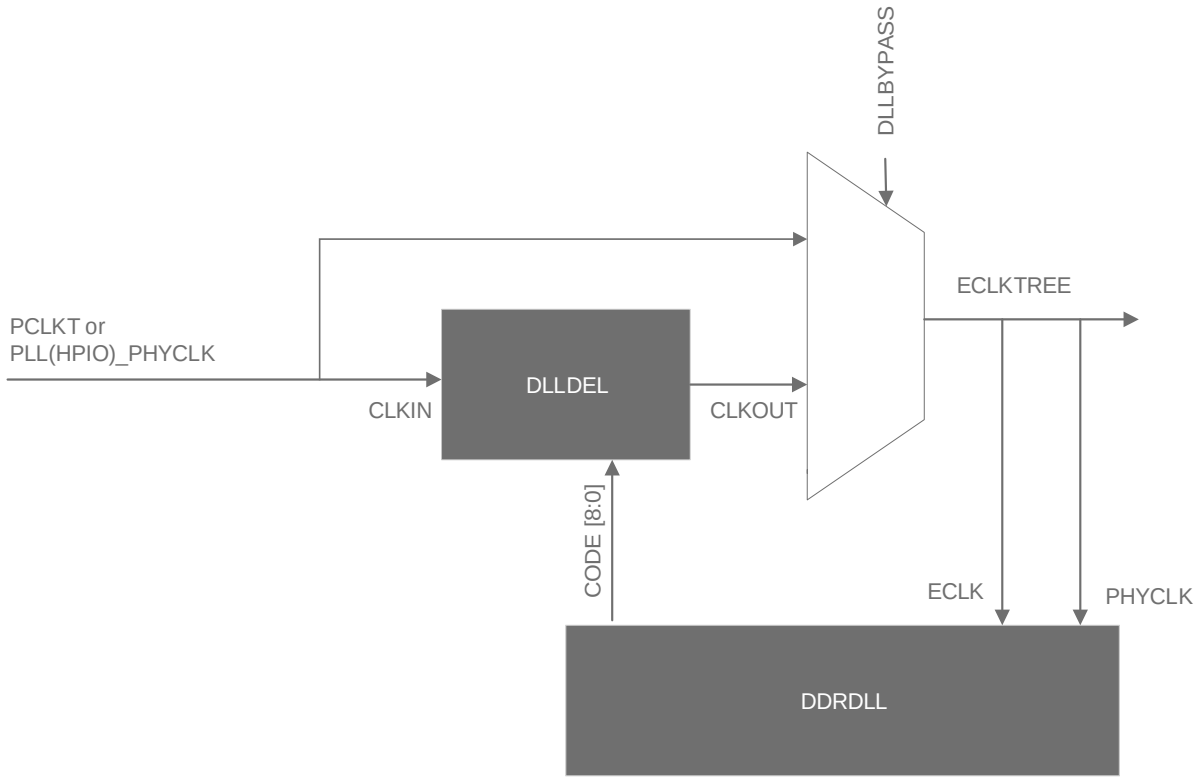


Figure 2.8. High-Level Implementation of DLLDEL and Code Control

2.5. sysMEM Embedded Memory

The Lattice Nexus 2 devices contain 114 to 306 sysMEM Embedded Block RAM (EBR) blocks, depending on the device density. The EBR consists of a 36 kb RAM with memory core, dedicated input registers and output registers as well as optional pipeline registers at the outputs. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM, and built-in FIFO. In Lattice Nexus 2 devices, unused EBR blocks are powered down to minimize power consumption.

2.5.1. sysMEM Embedded Memory Block

The sysMEM Embedded Memory block can implement single port, dual port, or pseudo dual port memories. Each block can be used in a variety of depths and widths as listed in Table 2.2. FIFOs can be implemented using the built-in read and write address counters and programmable full, almost full, empty, and almost empty flags. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with up to 72-bit data widths. For more information, refer to Lattice Nexus 2 Embedded Memory User Guide (FPGA-TN-02366).

EBR also provides a built in ECC engine. The ECC engine supports a write data width of 64 bits, and it can be cascaded for larger data widths such as x128, ECC read may be performed in x1, x2, x4, x8, x16, x32, or x64 modes. The ECC parity generator creates and stores parity data for each 64-bit word written. When a read operation is performed, it compares the data with its associated parity data and reports back if any Single Event Upset (SEU) event has disturbed the data. Any single bit data disturbance is automatically corrected at the data output. In addition, two dedicated error flags indicate if a single-bit or two-bit error has occurred.

Table 2.2 sysMEM Embedded Memory Block Configurations

Single Port	Pseudo Dual Port	True Dual Port
32,768 × 1	32,768 × 1	32,768 × 1
16,384 × 2	16,384 × 2	16,384 × 2
8,192 × 4	8,192 × 4	8,192 × 4
4,096 × 9	4,096 × 9	4,096 × 9
2,048 × 18	2,048 × 18	2,048 × 18
1,024 × 36	1,024 × 36	1,024 × 36

2.5.2. Bus Size Matching

All the multi-port memory modes support different widths on each of the ports (except ECC mode, which only supports a write data width of 64 bits). The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.5.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM Embedded Memory block can also be utilized as a ROM.

2.5.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Embedded Memory Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

2.5.5. Single, Dual, and Pseudo-Dual Port Modes

In all the sysMEM Embedded Memory modes, the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

2.5.6. FIFO Modes

Lattice Nexus 2 platform devices support two different types of FIFOs with sysMEM Embedded Memory: Single Clock FIFO (FIFO) and Dual Clock FIFO (FIFO_DC). FIFO Controller Implementation has options as LUT-Based, or hardware-based. It also supports the First Word Fall Through mode.

2.5.7. Memory Output Reset

The EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.9. The optional Pipeline Registers at the outputs of both ports are also reset in the same way.

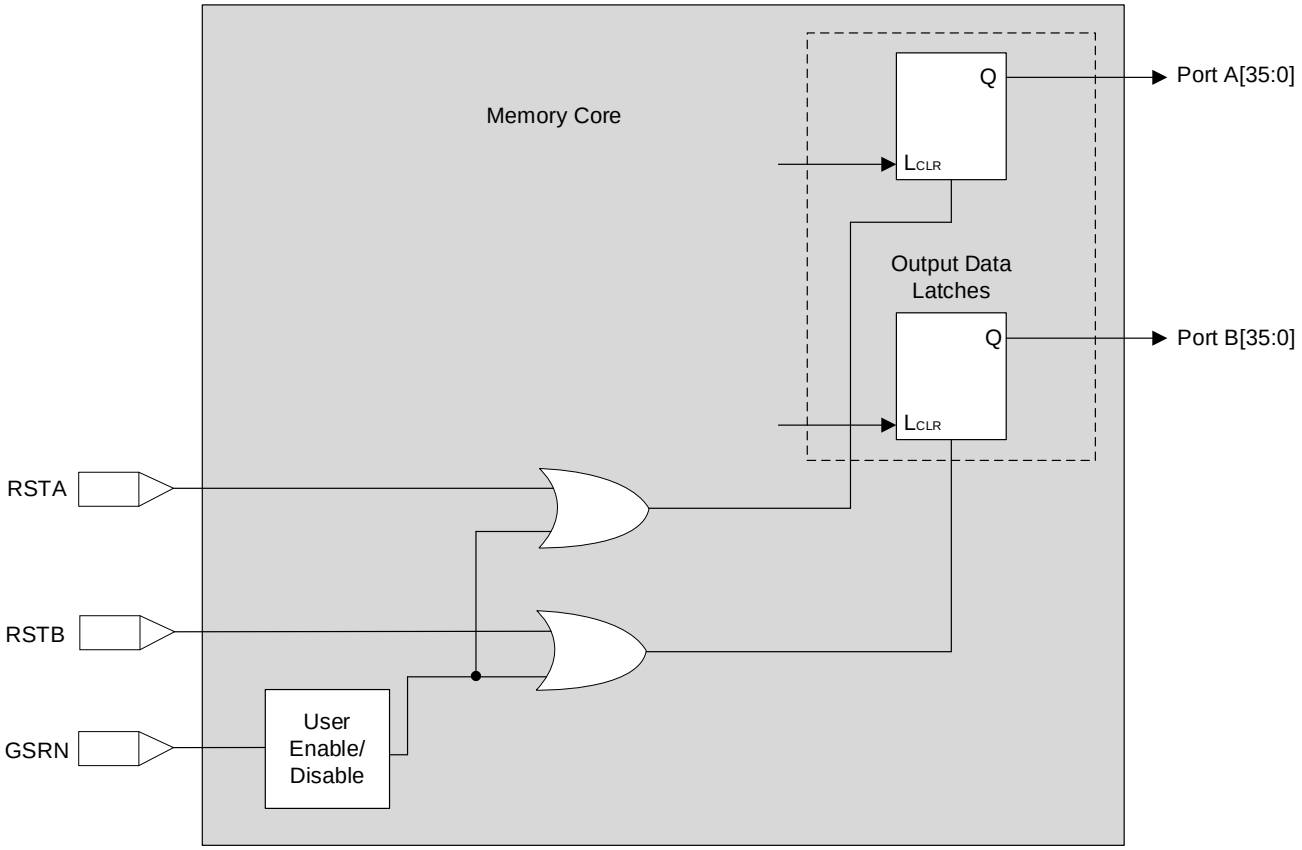


Figure 2.9. Memory Core Reset

For further information on the sysMEM Embedded Memory block, see the list of technical documentation in References section.

2.6. sysDSP

The Lattice Nexus 2 platform provides an enhanced sysDSP architecture, making it ideally suitable for low-cost, high-performance Digital Signal Processing (DSP) applications. The internal DSP can also run up to 625 MHz maximum frequency on fully pipelined configuration.

The Lattice Nexus 2 DSP block is a single-clock domain block with simpler structures to enable streamlined RTL implementation. Figure 2.10 shows the simplified DSP functional block, which can be configured to implement four 8 × 8 multipliers, three 9 × 9 multipliers, four 9 × 9 dot products, or one 18 × 18 multiplier. Each DSP block also contains an 18-bit pre-adder to support the symmetric filter and complex number multiplication, as well as a 48-bit adder with saturation and rounding options.

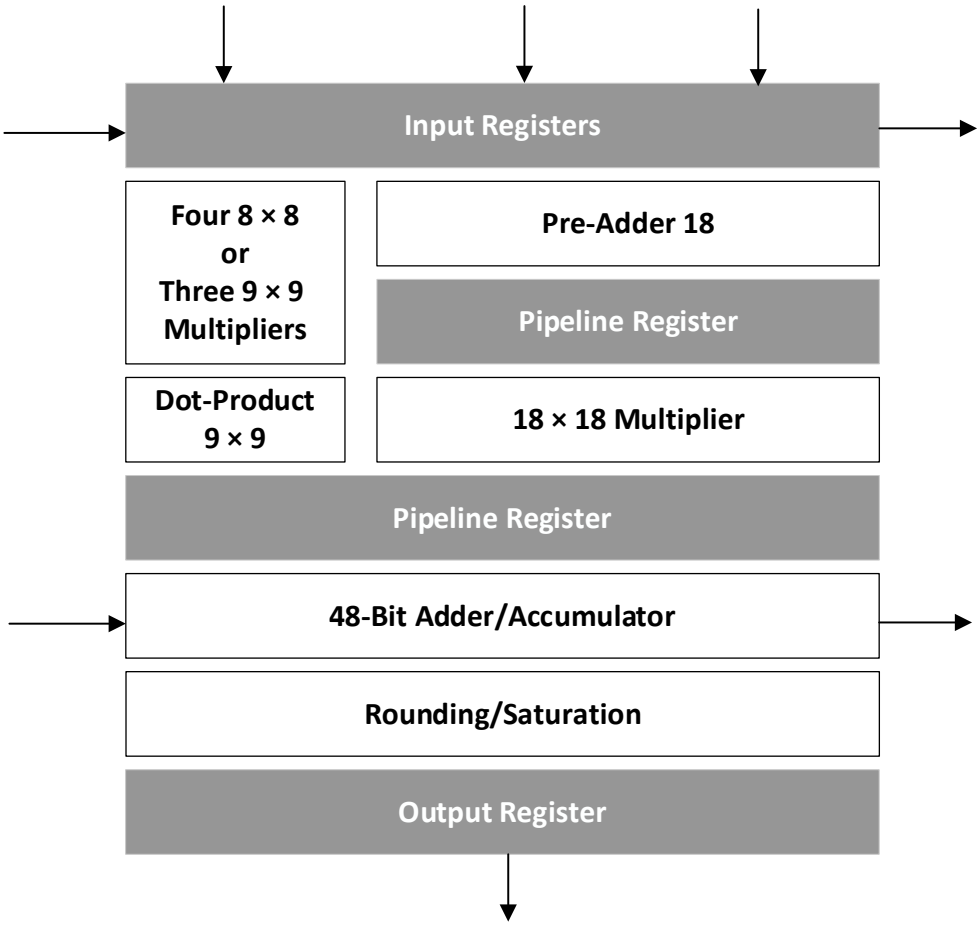


Figure 2.10. DSP Functional Block

The Lattice Nexus 2 sysDSP block supports the following basic elements.

- MULT8x8 (8-bit multiplication)
- MULT9x9A (9-bit multiplication)
- MULT18x18A (18-bit multiplication)
- MULTADDSUB18x18A (18-bit multiplication with pre-adder and accumulator)
- DOTPRODADDSUB9x9/DOTPRODADDSUB9x9A (9x9 multiplication and addition with accumulator)

For further information, refer to Lattice Nexus 2 sysDSP User Guide (FPGA-TN-02362).

2.7. Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysI/O buffers and pads. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement a wide variety of standards that are found in today's systems including LVDS, HSUL, SSTL, POD, LVSTL, SLVS, SUBLVDS, LVCMOS, and MIPI.

The Lattice Nexus 2 platform contains multiple Programmable I/O Cell (PIC) blocks. Each PIC contains two Programmable I/O, PIOA and PIOB. Each PIO includes a sysI/O buffer and I/O logic. Two adjacent PIO can be joined to provide a differential I/O pair referred to as True and Comp, where True Pad is associated with the positive side of the differential I/O, and the complement with the negative.

Lattice Nexus 2 devices offer two types of I/O banks. The top bank I/O are WRIO (Wide Range I/O), and the bottom bank I/O are HPIO (High Performance I/O), with following feature summary:

WRIO (Wide Range I/O) operating with a VCCIO of 3.3 V down to 1.2 V:

- LVCMOS33/25/18/12
- Programmable Drive Strengths (4 to 12 mA)
- Programmable Slew rate: Fast and Slow
- Bus Keeper, Weak Pull-up and Weak Pulldown
- Open-drain support
- Complementary Outputs through the PIC
- Bypassable glitch filter on every input
- Always on Hysteresis in the Input buffer
- Per I/O Early I/O Selection
- 50 Ω Driver Impedance to mitigate reflections on board
- Supports complementary outputs via external resistors for LVDS and subLVDS

HPIO (High-Performance I/O) operating with a VCCIO of 1.8 V down to 0.9 V:

- DDR4/LPDDR4 @ 2400 Mbps
- DDR3L @ 1866 Mbps
- LVDS Differential on every pair of I/O @ 1600 Mbps
- SUBLVDSE on every pair of I/O @ 800 Mbps
- SUBLVDS RX on every pair of I/O @ 1600 Mbps
- MIPI DPHY–- SLVS-200 @1800 Mbps
- SGMII TX/RX compatible with LVDS Electrical signaling
- LVCMOS18/12/10/09
- Programmable Drive Strengths (2 to 12 mA)
- On-Chip Termination.
- Dynamic control, trimmed on-chip 100 Ω differential termination resistor
- External and Internal (trainable) VREF in each bank
- Polarity Control for Differential RX and TX Paths
- Open drain
- Programmable Slew rates: Fast and Slow
- Programmable Tx pre-emphasis
- Complementary Outputs

For more information about DDR implementation in I/O Logic and DDR memory interface support, refer to Lattice Nexus 2 High-Speed I/O and External Memory Interface (FPGA-TN-02372).

2.7.1. Supported sysI/O Standards

Lattice Nexus 2 sysI/O buffers support both single-ended differential and differential standards. Single-ended standards can be further subdivided into internally ratioed standards such as LVCMOS, and externally referenced standards such as HSUL and SSTL. The buffers support the LVCMOS 0.9 V, 1.0 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V standards. Differential standards supported include LVDS, SLVS, differential LVCMOS, differential SSTL, differential HSUL, differential LVSTL, and differential POD. For better support of video standards, subLVDS and MIPI D-PHY are also supported. Table 2.3 and Table 2.4 provide a list of sysI/O standards supported in the Lattice Nexus 2 devices.

2.7.2. sysI/O Banking Scheme

Lattice Nexus 2 devices have up to 11 banks in total. For LN2-CT20 device, there are six banks on top and five banks on the bottom side of device. The lower density Lattice Nexus 2 device has less banks. The top banks support up to VCCIO 3.3 V while bottom banks support up to VCCIO 1.8 V. In addition, bottom banks support one external VREF input for flexibility to receive the referenced input level on the same bank. And it also has the internal generated VREF input, which can be trained. DDR4/LPDDR4 must use internal VREF. For the top bank 0, bank 1, and bank 2, these provide 52 total I/O, which is also the same for the bank 12, bank 13, and bank 14. For bottom banks, each bank is built with 52 data I/O and other power/ground pads. The data I/O is divided into four DQS Groups comprised of 12 I/O each, and four addition shared function I/O, like VREF_EXT, PLL clock input, and external resistor input. Figure 2.11 shows the location of each bank.

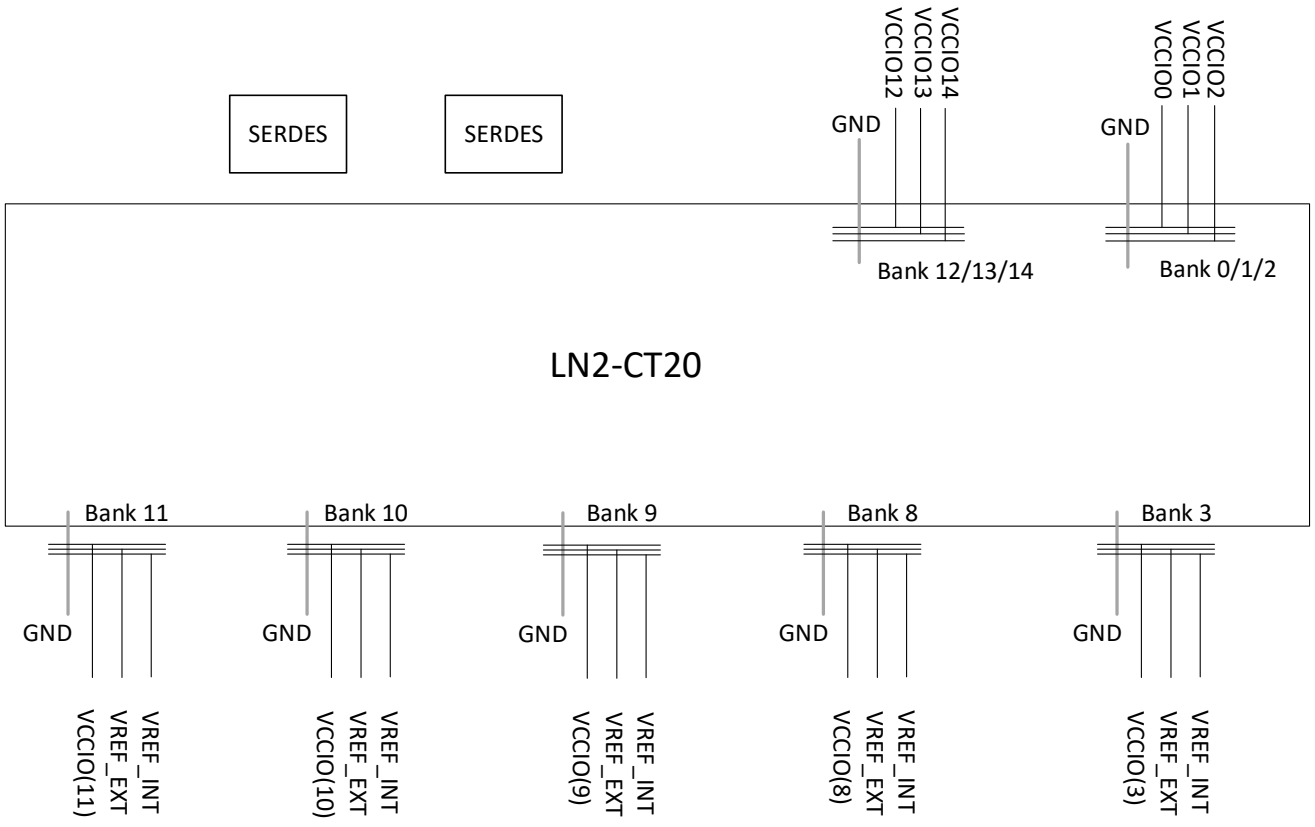


Figure 2.11. sysI/O Banking (LN2-CT20 Device)

Typical sysI/O Behavior During Power-up

The internal Power-On-Reset (POR) signal is deactivated when V_{CC} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated the FPGA core logic becomes active. It is the responsibility of the user to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in Lattice Nexus 2 devices, see the list of technical documentation in References section.

V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas V_{CCIO} supplies power to the I/O buffers. For the different power supply voltage levels supported by the I/O banks, refer to Lattice Nexus 2 sysI/O User Guide (FPGA-TN-02365) for detailed information.

sysI/O Standards Supported by I/O Bank

All banks can support multiple I/O standards under the VCCIO rules discussed above. Table 2.3 and Table 2.4 summarize the I/O standards supported on various sides of the Lattice Nexus 2 device.

Table 2.3. Single-Ended I/O Standards Supported on Various Sides

Standard	Top (WRIO)	Bottom (HPIO)	Input	Output	Bi-directional
LVCMOS33	Yes	—	Yes	Yes	Yes
LVCMOS25	Yes	—	Yes	Yes	Yes
LVCMOS18	Yes	Yes	Yes	Yes	Yes
LVCMOS12	Yes	Yes	Yes	Yes	Yes
LVCMOS10	—	Yes	Yes	Yes	Yes
LVCMOS09	—	Yes	Yes	Yes	Yes
SSTL 135	—	Yes	Yes	Yes	Yes
HSUL12	—	Yes	Yes	Yes	Yes
LVSTL11_I	—	Yes	Yes	Yes	Yes
LVSTL11_II	—	Yes	Yes	Yes	Yes
POD12	—	Yes	Yes	Yes	Yes
POD11	—	Yes	Yes	Yes	Yes

Table 2.4. Differential I/O Standards Supported on Various Sides

Standard	Top (WRIO)	Bottom (HPIO)	Input	Output	Bi-directional
LVDS	—	Yes	Yes	Yes	Yes
SUBLVDS	—	Yes	Yes	—	—
SLVS	—	Yes	Yes	Yes	—
SUBLVDSE	Yes	Yes	—	Yes	—
LVDSE	Yes	—	—	Yes	—
MIPI_D-PHY	—	Yes	Yes	Yes	Yes
SSTL135D	—	Yes	Yes	Yes	Yes
HSUL12D	—	Yes	Yes	Yes	Yes
LVSTL11D_I	—	Yes	Yes	Yes	Yes
LVSTL11D_II	—	Yes	Yes	Yes	Yes
POD12D	—	Yes	Yes	Yes	Yes
POD11D	—	Yes	Yes	Yes	Yes

For more information on the various sysI/O features available on the Lattice Nexus 2 device, refer to Lattice Nexus 2 sysI/O User Guide (FPGA-TN-02365).

2.8. Programmable I/O Cell (PIC)

The programmable I/O cells (PIC) provide I/O function and necessary gearing logic associated with PIO. Lattice Nexus 2 devices consist of base PIC and gearing PIC.

Base PICs contain three blocks: an input register block, output register block, and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic. Base PICs cover the top bank. Gearing PICs contain gearing logic and edge monitor used for locating the center of data window. Gearing PICs cover the bottom banks to support DDR operation.

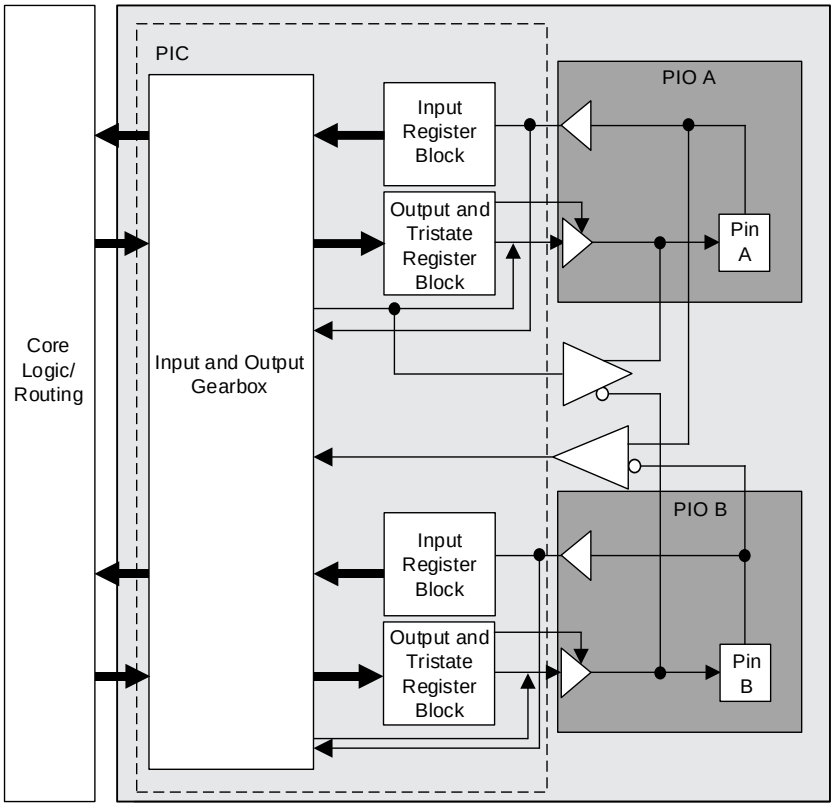


Figure 2.12. Group of Two High Performance Programmable I/O Cells

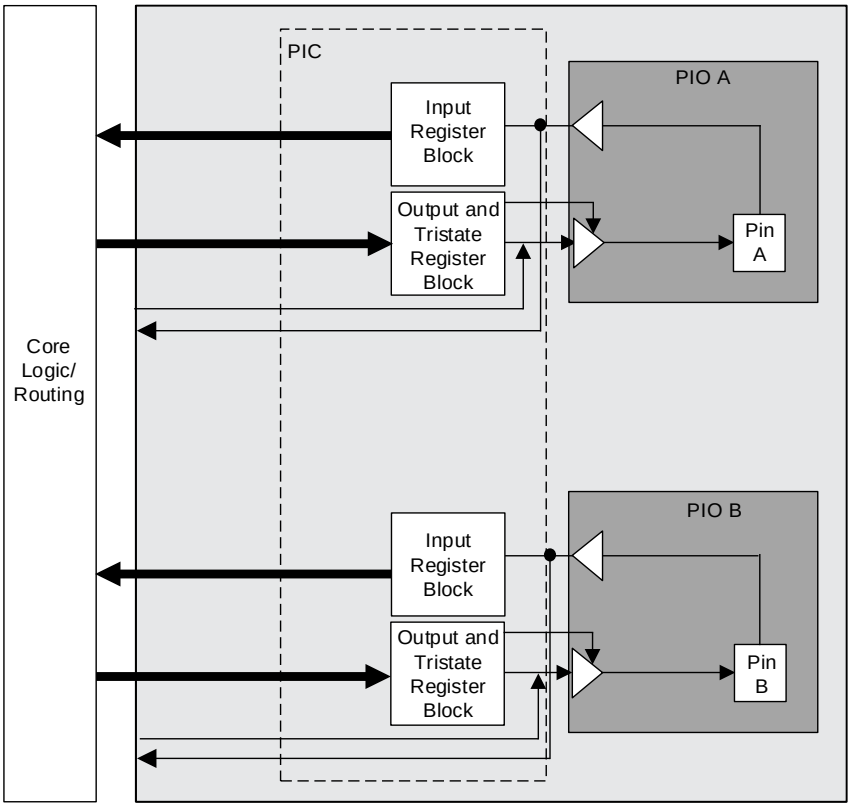


Figure 2.13. Wide Range Programmable I/O Cells

2.8.1. Input Register Block

The input register blocks for the PIO contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition, the input register blocks for the PIO on the bottom edges include built-in FIFO logic to interface to GDDR and xSPI.

The Input register block on the bottom side includes gearing logic and registers to implement 2:1, 4:1, 8:1, and 10:1 gearing functions. It can also implement the 7:1 gearing function used for 7:1 LVDS interfaces. It uses three sets of registers – shift, update, and transfer to implement gearing and the clock domain transfer. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. For more information on gearing function, refer to Lattice Nexus 2 High-Speed I/O and External Memory Interface (FPGA-TN-02372).

2.8.2. Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers.

The Lattice Nexus 2 output data path has programmable registers and output gearing logic. On the bottom side, the output register block can support 2:1, 4:1, 8:1, 10:1, and 7:1 gearing GDDR interfaces. On the top side, the banks support 2:1 gearing. The programmable delay cells are also available in the output data path.

For more information on gearing function, refer to Lattice Nexus 2 High-Speed I/O and External Memory Interface (FPGA-TN-02372).

2.8.3. Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation. In SDR, the TD input feeds one of the flip-flops that then feeds the output.

2.9. DDR Memory Support

Lattice Nexus 2 DDRPHY is compliant with the DFI 4.0+ specification and supports multiple DDR memory standards: DDR4/LPDDR4 and DDR3L. Table 2.5 lists a summary of Lattice Nexus 2 devices supported memory standards and the max speed rates.

Table 2.5. Summary of DDR Standards and Max Rates

Standard	Max Speed[1]
DDR4/LPDDR4	2400 Mbps
DDR3L	1866 Mbps

Note:

1. Max speeds reflect single-rank configurations only.

2.9.1. DDRPHY Overview

The Lattice Nexus 2 DDRPHY interface provides a physical interface between the FPGA soft memory controller and DRAM device. It consists of two logic blocks: 2:1 gearing logic and sync logic IP wrapper to implement quarter rate DDRPHY functionality.

Lattice Nexus 2 DDRPHY shares routing resources between the PIC and DDRPHY. In cases where the DDRPHY is partially used, the I/O can be configured in GDDR mode.

For DQ and CA lanes, the PHYCLK can operate up to 2.4 GHz to achieve 2.4 Gbps performance while leveraging a 300 MHz fabric interface clock.

For additional details on the Lattice Nexus 2 DDRPHY, refer to the Lattice Nexus 2 High-Speed I/O and External Memory Interface (FPGA-TN-02372).

2.9.2. DQS Grouping for DDR Memory

Lattice Nexus 2 DDRPHY occupies up to three HPIO banks, where each HPIO bank has 52 I/O.

Lattice Nexus 2 memory interfaces can support up to:

- x72 full DIMMs (three HPIO banks)[1]
- x40 half DIMM (two HPIO banks)
- x16 interfaces (one HPIO banks)

Note:

1. For LN2-CT20 and LN2-CT16 devices only.

In DDRPHY DDRx memory mode, the digital logic is partitioned into two types of lanes: DQ/DQS lanes and CA lanes. A DQS group contains six I/O pairs to provide 12 high-speed I/O. These can be configured as differential/complementary I/O or individual I/O. Within each DQS group, there are two pre-placed pins for DQS and DQSN signals. The rest of the pins in the DQS group can be used as DQ and DM/DMI/DBI signals. The number of pins bonded out in each DQS group is package dependent. For all Lattice Nexus 2 devices supported memory standards, a data lane occupies 11 bits in total: 8-bit DQ, DQS/DQSN, and DM/DMI/DBI. DDRPHY CA lane pin assignments are different based on the DDR standard used.

For additional details on the portioning of the DDRPHY, refer to the Lattice Nexus 2 High-Speed I/O and External Memory Interface (FPGA-TN-02372).

2.10. Device Configuration

Lattice Nexus 2 devices provide three ports that can be used for device configuration. The JTAG Port, the Controller SPI port, and the Target SPI port. Both SPI ports support x1, x2, x4, and xSPI (x8, dual transfer rate) protocols. The JTAG port, which has dedicated I/O, supports IEEE 1149.1 Boundary Scan, Lattice proprietary configuration protocol, and ispTracy™. CFGMODE, PROGRAMN, INITN, and DONE are dedicated configuration pins. The remaining sysCONFIG pins are used as dual function pins which become general purpose I/O by default once the device is configured. Refer to Lattice Nexus 2 sysCONFIG User Guide (FPGA-TN-02370) for more information about configuring the dual-use pins as sysCONFIG pins once the device is configured (known as persistence).

The following configuration interfaces are supported:

- Controller SPI (MSPI) – x1, x2, x4, xSPI (x8, dual transfer rate)
- Target SPI (SSPI)[1] – x1, x2, x4, xSPI (x8, dual transfer rate)
- JTAG (Lattice proprietary configuration protocol)

Note:

1. For Certus variants only.

On power-up, based on the voltage level (high or low) of the CFGMODE pin, the FPGA SRAM is configured by the appropriate sysCONFIG port. If CFGMODE pin is low, the FPGA is in Target configuration mode (Target SPI or JTAG). If CFGMODE pin is driven high, the FPGA is in Controller SPI booting mode. In Controller SPI booting mode, the FPGA boots from an external (LN2-CT) SPI flash.

2.10.1. Enhanced Configuration Options

The Lattice Nexus 2 devices have enhanced configuration features such as:

- Early I/O release
- Bitstream Decryption
- Bitstream Authentication
- Bitstream Compression
- Dual and Multi-boot images

With Early I/O Release, the I/O is released before the FGPA is fully configured so that customer systems have minimal disruption. For more details, refer to Lattice Nexus 2 sysCONFIG User Guide (FPGA-TN-02370).

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the Lattice Nexus 2 devices can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the Lattice Nexus 2 device can revert to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, refer to Lattice Nexus 2 sysCONFIG User Guide (FPGA-TN-02370).

2.10.2. Soft Error Detection and Correction (SEDC)

Lattice Nexus 2 devices have a Soft Error Detection and Correction (SEDC) module which can detect and correct SRAM errors due to Single Event Upsets (SEU). The SEDC module in Lattice Nexus 2 contains enhancements compared to the SEDC modules implemented in previous Lattice devices and can perform frame-level error detection and correction and chip-level multi-bit error detection.

The SEDC module reads data from the FPGA configuration memory and performs an Error Correction Code (ECC) calculation on every frame of configuration data. Single bit errors within a frame can be detected and corrected and dual bit errors within a frame can be detected but not corrected. Multi-bit errors in a single frame which are not detected by ECC and errors in multiple frames can be detected using a full-chip CRC. The SEDC module can be run in an automatic mode or user-controlled mode. In automatic mode, once a single bit error is detected it is automatically corrected and SEDC scanning resumes without user intervention. Dual bit errors which are detected but uncorrectable result in notification to the user and halt SEDC scanning. In user-controlled mode once an error is detected, the SEDC module halts and notifies the user. You can query the SEDC module to read the location of the error (if desired) and take any appropriate actions. You can then trigger the SED module to correct the error and continue scanning.

Lattice Nexus 2 devices also have dedicated logic to perform Cyclic Redundancy Code (CRC) checks for the entire SRAM array. You can trigger a full-chip CRC calculation on-demand and compare the results to the expected CRC value which is programmed into the device by the bitstream. Full-chip CRC calculation and SED frame scanning are mutually exclusive; only one of them can be running at a time.

The SEDC module does not check the contents of RAMs (EBRs and distributed RAM). EBRs contain their own optional error detection and correction capability using dedicated ECC logic.

2.11. Trace ID

Each Lattice Nexus 2 device contains a unique (per device) TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the SSPI and JTAG interfaces. For further information on TraceID, refer to Using TraceID (FPGA-TN-02084).

2.12. SERDES and PCS

The Lattice Nexus 2 platform SERDES/PCS is a multi-protocol PHY design with quad (x4) base. Each quad consists of the following:

- Quad x4 PMA: 4 Tx, 4 Rx, 1 common block (REFCLK,2 × Tx PLL)
- Multiple Protocol PCS (MPPCS)

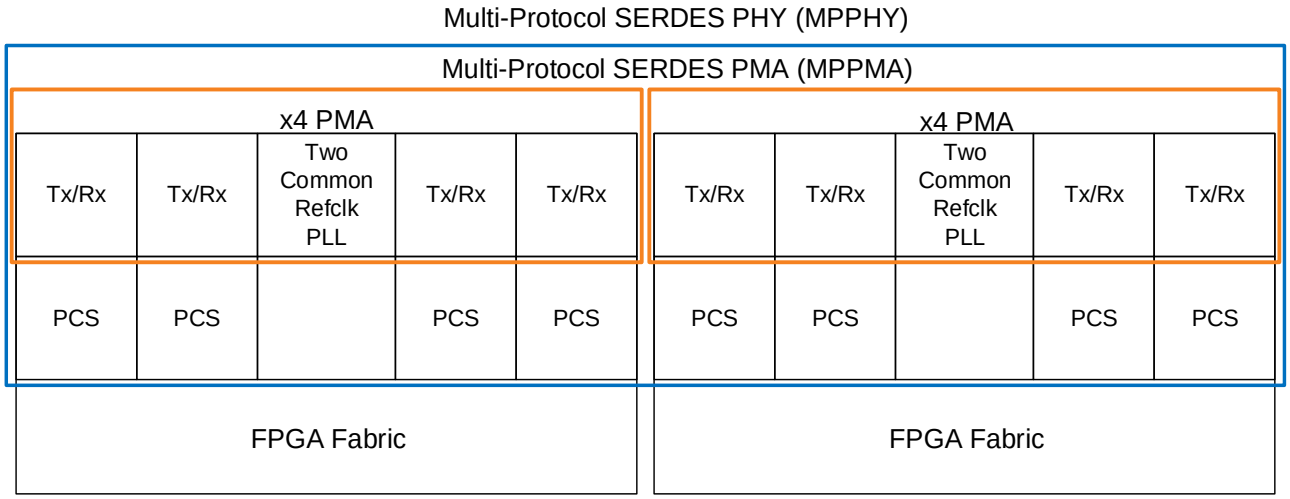


Figure 2.14. SERDES Overview Diagram

The Lattice Nexus 2 SERDES is in Quad x4 units. Each device may support multiple instances of Quad x4 units.

The PMA covers multiple sub-ranges of 1.25 Gbps to 16 Gbps. Table 2.6 shows the list of supported protocols.

Table 2.6. SERDES/PCS Supported Protocols

Protocol	PMA Support	PCS Support	Link and Upper Layer Support
PCIe Gen1/2/3	Yes	Yes	Hard DLL, TL, and DMA
PCIe Gen4	Yes	Yes	Hard DLL, TL, and DMA
10G Ethernet	Yes	Yes	Soft MAC in Fabric
DisplayPort	Yes	Yes	Soft logic in Fabric
SLVS-EC	Yes	Yes	Soft logic in Fabric
CoaXPress	Yes	Yes	Soft logic in Fabric
CPRI (x1, x2, x4, x8)	Yes	Yes	Soft logic in Fabric
eCPRI	Yes	Yes	Soft logic in Fabric
JESD204B	Yes	Yes	Soft logic in Fabric

Notes:

- Protocol performance speeds met with LFG and CBG packages. Other packages are limited to 10G.
- Platform support outlined. See tables in the Features section for capabilities supported in specific family.

Table 2.7. Lattice Nexus 2 SERDES Protocol Width Support

Protocol	Typical Width	Rate (Gbps) × Width Examples
PCIe	x1, x2, x4	(2.5, 5, 8, 16) × (1, 2, 4)
Ethernet	x1	1.25 × 1, 3.125 × 1, 3.125 × 4, 5 × 1, 6.25 × 2, 10.3125 × 1, Port Ethernet Switches
DP/eDP	x1, x2, x4	(1.62, 2.7, 5.4, 8.1) × (1, 2, 4)
SLVS-EC	x4, x8	(1.25, 2.5, 5) × (4, 8)
CoaXPress	x1, x2, x4, x8	(3, 6.25, 10, 12.5) × (1, 2, 4, 8)
CPRI	x1, x2, x4, x8	(1.2288, 2.4576, 3.072, 4.915, 6.144, 8.11008, 9.8304, 10.1376, 12.16512) x (1, 2, 4, 8)
eCPRI	x1	10.3125 × 1
JESD204B	x1, x2, x4, x8	(3.125, 6.25, 12.5) × (2, 4, 8)

Notes:

- Protocol performance speeds met with LFG and CBG packages. Other packages are limited to 10G.
- Platform support outlined. See tables in the Features section for capabilities supported in specific family.

In Lattice Nexus 2 devices, the wide bus width is supported with running reference clock distribution to each quad. Synchronization logic provided to ensure multiple x4 is in sync in the PMA IP.

2.12.1. SERDES/PMA Block

The PMA hard macro comprises of four lanes with a full duplex transceiver for each lane, each lane includes Transmitter (TX), Receiver (RX), Support, and test features. The TX lane receives 8, 10, 16, 20, 32, or 40 bits of transition-encoded data synchronous with a Tx clock, serializes it into a single stream of differential transmitted data and transmits to the lane. The transmitter supports multi-level output driver, multi-level transition emphasis, and multi-level Common Mode levels. The RX Lane performs a series function such as adaptive continuous-time linear equalization (CTLE), decision feedback equalization (DFE), and clock data recovery (CDR) to ensure recovered clock is used to retime received data with channel loss compensated and optimized and send it to deserializer which produces parallel data and a parallel data clock for the relevant PCS lane. The Support block provides all the common functions for the RX/TX link, TX clock generation, TX/RX termination calibration, biasing voltage, and reference clock buffering.

2.12.2. Multi-Protocol PCS (MPPCS)

The Lattice Nexus 2 Platform SERDES supports multi-protocol PCS with key features below:

- Encoder/Decoder: 8B10B, 64B/66B, 128B/130B.
- Comma detection and word alignment
- Clock tolerance Elastic FIFO
- Gearing to FPGA by 8/10/16/20/32/40/64/80/128
- Built in Pipe Control Interface for PCIe
- GMII/XGMII/XLGMII/CGMII for Ethernet
- Forward Error Correction (FEC) supporting both:
  - BASE-R/Fire Code FEC
  - KR RS-FEC 528,514 FEC (Reed-Solomon)
- Programmable Interface Width/Speed to connect to either hard IP (PCIe LL controller) or FPGA fabric
- Channel bonding, for channels within quads, and between quads: Rx FIFO alignment and Tx FIFO delay adjustment to minimize channel to channel skew.
- Parallel loopback mode for testability

Protocol support varies by family. See the Features section for details of protocols supported in a specific family.

2.12.3. Multi-Protocol PHY (MPPHY) Integration

Figure 2.15 shows the MPPHY top-level integration block diagram.

Each PMA Lane has a corresponding PCS lane. The 40-bit SERDES interface between PMA, PCS, and the 32-bit PIPE interface between PCS and link layer follow the Intel Standard PHY Interface [PHY].

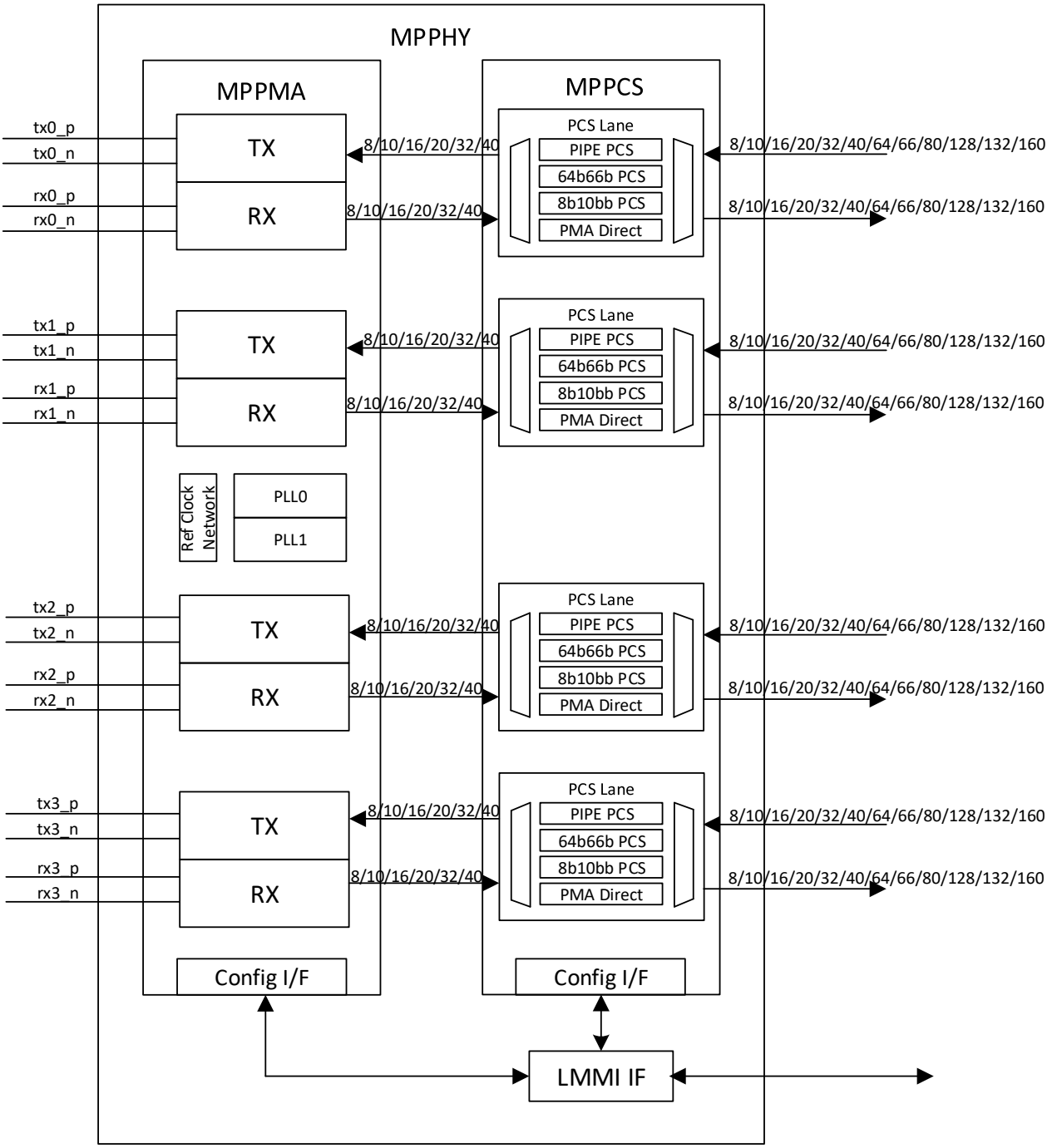


Figure 2.15. MPPHY Top-Level Block Diagram

2.12.4. Peripheral Component Interconnect Express (PCIe)

The Lattice Nexus 2 device features up to four lanes of hardened PCIe, with a maximum PCIe link width of x4. The PCIe block implements all three layers defined by the PCI Express Specification: Physical, Data Link, and Transaction as shown in Figure 2.16. Below is a summary of the features supported by the PCIe block:

- PCIe Express Base Specification 4.0 compliant including compliance with earlier PCI Express Specifications
- Support for link width of x4 PCI Express Lanes with support for bifurcation, including 1 × 4, 1 × 2, and 1 × 1
- 16.0 GT/s, 8.0 GT/s, 5.0 GT/s, and 2.5 GT/s line rate support
- Multi-function support with up to eight physical functions
- Support for Autonomous and Software-Controlled Equalization
- Support for Figure of Merit and Up/Down PIPE PHY Equalization
- Flexible Equalization methods (Algorithm, Preset, User-Table, Adaptive-Table, Firmware-controlled)
- ECC RAM and Parity Data Path Protection
- 64-bit Core Data Width (per lane)
- Robust Error-Handling support, including AER, ECRC generation/checking, recovery from parity and ECC errors, and error injection diagnostics.
- Optional Hardened high-performance multi-channel scatter-gather DMA controller
- Support for power management features including ASPM L0s and L1, L1 PM states with CLKREQ, Power Budgeting, and Dynamic Power Allocation

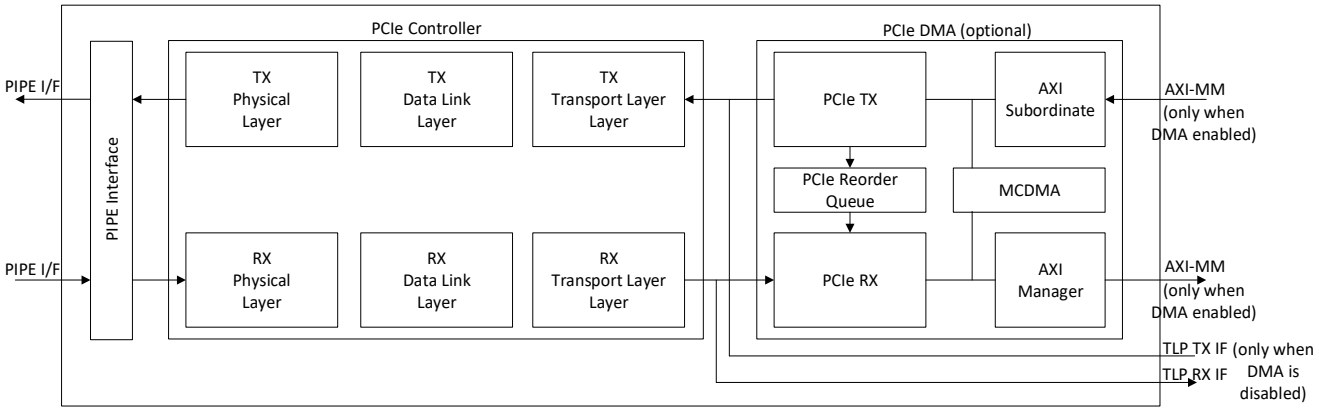


Figure 2.16. PCIe Core

The hardened PCIe block can be instantiated using the PCIe IP Core through the Radiant IP Catalog and IP Block Wizard. In Figure 2.17, the PCIe core is configured as an Endpoint using a soft IP wrapper that provides useful functions such as bridging support for bus interfaces and DMA applications. In addition to the standard Transaction Layer Packet (TLP) interface, the data interface can also be configured to be AXI4 as well. The PCIe hardened block also features a register interface for the Lattice Memory Mapped Interface (LMMI). The PCIe block has many registers which contain information about the current status of the PCIe block as well as the capability to dynamically switch PCIe settings. These registers can also be accessed through the Reveal Controller Tool.

For more information about the PCIe soft IP, refer to the PCIe Endpoint IP Core document.

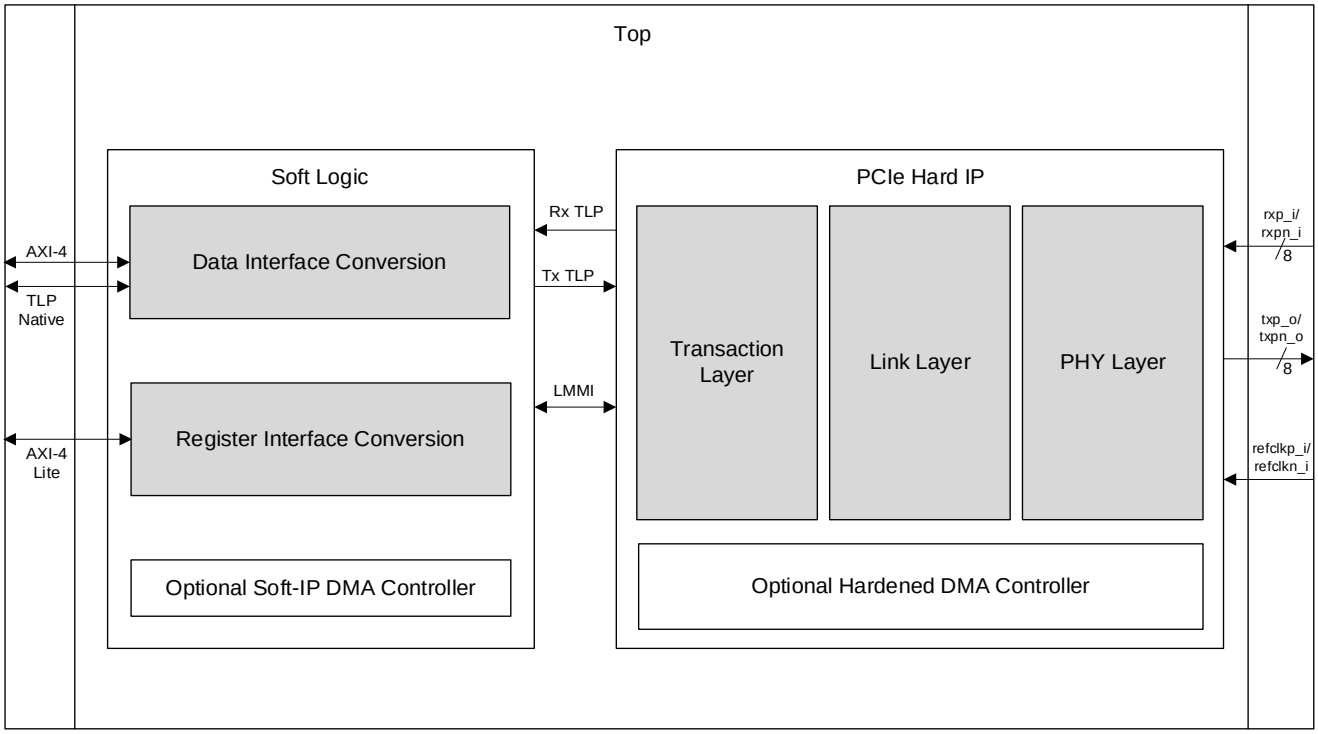


Figure 2.17. PCIe Soft IP Wrapper

2.13. Pin Migration

The Lattice Nexus 2 platform is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a low utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization impact the likelihood of success in each case. An example is that some user I/O may become No Connects in smaller devices in the same package. Refer to the Lattice Nexus 2 Pin Migration Tables and Lattice Radiant software for specific restrictions and limitations.

2.14. Security

The Lattice Nexus 2 platform provides advanced bitstream security and user security features. These security features represent a significant step up in capabilities and performance compared to previous Lattice products.

Security features include:

- Bitstream Encryption
- Bitstream Authentication
- User-accessible cryptographic APIs
- Physically Unclonable Function (PUF)
- Strong resistance to side channel analysis (SCA) and fault injection (FIA) attacks
- Anti-tamper detection and remedies with various severity levels

Security support varies by family. See the Features section for details of security support in a specific family.

Lattice Nexus 2 devices support bitstream security features such as bitstream encryption (AES-256-GCM) for protecting the confidentiality of FPGA bitstream data, and bitstream authentication (ECDSA or RSA) which ensures bitstream integrity and authenticity, protecting the FPGA design bitstream from accidental or unauthorized tampering. Bitstream authentication supports user-selectable algorithms and key strengths.

Lattice Nexus 2 devices support user security features which are available to a user's design after device configuration has completed. User security features are accessible through user security APIs which are implemented using a message-based control interface. User security APIs access data for cryptographic functions through an AXI4 manager interface and AXI-Stream transmit and receive interfaces to the user's design in fabric, as shown in Figure 2.18.

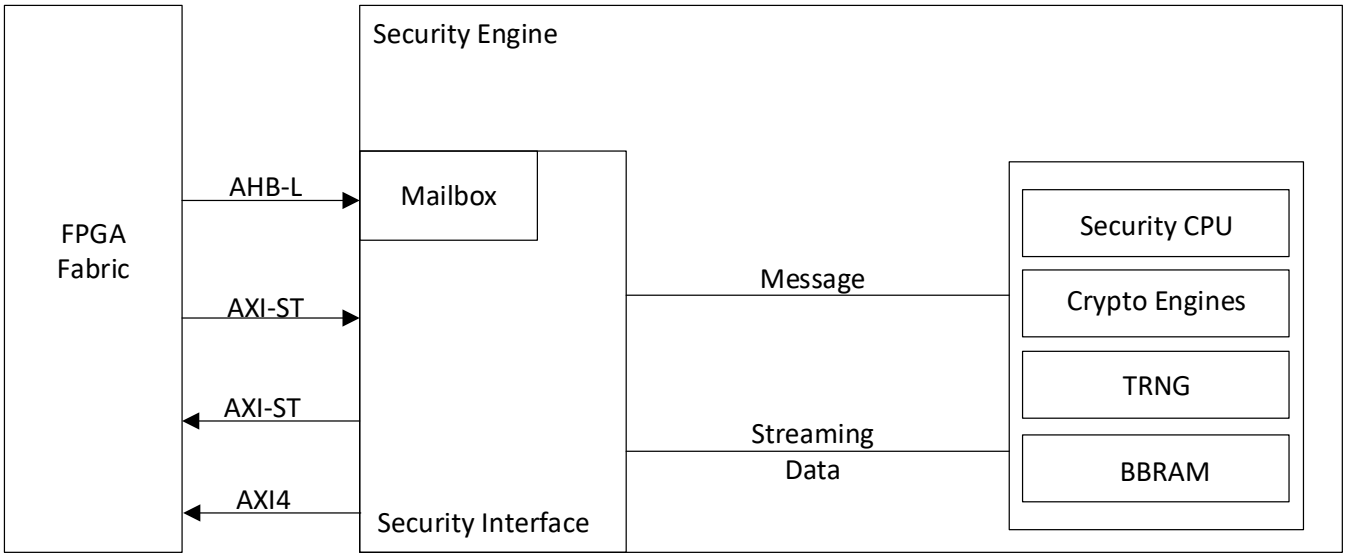


Figure 2.18. Cryptographic Engine Block Diagram

The Lattice Nexus 2 platform supports the following cryptographic algorithms and security functions:

- True Random Number Generator (TRNG)
- Fortified AES-256, up to 2.5 Gbps throughput
- Fast AES-256, up to 10 Gbps throughput
- SHA2 and SHA3, 256/384/512-bit
- HMAC-SHA2, 256/384/512-bit
- Elliptic Curve Cryptography (ECC), 256/384/521-bit
  - ECDSA, ECDH, ECIES
- RSA Cryptography, 2048/3072/4096-bit

Lattice Nexus 2 devices include a Physically Unclonable Function (PUF) with 256 bits of entropy and a stable lifetime > 20 years. The PUF provides an unclonable device-unique value which is used to derive secure device-specific values for various purposes, such as device identification and encryption keys. This provides an extra layer of security unique to each device. The PUF is part of the cryptographic engine and all PUF-derived secrets are never exposed outside the cryptographic engine.

The cryptographic engine has direct access to Battery Backed RAM (BBRAM), which can be used as nonvolatile storage for sensitive information. Unlike OTP, BBRAM can be programmed more than once, and the content cannot be easily read through physical inspection. Usage of BBRAM is optional (enabled by a user writable OTP bit). By default, OTP is used for persistent storage of user-programmed secrets but if BBRAM is enabled, BBRAM is used for all user-programmed secrets.

2.15. Anti-Tamper Monitor

The Anti-Tamper Monitor (ATM) uses analog sensors to measure on-die temperatures and voltages of critical power supplies. The ATM can be used to continuously provide sampled voltage and temperature data, or it can be programmed to trigger alarm interrupts based on user-defined upper and lower threshold values. The ATM also provides an interface for user logic to trigger one or more remedy actions if the user determines that tampering has been detected. Remedy actions vary in severity and include zeroization of FPGA SRAM and EBRs, zeroization of user secrets in secure volatile storage (SRAM), zeroization of user secrets in secure persistent storage (OTP or BBRAM), or even permanently disabling the device.

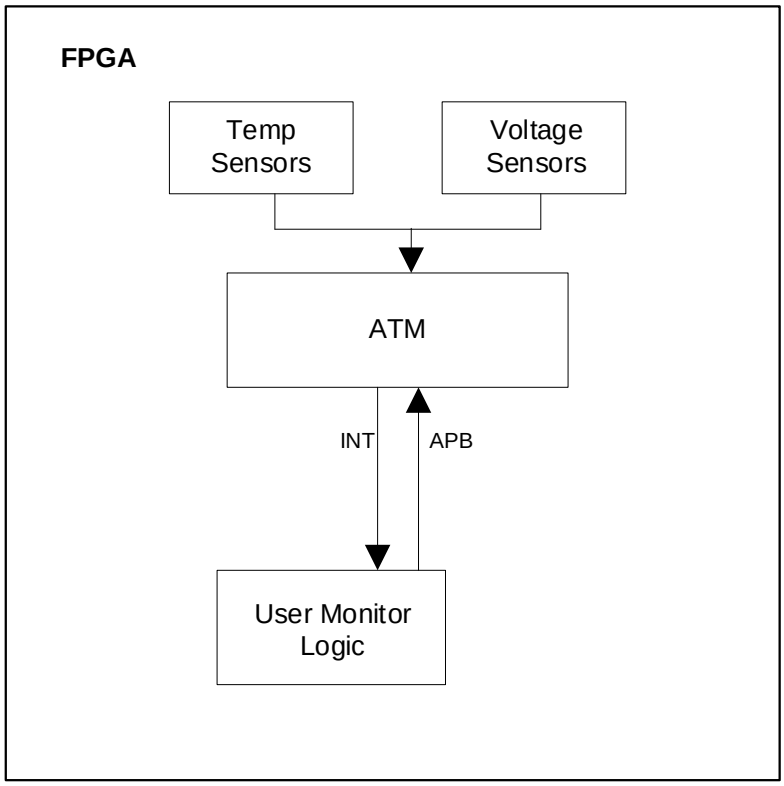


Figure 2.19. ATM Block Diagram

3. Pinout Information

3.1. Signal Descriptions

Table 3.1. Signal Descriptions

Signal Name	Bank	Type	Description
Power and GND			
Vss	—	GND	Ground for internal FPGA logic and I/O
V_{SSR}	—	GND	Reserved. Connect to Ground.
V_{CC}	—	Power	Power supply pins for core logic. V_{CC} is connected to 0.82 V (nom.) supply voltage. Power On Reset (POR) monitors this supply voltage.
V_{CCAUXA}	—	Power	Auxiliary power supply pin for internal analog circuitry. This supply is connected to 1.8 V (nom.) supply voltage. POR monitors this supply voltage.
V_{CCAUX}	—	Power	Auxiliary power supply. This supply is connected to 1.8 V (nom.) supply voltage, and is used for generating stable drive current for the I/O.
V_{CCA_PLLx}	—	Power	Used by the PLL blocks. This supply is connected to 0.82 V (nom.) supply voltage. X can be various PLL numberings.
V_{CC_BAT}	—	Power	This supply can be connected to 1.5 V (nom.) supply voltage. It allows a battery to be used to keep the volatile RAM configuration when the other DC supply source is absent.
V_{CCIOx}	0–14	Power	Power supply pins for I/O bank x. For x = 0, 1, 2, 12, 13, and 14, VCCIO can be connected to (nom.) 1.2 V, 1.8 V, 2.5 V, or 3.3 V. For x = 3, 4, 5, 6, 7, 8, 9, 10, and 11, VCCIO can be connected to (nom.) 0.9, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V. There are dedicated and shared configuration pins in banks 1 and 2. POR monitors these banks supply voltages.
V_{CCA_MPQx}	—	Power	Power supply for the SERDES blocks. X = 0, 1, 2, 3, 4, 5, 6
V_{CCH_MPQx}	—	Power	Power supply for the SERDES blocks. X = 0, 1, 2, 3, 4, 5, 6
Dedicated SERDES I/O Pins			
MPQx_RXyP/N	MPQ0	Input	SERDES Data Differential Input Pairs. X=0, 1, 2, 3, 4, 5, 6. Y=0, 1, 2, 3
MPQx_TXyDP/N	MPQ0	Output	SERDES Data Differential Output Pairs. X=0, 1, 2, 3, 4, 5, 6. Y=0, 1, 2, 3
MPQx_REFCLKP/N	MPQ0	Input	SERDES Reference Clock Differential Input Pairs. X=0, 1, 2, 3, 4, 5, 6
REXT_MPQx	MPQ0	Input	SERDES External Reference Resistor Input. This is used to adjust the on-chip differential termination impedance, based on the external resistance value. X=0, 1, 2, 3, 4, 5, 6
Misc Pins			
NC	—	—	No connect.

Signal Name	Bank	Type	Description
General Purpose I/O Pins			
WRIO[BankNumber]_[Number][A/B]	0, 1, 2, 12, 13, 14	Input, Output, Bi-Dir	Programmable Wide Range User I/O: [BankNumber] indicates the package pin/ball is in the bank specified. [Number] identifies the PIO [A/B] pair. [A/B] shows the package pin/ball is A or B signal in the pair. PIO A and PIO B are grouped as a pair. Each A/B pair in the top bank does not support true differential input or output buffer. It supports all single-ended inputs and outputs and can be used for emulated differential output buffer. Some of these user programmable I/O are used during configuration, depending on the configuration mode. You need to make the appropriate connection on the board to isolate the two different functions before/after configuration. During configuration the user-programmable I/O are tri-stated with an internal weak pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tri-stated and default to have weak pull-down enabled after configuration.
HPIO[BankNumber]_[Number][A/B]	3, 4, 5, 6, 7, 8, 9, 10, 11	Input, Output, Bi-Dir	Programmable High-Performance User I/O: [BankNumber] indicates the package pin/ball is in the bank specified. [Number] identify the PIO [A/B] pair. [A/B] shows the package pin/ball is A or B signal in the pair. PIO A and PIO B are grouped as a pair. Each A/B pair in the bottom banks supports true differential input and output buffers. When configured as differential input, differential termination of 100 Ω can be selected. During configuration the user-programmable I/O are tri-stated with an internal weak pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tri-stated and default to have weak pull-down enabled after configuration.
Shared Configuration Pins **1. These pins can be used for configuration during configuration mode. When configuration is completed, these pins can be used as GPIO, or shared function in GPIO. When these pins are used in dual function, the user needs to isolate the signal paths for the dual functions on the board.** **2. The pins used are defined by the configuration modes detected. Target SPI modes are detected during target activation. Pins that are not used in the configuration mode selected are tri-stated during configuration and can connect directly as GPIO in user's function.**			
WRIO2_yy/SDQ0:7	2	Input, Output, Bi-Dir	Configuration: Target SPI Mode: Slave Parallel Data User Mode: WRIO2_yy: GPIO
WRIO2_yy/SSDO	2	Input, Output, Bi-Dir	Configuration: Target SPI Mode: Slave Serial Output User Mode: WRIO2_yy: GPIO
WRIO2_yy/SCSN	2	Input, Output, Bi-Dir	Configuration: Target SPI Mode: Slave Chip Select User Mode: WRIO2_yy: GPIO
WRIO2_yy/SCLK	2	Input, Output, Bi-Dir	Configuration: Target SPI Mode: Slave Clock Input User Mode: WRIO2_yy: GPIO

Signal Name	Bank	Type	Description
WRIO2_yy/SDS	2	Input, Output, Bi-Dir	Configuration: Target SPI Mode: Slave Data Strobe User Mode: WRIO2_yy: GPIO
WRIO1_yy /MCSN	1	Input, Output, Bi-Dir	Configuration: Controller SPI Mode: Master Chip Select User Mode: WRIO1_yy: GPIO
WRIO1_yy /MSDO	1	Input, Output, Bi-Dir	Configuration: Controller SPI Mode: Master Serial Data Out User Mode: WRIO1_yy: GPIO
WRIO1_yy /MDS	1	Input, Output, Bi-Dir	Configuration: Controller SPI Mode: Master Data Strobe User Mode: WRIO1_yy: GPIO
WRIO1_yy /MDQ0:7	1	Input, Output, Bi-Dir	Configuration: Controller SPI Mode: Master Parallel Data User Mode: WRIO1_yy: GPIO
WRIO1_yy /MCLK	1	Input, Output, Bi-Dir	Configuration: Controller SPI Mode: Master Clock Output User Mode: WRIO1_yy : GPIO
WRIO1_yy /MCLKN	1	Input, Output, Bi-Dir	Configuration: Controller SPI Mode: Master Clock Output User Mode: WRIO1_yy : GPIO
Dedicated Pins **1. Dedicated pins are used for specific configuration functions**			
Dedicated Pins			
TDO	2	Output	Used as TDO signal for JTAG
TDI	2	Input	Used as TDI signal for JTAG
TMS	2	Input	Used as TMS signal for JTAG
TCK	2	Input	Used as TCK signal for JTAG
CFGMODE	2	Input	When low, enables JTAG and SSPI modes. When high, enables MSPI mode.
PROGRAMN	2	Input	Initiate configuration sequence when pulsed LOW.
INITN	2	Input, Output, Bi-Dir	Open Drain I/O pin. This signal is driven to LOW when configuration sequence is started, to indicate the device is in initialization state. This signal is released after initialization is completed, and the configuration download can start. You can drive this signal LOW to delay the start of configuration download.
DONE	2	Input, Output, Bi-Dir	Open Drain I/O pin. This signal is driven to LOW during configuration time. It is released to indicate the device has completed configuration. You can drive this signal LOW to delay device wake up after configuration.

Signal Name	Bank	Type	Description
ERASEKEY	1	Input	Trigger erase of BBRAM and OTP security keys. Pin is disabled by default, enabled by an OTP setting.
EXT_RES[3,4,5,6,7,8,9,10,11]	3, 4, 5, 6, 7, 8, 9, 10, 11	Input	EXT_RES: External reference resistor [3,4,5,6,7,8,9,10,11] = Bank
Shared CLOCK Pins **1. Some PCLK pins can also be used as GPLL reference clock input pin. Refer to Lattice Nexus 2 sysCLOCK PLL Design and User Guide (FPGA-TN-02364).**			
WRIOx_zz/PCLK[R]T[0,1,2]_[0, 1]/yyyy	0, 1, 2, 12, 13, 14	Input, Output, Bi-Dir	User Mode: WRIOx_zz: GPIO PCLK: Primary Clock Refclk signal [0,1,2,12,13,14] = Bank [0,1] Up to 2 signals in the bank yyyy: Other possible selectable specific functional
WRIOx_zz/PLLT[FB][0,12]_IN/yyyy	0, 12	Input, Output, Bi-Dir	User Mode: HPIOx_zz: GPIO PLL: PLL signal [0,12] = Bank [FB] Used if input is for PLL feedback yyyy: Other possible selectable specific functional
HPIOx_zz/PCLK[R][T,C][3,4,5,6,7,8,9,10,11]_[0,1,2,3]/yyyy	3, 4, 5, 6, 7, 8, 9, 10, 11	Input, Output, Bi-Dir	User Mode: HPIOx_zz: GPIO PCLK: Primary Clock Refclk signal [T,C] = True or Complement if using differential signaling [3,4,5,6,7,8,9,10,11] = Bank [0,1,2,3] Up to 4 signals in bank yyyy: Other possible selectable specific functional
HPIOx_zz/PLL[T,C][3,4,5,6,7,8,9,10,11]_IN	3, 4, 5, 6, 7, 8, 9, 10, 11	Input, Output, Bi-Dir	User Mode: HPIOx_zz: GPIO PLL: PLL input signal [T,C] = True or Complement if using differential signaling [3,4,5,6,7,8,9,10,11] = Bank
Shared Reference Pins			
HPIOx_zz/VREF[3,4,5,6,7,8,9,10,11]	3, 4, 5, 6, 7, 8, 9, 10, 11	Input, Output, Bi-Dir	User Mode: HPIOx_zz: GPIO VREF: External voltage reference [3,4,5,6,7,8,9,10,11] = Bank

Note:

1. Not all signals are available as external pins in all packages. Refer to the Pinout List file for various package details.

3.2. Pin Information Summary

3.2.1. Lattice Certus-N2 Family

Table 3.2. Lattice Certus-N2 Family

Pin Information Summary		LN2-CT06				LN2-CT10				LN2-CT16			LN2-CT20			
		ASG187	ASG273	CBG256	CBG484	ASG187	ASG273	CBG256	CBG484	ASG410	CBG484	LFG672	ASG410E	ASG410	CBG484	LFG672
User I/O Pins																
Wide Range Inputs/Outputs per Bank	Bank 0	—	—	—	—	—	—	—	—	—	—	—	15	—	15	—
	Bank 1	—	—	—	—	—	—	—	—	—	—	—	15	—	15	—
	Bank 2	—	—	—	—	—	—	—	—	—	—	—	12	—	12	—
	Bank 12	—	—	—	—	—	—	—	—	—	—	—	16	—	16	—
	Bank 13	—	—	—	—	—	—	—	—	—	—	—	16	—	16	—
	Bank 14	—	—	—	—	—	—	—	—	—	—	—	20	—	20	—
Total Wide Range User I/O		—	—	—	—	—	—	—	—	—	—	—	94	—	94	—
High Performance Input/Output Pairs	Bank 3	—	—	—	—	—	—	—	—	—	—	—	51	—	51	—
	Bank 4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 9	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 10	—	—	—	—	—	—	—	—	—	—	—	51	—	51	—
	Bank 11	—	—	—	—	—	—	—	—	—	—	—	51	—	51	—
Total High Performance I/O		—	—	—	—	—	—	—	—	—	—	—	153	—	153	—
Power Pins																
V_{CC}		—	—	—	—	—	—	—	—	—	—	—	40	—	18	—
V_{CC_PLL}, $V_{CC\_PLL\_W}$		—	—	—	—	—	—	—	—	—	—	—	4	—	4	—
V_{CC_BAT}		—	—	—	—	—	—	—	—	—	—	—	1	—	1	—
V_{CCAUXA}		—	—	—	—	—	—	—	—	—	—	—	1	—	1	—
V_{CCAUX}		—	—	—	—	—	—	—	—	—	—	—	11	—	3	—
V_{CCIO}	Bank 0	—	—	—	—	—	—	—	—	—	—	—	1	—	2	—
	Bank 1	—	—	—	—	—	—	—	—	—	—	—	1	—	2	—
	Bank 2	—	—	—	—	—	—	—	—	—	—	—	2	—	3	—
	Bank 3	—	—	—	—	—	—	—	—	—	—	—	2	—	4	—
	Bank 4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 9	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 10	—	—	—	—	—	—	—	—	—	—	—	2	—	5	—
	Bank 11	—	—	—	—	—	—	—	—	—	—	—	2	—	4	—
	Bank 12	—	—	—	—	—	—	—	—	—	—	—	1	—	2	—
	Bank 13	—	—	—	—	—	—	—	—	—	—	—	1	—	2	—
	Bank 14	—	—	—	—	—	—	—	—	—	—	—	1	—	2	—
Total Power Pins		—	—	—	—	—	—	—	—	—	—	—	70	—	53	—

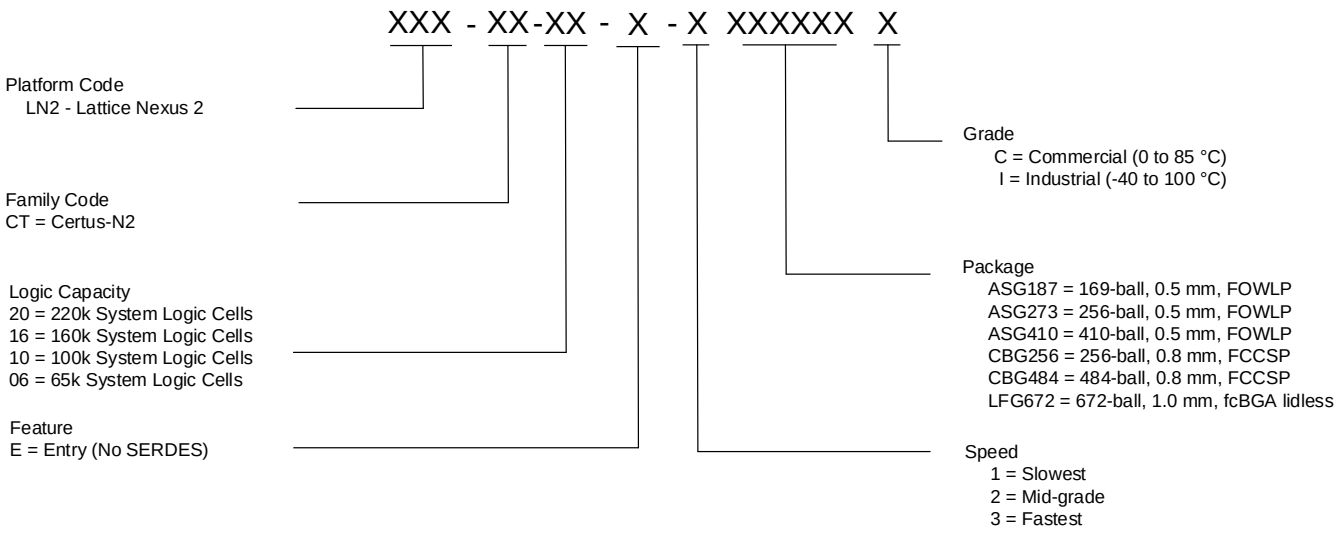
Pin Information Summary		LN2-CT06				LN2-CT10				LN2-CT16			LN2-CT20			
		ASG187	ASG273	CBG256	CBG484	ASG187	ASG273	CBG256	CBG484	ASG410	CBG484	LFG672	ASG410E	ASG410	CBG484	LFG672
GND and NC Pins																
Vss		—	—	—	—	—	—	—	—	—	—	—	80	—	87	—
V_{SSR}		—	—	—	—	—	—	—	—	—	—	—	2	—	2	—
NC		—	—	—	—	—	—	—	—	—	—	—	0	—	54	—
Dedicated Pins																
Dedicated SERDES Pins		—	—	—	—	—	—	—	—	—	—	—	—	—	30	—
Dedicated Misc Pins																
JTAG (TDI, TDO, TCK, TMS)		—	—	—	—	—	—	—	—	—	—	—	4	—	4	—
PROGRAMN		—	—	—	—	—	—	—	—	—	—	—	1	—	1	—
CFGMODE		—	—	—	—	—	—	—	—	—	—	—	1	—	1	—
DONE		—	—	—	—	—	—	—	—	—	—	—	1	—	1	—
INITN		—	—	—	—	—	—	—	—	—	—	—	1	—	1	—
EXT_RESn		—	—	—	—	—	—	—	—	—	—	—	3	—	3	—
Total Dedicated Pins		—	—	—	—	—	—	—	—	—	—	—	11	—	11	—
Shared Pins																
Shared Configuration Pins	Bank 1	—	—	—	—	—	—	—	—	—	—	—	13	—	13	—
	Bank 2	—	—	—	—	—	—	—	—	—	—	—	12	—	12	—
Shared PCLK Pins	Bank 0	—	—	—	—	—	—	—	—	—	—	—	2	—	2	—
	Bank 1	—	—	—	—	—	—	—	—	—	—	—	1	—	1	—
	Bank 2	—	—	—	—	—	—	—	—	—	—	—	1	—	1	—
	Bank 3	—	—	—	—	—	—	—	—	—	—	—	8	—	8	—
	Bank 4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 9	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 10	—	—	—	—	—	—	—	—	—	—	—	8	—	8	—
	Bank 11	—	—	—	—	—	—	—	—	—	—	—	8	—	8	—
	Bank 12	—	—	—	—	—	—	—	—	—	—	—	2	—	2	—
	Bank 13	—	—	—	—	—	—	—	—	—	—	—	1	—	1	—
	Bank 14	—	—	—	—	—	—	—	—	—	—	—	1	—	1	—

Pin Information Summary		LN2-CT06				LN2-CT10				LN2-CT16			LN2-CT20			
		ASG187	ASG273	CBG256	CBG484	ASG187	ASG273	CBG256	CBG484	ASG410	CBG484	LFG672	ASG410E	ASG410	CBG484	LFG672
Shared Reference Pins	Bank 0	—	—	—	—	—	—	—	—	—	—	—	0	—	0	—
	Bank 1	—	—	—	—	—	—	—	—	—	—	—	0	—	0	—
	Bank 2	—	—	—	—	—	—	—	—	—	—	—	0	—	0	—
	Bank 3	—	—	—	—	—	—	—	—	—	—	—	1	—	1	—
	Bank 4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 9	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Bank 10	—	—	—	—	—	—	—	—	—	—	—	1	—	1	—
	Bank 11	—	—	—	—	—	—	—	—	—	—	—	1	—	1	—
	Bank 12	—	—	—	—	—	—	—	—	—	—	—	0	—	0	—
	Bank 13	—	—	—	—	—	—	—	—	—	—	—	0	—	0	—
	Bank 14	—	—	—	—	—	—	—	—	—	—	—	0	—	0	—

4. Ordering Information

Lattice provides a wide variety of services for its products including custom marking, factory programming, known good die, and application specific testing. Contact the local sales representatives for more details.

4.1. Lattice Nexus 2 Part Number Description



4.2. Ordering Part Numbers

4.2.1. Commercial

Table 4.1. Commercial Part Numbers

Part Number	Speed	Package	Pins	Grade	System Logic Cells (k)
LN2-CT-20E-1ASG410C	1	ASG410	410	Commercial	220
LN2-CT-20E-2ASG410C	2	ASG410	410	Commercial	220
LN2-CT-20E-3ASG410C	3	ASG410	410	Commercial	220
LN2-CT-20-1ASG410C	1	ASG410	410	Commercial	220
LN2-CT-20-2ASG410C	2	ASG410	410	Commercial	220
LN2-CT-20-3ASG410C	3	ASG410	410	Commercial	220
LN2-CT-20-1CBG484C	1	CBG484	484	Commercial	220
LN2-CT-20-2CBG484C	2	CBG484	484	Commercial	220
LN2-CT-20-3CBG484C	3	CBG484	484	Commercial	220
LN2-CT-20-1LFG672C	1	LFG672	672	Commercial	220
LN2-CT-20-2LFG672C	2	LFG672	672	Commercial	220
LN2-CT-20-3LFG672C	3	LFG672	672	Commercial	220
LN2-CT-16E-1ASG410C	1	ASG410	410	Commercial	160
LN2-CT-16E-2ASG410C	2	ASG410	410	Commercial	160
LN2-CT-16E-3ASG410C	3	ASG410	410	Commercial	160
LN2-CT-16-1ASG410C	1	ASG410	410	Commercial	160
LN2-CT-16-2ASG410C	2	ASG410	410	Commercial	160
LN2-CT-16-3ASG410C	3	ASG410	410	Commercial	160
LN2-CT-16-1CBG484C	1	CBG484	484	Commercial	160
LN2-CT-16-2CBG484C	2	CBG484	484	Commercial	160
LN2-CT-16-3CBG484C	3	CBG484	484	Commercial	160
LN2-CT-16-1LFG672C	1	LFG672	672	Commercial	160
LN2-CT-16-2LFG672C	2	LFG672	672	Commercial	160
LN2-CT-16-3LFG672C	3	LFG672	672	Commercial	160
LN2-CT-10-1ASG187C	1	ASG187	187	Commercial	100
LN2-CT-10-2ASG187C	2	ASG187	187	Commercial	100
LN2-CT-10-3ASG187C	3	ASG187	187	Commercial	100
LN2-CT-10-1ASG273C	1	ASG273	273	Commercial	100
LN2-CT-10-2ASG273C	2	ASG273	273	Commercial	100
LN2-CT-10-3ASG273C	3	ASG273	273	Commercial	100
LN2-CT-10-1CBG256C	1	CBG256	256	Commercial	100
LN2-CT-10-2CBG256C	2	CBG256	256	Commercial	100
LN2-CT-10-3CBG256C	3	CBG256	256	Commercial	100
LN2-CT-10-1CBG484C	1	CBG484	484	Commercial	100
LN2-CT-10-2CBG484C	2	CBG484	484	Commercial	100
LN2-CT-10-3CBG484C	3	CBG484	484	Commercial	100
LN2-CT-06-1ASG187C	1	ASG187	187	Commercial	65
LN2-CT-06-2ASG187C	2	ASG187	187	Commercial	65
LN2-CT-06-3ASG187C	3	ASG187	187	Commercial	65
LN2-CT-06-1ASG273C	1	ASG273	273	Commercial	65
LN2-CT-06-2ASG273C	2	ASG273	273	Commercial	65
LN2-CT-06-3ASG273C	3	ASG273	273	Commercial	65
LN2-CT-06-1CBG256C	1	CBG256	256	Commercial	65

Part Number	Speed	Package	Pins	Grade	System Logic Cells (k)
LN2-CT-06-2CBG256C	2	CBG256	256	Commercial	65
LN2-CT-06-3CBG256C	3	CBG256	256	Commercial	65
LN2-CT-06-1CBG484C	1	CBG484	484	Commercial	65
LN2-CT-06-2CBG484C	2	CBG484	484	Commercial	65
LN2-CT-06-3CBG484C	3	CBG484	484	Commercial	65

4.2.2. Industrial

Table 4.2. Industrial Part Numbers

Part Number	Speed	Package	Pins	Grade	System Logic Cells (k)
LN2-CT-20E-1ASG410I	1	ASG410	410	Industrial	220
LN2-CT-20E-2ASG410I	2	ASG410	410	Industrial	220
LN2-CT-20E-3ASG410I	3	ASG410	410	Industrial	220
LN2-CT-20-1ASG410I	1	ASG410	410	Industrial	220
LN2-CT-20-2ASG410I	2	ASG410	410	Industrial	220
LN2-CT-20-3ASG410I	3	ASG410	410	Industrial	220
LN2-CT-20-1CBG484I	1	CBG484	484	Industrial	220
LN2-CT-20-2CBG484I	2	CBG484	484	Industrial	220
LN2-CT-20-3CBG484I	3	CBG484	484	Industrial	220
LN2-CT-20-1LFG672I	1	LFG672	672	Industrial	220
LN2-CT-20-2LFG672I	2	LFG672	672	Industrial	220
LN2-CT-20-3LFG672I	3	LFG672	672	Industrial	220
LN2-CT-16E-1ASG410I	1	ASG410	410	Industrial	160
LN2-CT-16E-2ASG410I	2	ASG410	410	Industrial	160
LN2-CT-16E-3ASG410I	3	ASG410	410	Industrial	160
LN2-CT-16-1ASG410I	1	ASG410	410	Industrial	160
LN2-CT-16-2ASG410I	2	ASG410	410	Industrial	160
LN2-CT-16-3ASG410I	3	ASG410	410	Industrial	160
LN2-CT-16-1CBG484I	1	CBG484	484	Industrial	160
LN2-CT-16-2CBG484I	2	CBG484	484	Industrial	160
LN2-CT-16-3CBG484I	3	CBG484	484	Industrial	160
LN2-CT-16-1LFG672I	1	LFG672	672	Industrial	160
LN2-CT-16-2LFG672I	2	LFG672	672	Industrial	160
LN2-CT-16-3LFG672I	3	LFG672	672	Industrial	160
LN2-CT-10-1ASG187I	1	ASG187	187	Industrial	100
LN2-CT-10-2ASG187I	2	ASG187	187	Industrial	100
LN2-CT-10-3ASG187I	3	ASG187	187	Industrial	100
LN2-CT-10-1ASG273I	1	ASG273	273	Industrial	100
LN2-CT-10-2ASG273I	2	ASG273	273	Industrial	100
LN2-CT-10-3ASG273I	3	ASG273	273	Industrial	100
LN2-CT-10-1CBG256I	1	CBG256	256	Industrial	100
LN2-CT-10-2CBG256I	2	CBG256	256	Industrial	100
LN2-CT-10-3CBG256I	3	CBG256	256	Industrial	100
LN2-CT-10-1CBG484I	1	CBG484	484	Industrial	100
LN2-CT-10-2CBG484I	2	CBG484	484	Industrial	100
LN2-CT-10-3CBG484I	3	CBG484	484	Industrial	100
LN2-CT-06-1ASG187I	1	ASG187	187	Industrial	65
LN2-CT-06-2ASG187I	2	ASG187	187	Industrial	65
LN2-CT-06-3ASG187I	3	ASG187	187	Industrial	65
LN2-CT-06-1ASG273I	1	ASG273	273	Industrial	65
LN2-CT-06-2ASG273I	2	ASG273	273	Industrial	65
LN2-CT-06-3ASG273I	3	ASG273	273	Industrial	65
LN2-CT-06-1CBG256I	1	CBG256	256	Industrial	65
LN2-CT-06-2CBG256I	2	CBG256	256	Industrial	65
LN2-CT-06-3CBG256I	3	CBG256	256	Industrial	65

Part Number	Speed	Package	Pins	Grade	System Logic Cells (k)
LN2-CT-06-1CBG484I	1	CBG484	484	Industrial	65
LN2-CT-06-2CBG484I	2	CBG484	484	Industrial	65
LN2-CT-06-3CBG484I	3	CBG484	484	Industrial	65

References

- Certus-N2 web page

A variety of technical notes for the Lattice Nexus 2 platform are available.

- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Lattice Nexus 2 Embedded Memory User Guide (FPGA-TN-02366)
- Lattice Nexus 2 Hardware Checklist (FPGA-TN-02317)
- Lattice Nexus 2 High-Speed I/O and External Memory Interface (FPGA-TN-02372)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- Lattice Nexus 2 sysCLOCK PLL Design and User Guide (FPGA-TN-02364)
- Lattice Nexus 2 sysDSP User Guide (FPGA-TN-02362)
- Lattice Nexus 2 sysCONFIG User Guide (FPGA-TN-02370)
- Lattice Nexus 2 sysI/O User Guide (FPGA-TN-02365)
- Lattice Nexus 2 SED/SEC User Guide (FPGA-TN-02380)
- Lattice Nexus 2 Power User Guide (FPGA-TN-02381)
- sub-LVDS Signaling Using Lattice Devices (FPGA-TN-02028)
- Thermal Management (FPGA-TN-02044)
- Using TraceID (FPGA-TN-02084)

For more information on Lattice Nexus 2-related IP, reference designs, and board documents, refer to the following pages:

- SGMII and Gb Ethernet PCS IP Core – Lattice Radiant Software (FPGA-IPUG-02077)
- IP and Reference Designs for Lattice Nexus 2
- Development Kits and Boards for Lattice Nexus 2

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL) – www.jedec.org
- PCI – www.pcisig.com

Other references:

- Lattice Insights for Lattice Semiconductor training courses and learning plans
- Lattice Radiant FPGA design software

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 0.71, December 2024

Section	Change Summary
All	• Updated platform and device name to *Lattice Nexus 2 and Certus-N2* and OPN name to *LN2* across the document. • Updated document to include Certus-N2 information only.

General Description	• Updated SLC from 200k to *220k* across the section.
	• Updated Table 1.1. Lattice Nexus 2 Platform Key Features to update values in the following sections: *Programmable Architecture, SERDES and Hardened Interface, and High-speed and Flexible Programmable I/O*.
	• Updated Table 1.2. Lattice Nexus 2 Families to add Certus-N2 in the column header name and added Multi-protocol SERDES row.
	• Updated the following in Table 1.3. Certus-N2 Family Selection Guide:
	  • Updated values of CT20 in SLC, LUT, Embedded Memory (Mb), and DSP.
	  • Updated packages and Total I/O values, including updating the ASG410 row to add values for CT16E and CT20E and adding footnote, and correcting FCBGA to *FCCSP* for CBG256 and CBG484.

Architecture	• Updated SLC (per clock region) from 20k to *22k* including Figure 2.1. High-level Device Floorplan (LN2-CT20 Device), Figure 2.5. High-Level View of Clock Networks and Elements (LN2-CT20 Device), and Figure 2.7. Multi-Region Clock Formation (LN2-CT20 Device). • Changed 26k to *22k* in Clocking Structure. • Updated sysMEM values to *114 to 306* in sysMEM Embedded Memory. • Updated text to *The internal DSP can also run up to 625 MHz maximum frequency on fully pipelined configuration* and *… to support the symmetric filter and complex number multiplication* in sysDSP. • Updated Figure 2.11. sysI/O Banking (LN2-CT20 Device) in Programmable I/O (PIO). • Updated text to *up to three HPIO banks* and updated note to add LN2-CT16 device support in DQS Grouping for DDR Memory. • Removed APB information in Multi-Protocol PHY (MPPHY) Integration. • Updated section name to Anti-Tamper Monitor.
Pinout Information	Updated Lattice Certus-N2 Family table to change column name to *ASG410E* and added a new ASG410 column with no data for LN2-CT20.
Ordering Information	• Updated diagram in Lattice Nexus 2 Part Number Description to update Family Code to Certus-N2, SLC value to 220k, FCCSP in CBG484, and added *E* feature. • Updated Ordering Part Numbers tables to change SLC from 200 to *220* and add rows for LN2-CT20E and LN2-CT16E.
References	Updated document references to add links.

Revision 0.70, August 2024

Section	Change Summary
All	Advance release.

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