FFT Compiler Resource Utilization

IP Configuration for Avant Family

LAV-AT-500E-3LFG1156I

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs	EBR	DSPs[2]
Default	251.762	830	638	3	4
Architecture: High Performance, Others = Default	-	-	-	-	-
Architecture: High Performance, Multiplier Type: LUT-based	156.323	1674	4021	1	0
FFT Mode: Dynamic Through Port, Others = Default	251.762	835	639	3	4
Input Data Width: 24, Twiddle Factor Width: 24, Others = Default	185.632	1921	1156	3	16
Multiplier Type: LUT-based, Memory Type: Distributed Memory, Others = Default	178.508	1296	2163	0	0

Note: Fmax is generated when the FPGA design only contains FFT Compiler IP Core, and the target frequency is 100MHz. These values may be reduced when user logic is added to the FPGA design

LAV-AT-500E-1LFG1156I

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs	EBR	DSPs[2]
Default	225.887	830	638	3	4
Architecture: High Performance, Others = Default	-	-	-	-	-
Architecture: High Performance, Multiplier Type: LUT-based	145.815	1674	4021	1	0
FFT Mode: Dynamic Through Port, Others = Default	237.304	835	639	3	4
Input Data Width: 24, Twiddle Factor Width: 24, Others = Default	162.655	1921	1156	3	16
Multiplier Type: LUT-based, Memory Type: Distributed Memory, Others = Default	165.673	1296	2163	0	0

Note: Fmax is generated when the FPGA design only contains FFT Compiler IP Core, and the target frequency is 100MHz. These values may be reduced when user logic is added to the FPGA design

FFT Compiler Resource Utilization

IP Configuration for Nexus Family

LFMXO5-25-9BBG400I

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs	EBR	DSPs[2]
Default	200	999	673	3	4
Architecture: High Performance, Others = Default	200	1128	1527	1	8
Architecture: High Performance, Multiplier Type: LUT-based	131.631	2338	4343	1	0
FFT Mode: Dynamic Through Port, Others = Default	200	1004	674	3	4
Input Data Width: 24, Twiddle Factor Width: 24, Others = Default	200	1483	973	6	16
Multiplier Type: LUT-based, Memory Type: Distributed Memory, Others = Default	140.154	1280	2364	0	0

Notes:

1. Fmax is generated when the FPGA design only contains FFT Compiler IP Core, and the target frequency is 100MHz. These values may be reduced when user logic is added to the FPGA design.
2. Number of Multipliers

LFMXO5-25-7BBG400I

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs	EBR	DSPs[2]
Default	164.772	999	673	3	4
Architecture: High Performance, Others = Default	167.757	1128	1527	1	8
Architecture: High Performance, Multiplier Type: LUT-based	84.402	2110	4349	1	0
FFT Mode: Dynamic Through Port, Others = Default	171.527	1004	674	3	4
Input Data Width: 24, Twiddle Factor Width: 24, Others = Default	162.153	1483	973	6	16
Multiplier Type: LUT-based, Memory Type: Distributed Memory, Others = Default	85.121	1280	2364	0	0

Notes:

1. Fmax is generated when the FPGA design only contains FFT Compiler IP Core, and the target frequency is 100MHz. These values may be reduced when user logic is added to the FPGA design.
2. Number of Multipliers

FFT Compiler Resource Utilization

ECP5[1]

# Points	Operating mode	SLICEs	LUTs	Registers	sysMEM EBRs	sysDSP Blocks	f^{MAX}(MHz)
64	Low Resource	583	773	775	3	1	260
64	High Performance	1043	1671	1218	1	2	279
256	Low Resource	605	807	803	3	1	249
256	High Performance	1471	2335	1679	3	3	286
1024	Low Resource	648	882	833	3	1	244
1024	High Performance	1837	2917	2098	6	4	271

1. Performance and utilization data are generated targeting an LFE5UM-85F-8BG756C device using Lattice Diamond 3.10 and Synplify Pro M-2017.03L-SP1-1. Performance may vary when using a different software version or targeting a different device density or speed grade within the ECP5 family.

LatticeECP3[1]

# Points	Operating mode	SLICEs	LUTs	Registers	sysMEM EBRs	sysDSP Blocks	f^{MAX}(MHz)
64	Low Resource	493	668	727	3	2	285
64	High Performance	733	1433	1174	1	2	243
256	Low Resource	575	821	783	3	2	255
256	High Performance	1065	2074	1636	3	3	266
1024	Low Resource	653	964	820	3	2	254
1024	High Performance	1329	2602	2056	6	4	261
8192	Low Resource	722	1089	870	18	2	258
8192	High Performance	1957	3843	2762	21	6	229

1. Performance and utilization data are generated targeting a LFE3-95E-8FN672CES device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.

FFT Compiler Resource Utilization

LatticeECP2M[1]

# Points	Operating mode	SLICEs	LUTs	Registers	sysMEM EBRs	sysDSP Blocks	f^{MAX}(MHz)
64	Low Resource	534	681	730	3	1	286
64	High Performance	989	1437	1174	1	2	243
256	Low Resource	616	830	789	3	1	292
256	High Performance	1419	2070	1636	3	3	266
1024	Low Resource	718	991	839	3	1	273
1024	High Performance	1782	2618	2056	6	4	261
8192	Low Resource	787	1123	897	18	1	234
8192	High Performance	2518	3867	2762	21	6	229

1. Performance and utilization data are generated targeting a LFE2M-35E-7F672C device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2M family.

LatticeECP2[1]

# Points	Operating mode	SLICEs	LUTs	Registers	sysMEM EBRs	sysDSP Blocks	f^{MAX}(MHz)
64	Low Resource	499	608	695	3	1	283
64	High Performance	723	1435	1174	1	2	283
256	Low Resource	578	745	755	3	1	250
256	High Performance	1049	2078	1636	3	3	250
1024	Low Resource	666	894	804	3	1	258
1024	High Performance	1324	2626	2056	6	4	258
8192	Low Resource	787	1123	897	18	1	240
8192	High Performance	1952	3880	2762	21	6	240

1. Performance and utilization data are generated targeting a LFE2-50-7F672C device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2 family.

FFT Compiler Resource Utilization

LatticeECP/EC[1]

# Points	Operating mode	SLICEs	LUTs	Registers	sysMEM EBRs	sysDSP Blocks	f^{MAX}(MHz)
64	Low Resource	488	588	705	3	1	213
64	High Performance	998	1444	1174	1	2	208
256	Low Resource	575	732	772	3	1	212
256	High Performance	1424	2060	1636	3	3	200
1024	Low Resource	702	957	861	5	1	192
1024	High Performance	1781	2589	2056	7	4	182
8192	Low Resource	769	1055	913	36	1	189
8192	High Performance	2579	3950	2762	38	6	179

1. Performance and utilization data are generated targeting a LFECP33E-5F672C device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP family.

LatticeXP2[1]

# Points	Operating mode	SLICEs	LUTs	Registers	sysMEM EBRs	sysDSP Blocks	f^{MAX}(MHz)
64	Low Resource	534	681	730	3	1	261
64	High Performance	989	1437	1174	1	2	243
256	Low Resource	616	830	789	3	1	226
256	High Performance	1419	2070	1636	3	3	266
1024	Low Resource	718	991	839	3	1	237
1024	High Performance	1782	2618	2056	6	4	261

1. Performance and utilization data are generated targeting a LFXP2-17E-7F484C device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeXP2 family.