

## Introduction

Motorola's MPC8260 is a chip that contains a 64-bit PowerPC microprocessor and a versatile communications processor module (CPM). The 8260 is used in a wide array of applications, especially those in the communications and networking market. Examples include remote access servers, regional office routers, cellular base stations, and SONET transmission controllers.

This reference design is intended to show how the Lattice Generic Digital Crosspoint Switch (ispGDx<sup>®</sup>) can be used to interface the MPC8260 with an external master and a number of slaves including SDRAM, FLASH and a CPLD. Note that this document is meant to be a reference design, and the code will vary greatly depending on the type and size of memory modules used in application-specific designs. The purpose of this design is to illustrate concepts that users can implement when building their own designs.

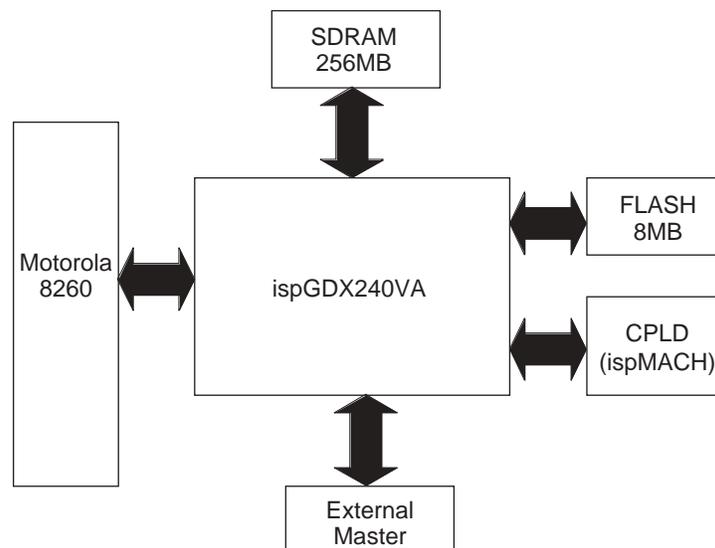
## Applicable Documents

- Lattice ispGDx240VA Data Sheet
- Motorola MPC8260 PowerQUICC II User's Manual
- Lattice Application Note #AN2083, *Using Lattice GDx160V with the Motorola MPC860 to Provide a Generic Communications Processor Solution*
- AMD Application Note #23710, *Understanding Burst Mode Flash Memory Devices*
- AMD Application Note# 23470, *Utilizing the Burst Mode Flash in a Motorola MPC8555 System*

## Overview

The MPC8260's memory controller contains an SDRAM machine that provides a convenient interface to SDRAM slaves, including support for muxing that individually loads the row and column addresses of the SDRAM. The 8260 also provides burst address lines, a 64-bit data bus, a 32-bit address bus and a GPCM (General Purpose Chip Select Machine). The ispGDx allows any input to any (or multiple) output signal routing and is ideal for applications of this nature where many slaves will try to read and write to the data bus of the 8260 and only one address bus is used for the SDRAM, FLASH and CPLD. The ispGDx has the option of matching bus voltages as needed as well, using an attribute in the software coding that allows the hardware to handle both 2.5 and 3.3V I/Os.

**Figure 1. General Block Diagram**



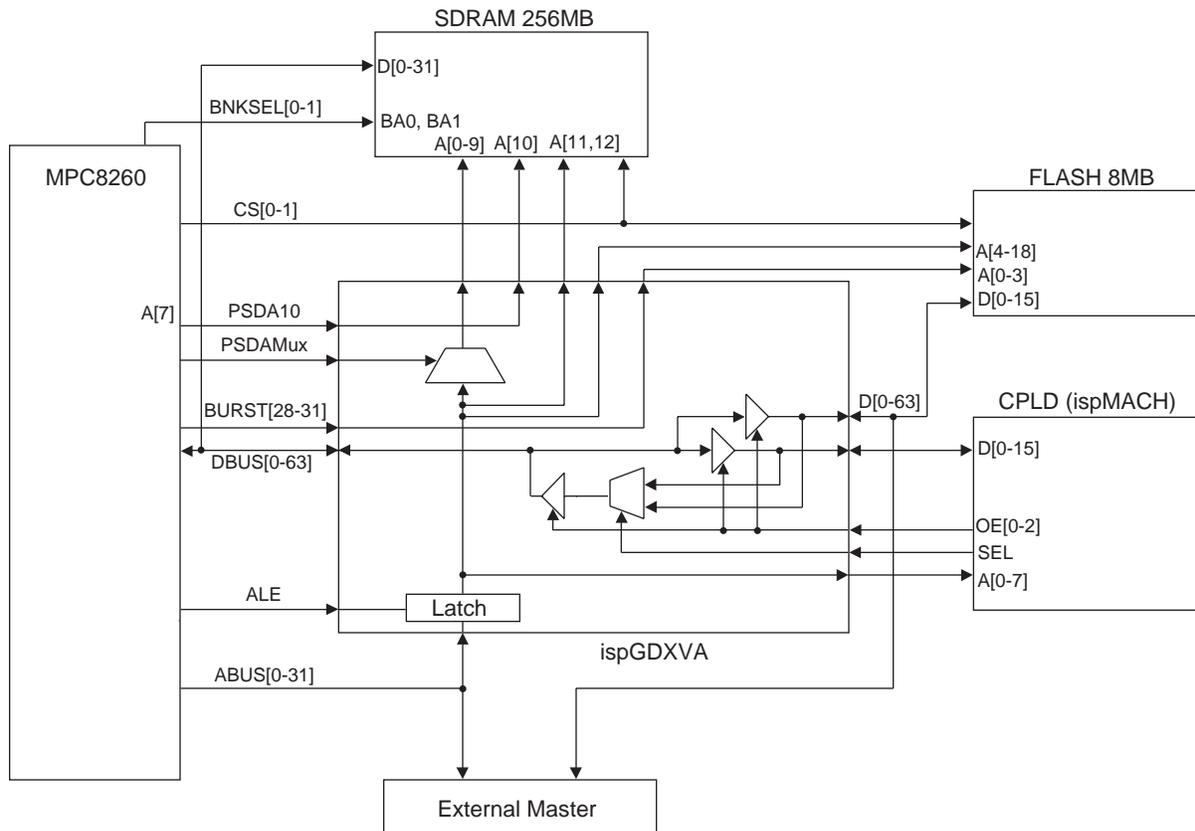
The GDx takes care of Big Endian to Little Endian issues that arise by allowing any input of any bus to appear as any output of any other bus, which makes swapping MSB and LSB easy. Using the GDx, this interface greatly reduces board space (since the ispGDx replaces many otherwise needed devices), provides reconfiguration at any time (through the IEEE 1149 port), and greatly reduces the number of traces required on the PCB. The CPLD in this design is responsible for selecting which memory module is allowed to write to the 8260 during “reads” using a MUX within the ispGDx, and which memory module’s data bus receives data during “writes” using the bus output enable functionality of the ispGDx.

Due to the robustness of both the ispGDx and the 8260, all of the 8260’s data and address lines are placed as inputs to the ispGDx even though this application does not require all of them. The source code includes these unused portions of the data and address buses since the number of bits being used on this bus varies depending on the type and size of memory selected for each unique application. Notice that the MPC\_ABUS\_UNUSED and MPC\_DBUS\_UNUSED are subsets of MPC\_ABUS and MPC\_DBUS in the source code.

### Functional Description

Figure 2 shows a more detailed block diagram of this application and includes the internal logic and cross-connections that the ispGDx is performing in the design. Table 1 displays the signal list used in the design.

**Figure 2. Detailed Block Diagram**



**Table 1. Signal List**

Signal Name	Signal Direction	Name-Definition
ALE	Input	Address Latch Enable
CPLD_ABUS	Output	CPLD Address Bus
CPLD_DBUS	Bidi	CPLD Data Bus
DBUS_OE	Input	Data Bus Output Enable - allows the slaves to send data to the 8260
FLASH_ABUS	Output	FLASH Address Bus
FLASH_DBUS	Bidi	FLASH Data Bus
MPC_ABUS	Input	8260 (microprocessor) Address Bus (only bits that are used in this application)
MPC_ABUS_UNUSED	Input	8260 Address Bus (bits that are unused in this application)
MPC_BNKSELBUS	Input	8260 Bank Select Bus - used to select SDRAM address banks
MPC_DBUS	Bidi	8260 Data Bus (only bits that are used in this application)
MPC_DBUS_UNUSED	Bidi	8260 Data Bus (bits that are unused in this application)
PSDA10	Input	60x Bus SDRAM A10 - Special pre-charge bit for SDRAM
PSDAMUX	Input	60x Bus SDRAM Address MUX - selects row or column address for SDRAM
SDRAM_ABUS	Output	SDRAM Address Bus
SDRAM_BNKSELBUS	Output	SDRAM Bank Select Bus
SDRAM_DBUS	Output	SDRAM Data Bus
SLAVE_SEL	Input	Slave Select - select line for MPC_DBUS MUX that assigns the 8260 data bus to one of the slaves

## Addressing

The master controls the address bus, ABUS. This bus is connected to the 8260 and is latched upon entering the ispGDx (using the 8260's ALE signal, see Section 10.2.11 of the 8260 User's Manual) to provide the memory modules with sufficient data tenure to read the address. After being latched, the address bus is then routed to the memory modules, with the required portions of the address bus appearing as outputs at the respective slaves. Since varying types and sizes of memory require different numbers of address bits, the ispGDx allows the FLASH, CPLD and SDRAM to only access those portions of the address bus that are specifically needed by the modules.

The master controls the address being written to through the address bus, MPC\_ABUS. This bus is visible not only to the memory modules and CPLD but also to the 8260. The 8260 is capable of supporting up to a 32-bit address bus in 60x mode, but this application does not require the use of all 32 because of the size of memory modules being used (Figure 4). The exchange of data and the address bank selection between the 8260 and the SDRAM is done externally to the ispGDx, utilizing the memory module's SDRAM machine, which is described in Chapter 10 of the 8260 User's Manual.

## SDRAM Address Configuration

The SDRAM in this application has 10 columns and 12 rows. By utilizing the 8260's PSDAMux signal as the select line for the SDRAM's address MUX, the ispGDx provides the correct address to the SDRAM, either row or column, at the correct times. Notice in Figure 2 that since the number of rows exceeds the number of columns for this SDRAM, the remaining two bits of the address bus bypass the MUX.

The ispGDx also takes into account the bit positions of the 8260's address bus and their corresponding positions in the memory's address bus. For example, in Figure 3, bit 5 of the 8260's address bus is the 12th row address of the SDRAM (one of the bypassed row addresses) and bits 17 and 29 of the 8260 address bus function as address bit zero of the SDRAM (row or column, depending on PSDAMux's value). As is standard with SDRAM, the 10th address bit is a special pre-charge bit. This bit is always address 10 for the SDRAM. Figure 3 shows the row portion of the address bus going from A0 on bit 17 of the 8260 address bus to A12 on bit 5. The 8260's architecture

provides for the special A10 anomaly with the output pin PSDA10, which is actually bit 7 of the 8260's address as can be seen in Figure 2.

Since the SDRAM in this application has four banks, the bank selection is done using two of the 8260's bank select pins (00, 01, 10, or 11 depending on the bank desired). Since page-mode gives better performance over bank-mode for bank interleaving, the bank selects utilize the lower bits of the address bus. The 8260's bank select capabilities are discussed in Section 10.4 of the 8260 User's Manual.

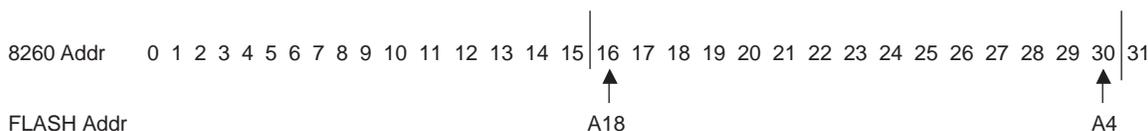
**Figure 3. SDRAM Address Designations**



### FLASH Address Configuration

The memory addressing for the burstable FLASH memory is done utilizing the 8260's burst address outputs (described in section 10.9.5 of the 8260 User's Manual), in addition to the required address bits from the 8260 address bus. Figure 4 shows address bits 4-18 of the FLASH being taken from bits 16-30 of the 8260 address bus. Bits 0-3 (the burst addresses) are routed directly through the GDX from the 8260 to the FLASH, as shown in Figure 2.

**Figure 4. FLASH Address Designations**



The external master obtains access to data using the FLASH data bus. This data bus actually has all 64 data bits on it even though the FLASH itself is only using 16 of those bits. The ispGDX handles the output enable for the data bus, as can be seen by the OE buffers in Figure 2, which are controlled via the CPLD. This ensures that the processor will be writing to the correct memory module or to the CPLD at the appropriate times.

### CPLD Control

The CPLD provides both OE signals for the bi-directional data buses, to make sure that data flow is in only one direction at a time. The CPLD also provides a select line for a MUX within the ispGDX that selects which of the slaves has access to the data bus going to the 8260 during "reads". Typically, the control logic will fit into a 32- to 64-macrocell device. The recommended CPLD device is the ispMACH 4A3-32/32 or the ispMACH 4A3-64/32.

### Conclusion

In conjunction with the applicable documents listed, this reference design provides the user with a template for using a Lattice ispGDX to interface the Motorola 8260 with SDRAM, FLASH and a Lattice ispMACH CPLD. The design also provides a template for interfacing with other slaves such as DRAM (which utilizes the same type of row/column muxing scheme as the SDRAM in this design) or SRAM (similar to the FLASH interface, without the burst lines). This design, as implemented, operates at a maximum frequency of 92.6MHz calculated from the timing report using the inverse of the sum of  $t_{CO}$  and  $t_{SU}$ .

### Technical Support Assistance

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