# CSI-2/DSI D-PHY Receiver Resource Utilization

## IP Configuration for Nexus Family

| Lane (Gear) | RX Interface Type | IP Type | Bit Rate (Lane) | Parser | AXI Bus | LMMI Bus | Registers | LUT2 | EBR | High Speed I/O resources |
|---|---|---|---|---|---|---|---|---|---|---|
| 4(8) | CSI-2 | Hard D-PHY[4] | 1000 Mbps | EN | EN | DIS | 629 | 699 | 2 | 1 x Hard D-PHY |
| 4(8) | CSI-2 | Soft D-PHY | 1000 Mbps | EN | EN | DIS | 706 | 1212 | 2 | 4 x IDDRX4,<br>1 x ECLKDIV,<br>1 x ECLKSYNC |
| 4(16)[3] | CSI-2 | Hard D-PHY[4] | 2500 Mbps | EN | EN | DIS | 852 | 991 | 4 | 1 x Hard D-PHY |
| 4(8)[3] | CSI-2 | Soft D-PHY | 1500 Mbps | EN | EN | DIS | 706 | 1270 | 2 | 4 x IDDRX4,<br>1 x ECLKDIV,<br>1 x ECLKSYNC |
| 4(16) | DSI | Hard D-PHY[4] | 2000 Mbps | EN | EN | En | 1006 | 1520 | 4 | 1 x Hard D-PHY |
| 4(16) | DSI | Hard D-PHY[5] | 2000 Mbps | EN | EN | EN | 1006 | 1520 | 4 | 1 x Hard D-PHY |
| 4(8) | DSI | Hard D-PHY[4] | 1200 Mbps | EN | EN | DIS | 682 | 843 | 2 | 1 x Hard D-PHY |
| 2(8) | DSI | Hard D-PHY[4] | 800 Mbps | EN | DIS | DIS | 448 | 566 | 2 | 1 x Hard D-PHY |
| 4(16)[3] | CSI-2 | Hard D-PHY[4] | 2500 Mbps | EN | EN | EN | 870 | 1041 | 4 | 1 x Hard D-PHY |
| 4(8)[3] | CSI-2 | Hard D-PHY[4] | 1500 Mbps | EN | EN | EN | 585 | 747 | 2 | 1 x Hard D-PHY |
| 2(8) | CSI-2 | Hard D-PHY[4] | 800 Mbps | EN | DIS | DIS | 447 | 554 | 2 | 1 x Hard D-PHY |

**Notes:**

1. All other settings are default.
2. The distributed RAM utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among logic, distributed RAM, and ripple logic.
3. Data Settle settings were changed in these configurations to match their target Bit Rate per Lane.
4. Hard D-PHY – CIL Bypassed
5. Hard D-PHY – CIL Enabled

For more information regarding a specific configuration, the user can generate the IP, run synthesis, and MAP, and check the MAP reports or resource utilization.

## IP Configuration for Nexus Family

| IP User-Configurable Parameters | Registers | Slices | LUTs | sysMEM EBRs | Programmable I/O | MIPI D-PHY | Target fMAX (MHz)[2] | Actual fMAX (MHz)[2] |
|---|---|---|---|---|---|---|---|---|
| **CSI-2 Hard D-PHY Gear 16** | | | | | | | | |
| 4-lane<br>Non-continuous clock<br>Packet parser disabled<br>Word aligner disabled<br>Lane aligner disabled | 241 | 190 | 250 | 4 | 0 | 1 | 93.75 | 185.11 |
| 2-lane Non-continuous clock Packet parser enabled Word aligner enabled Lane aligner LUT FIFO | 574 | 812 | 1183 | 2 | 0 | 1 | 93.75 | 230.52 |
| 1-lane<br>Non-continuous clock<br>Packet parser disabled<br>Word aligner disabled<br>Lane aligner disabled | 145 | 140 | 184 | 1 | 0 | 1 | 93.75 | 179.86 |
| 4-lane<br>Continuous clock<br>Packet parser enabled<br>Word aligner enabled Lane aligner EBR FIFO | 708 | 1338 | 2023 | 8 | 0 | 1 | 93.75 | 184.98 |
| 2-lane<br>Continuous clock<br>Packet parser disabled<br>Word aligner disabled | 168 | 148 | 191 | 2 | 0 | 1 | 93.75 | 207.9 |
| 1-lane<br>Continuous clock<br>Packet parser enabled<br>Word aligner enabled<br>Lane aligner disabled | 312 | 408 | 594 | 1 | 0 | 1 | 93.75 | 193.94 |
| **CSI-2 Hard D-PHY Gear 8** | | | | | | | | |
| 4-lane<br>Non-continuous clock Packet parser enabled Word aligner enabled Lane aligner EBR FIFO | 563 | 866 | 1256 | 6 | 0 | 1 | 150 | 207.64 |
| 2-lane<br>Non-continuous clock<br>Packet parser enabled<br>Word aligner disabled Lane aligner disabled | 300 | 286 | 403 | 1 | 0 | 1 | 150 | 225.53 |
| 1-lane<br>Non-continuous clock<br>Packet parser enabled<br>Word aligner enabled Lane aligner disabled | 281 | 331 | 461 | 1 | 0 | 1 | 150 | 193.01 |

## IP Configuration for Nexus Family

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|---|---|---|---|---|---|---|---|---|
| 4-lane Continuous clock Packet parser enabled Word aligner enabled Lane aligner EBR FIFO | 554 | 857 | 1245 | 6 | 0 | 1 | 150 | - |
| 2-lane Continuous clock Packet parser enabled Word aligner enabled Lane aligner EBR FIFO | 354 | 489 | 708 | 3 | 0 | 1 | 150 | 200.92 |
| 1-lane Continuous clock Packet parser disabled Word aligner disabled Lane aligner disabled | 120 | 118 | 164 | 1 | 0 | 1 | 150 | 208.64 |
| **CSI-2 Soft D-PHY Gear 16** | | | | | | | | |
| 4-lane Non-continuous clock Packet parser enabled Word aligner enabled Lane aligner LUT FIFO | 511 | 1079 | 1573 | 8 | 10 | 0 | 75 | 164.17 |
| 2-lane Non-continuous clock Packet parser enabled Word aligner enabled Lane aligner EBR FIFO | 470 | 668 | 1043 | 2 | 6 | 0 | 75 | 200.8 |
| 1-lane Non-continuous clock Packet parser enabled Word aligner enabled Lane aligner disabled | 262 | 361 | 547 | 1 | 4 | 0 | 75 | 211 |
| 4-lane Continuous clock Packet parser enabled Word aligner enabled Lane aligner EBR FIFO | 503 | 1073 | 1566 | 8 | 10 | 0 | 75 | 175.87 |
| 2-lane Continuous clock Packet parser disabled Word aligner enabled Lane aligner EBR FIFO | 225 | 450 | 671 | 4 | 6 | 0 | 75 | 218.82 |
| 1-lane Continuous clock Packet parser enabled Word aligner enabled Lane aligner disabled | 105 | 123 | 175 | 1 | 4 | 0 | 75 | 245.28 |
| **CSI-2 Soft D-PHY Gear 8** | | | | | | | | |
| 4-lane Non-continuous clock Packet parser enabled Word aligner enabled Lane aligner EBR FIFO | 523 | 783 | 1166 | 2 | 10 | 0 | 150 | 218.2 |
| 2-lane Non-continuous clock Packet parser enabled Word aligner enabled Lane aligner LUT FIFO | 304 | 442 | 661 | 3 | 6 | 0 | 150 | 232.07 |

## IP Configuration for Nexus Family

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|---|---|---|---|---|---|---|---|---|
| 1-lane<br>Non-continuous clock<br>Packet parser enabled<br>Word aligner enabled<br>Lane aligner disabled | 247 | 297 | 429 | 1 | 4 | 0 | 150 | 216.66 |
| 4-lane<br>Continuous clock<br>Packet parser enabled<br>Word aligner enabled<br>Lane aligner EBR FIFO | 450 | 736 | 1109 | 6 | 10 | 0 | 150 | 202.72 |
| 2-lane<br>Continuous clock<br>Packet parser enabled<br>Word aligner enabled<br>Lane aligner EBR FIFO | 223 | 346 | 496 | 2 | 6 | 0 | 150 | 258.6 |
| 1-lane<br>Continuous clock<br>Packet parser disabled<br>Word aligner enabled<br>Lane aligner disabled | 238 | 290 | 420 | 1 | 4 | 0 | 150 | 235.18 |
| **DSI Hard D-PHY Gear 16** | | | | | | | | |
| 4-lane<br>Non-continuous clock<br>Packet parser enabled Word aligner enabled Lane aligner EBR FIFO | 769 | 1505 | 2265 | 8 | 0 | 1 | 93.75 | 197.71 |
| 2-lane<br>Non-continuous clock<br>Packet parser enabled Word aligner enabled Lane aligner EBR FIFO | 517 | 779 | 1166 | 4 | 0 | 1 | 93.75 | 169.32 |
| 1-lane<br>Non-continuous clock<br>Packet parser enabled<br>Word aligner enabled Lane aligner disabled | 322 | 426 | 622 | 1 | 0 | 1 | 93.75 | 200.6 |
| 4-lane<br>Continuous clock<br>Packet parser enabled<br>Word aligner enabled<br>Lane aligner EBR FIFO | 760 | 1496 | 2254 | 8 | 0 | 1 | 93.75 | 187.62 |
| 2-lane<br>Continuous clock<br>Packet parser enabled<br>Word aligner enabled<br>Lane aligner EBR FIFO | 508 | 770 | 1155 | 4 | 0 | 1 | 93.75 | 200.2 |
| 1-lane<br>Continuous clock<br>Packet parser enabled<br>Word aligner enabled<br>Lane aligner disabled | 313 | 417 | 611 | 1 | 0 | 1 | 93.75 | 174.87 |
| **DSI Hard D-PHY Gear 8** | | | | | | | | |
| 4-lane<br>Non-continuous clock<br>Packet parser enabled<br>Word aligner enabled Lane aligner EBR FIFO | 571 | 874 | 1286 | 6 | 0 | 1 | 150 | 231.91 |

## IP Configuration for Nexus Family

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|---|---|---|---|---|---|---|---|---|
| 2-lane Non-continuous clock Packet parser enabled Word aligner disabled Lane aligner disabled | 301 | 290 | 414 | 1 | 0 | 1 | 150 | 225.38 |
| 1-lane Non-continuous clock Packet parser enabled Word aligner enabled Lane aligner disabled | 279 | 326 | 444 | 1 | 0 | 1 | 150 | 249.63 |
| 4-lane Continuous clock Packet parser enabled Word aligner enabled Lane aligner EBR FIFO | 526 | 865 | 1275 | 6 | 0 | 1 | 150 | 245.22 |
| 2-lane Continuous clock Packet parser enabled Word aligner enabled Lane aligner EBR FIFO | 355 | 493 | 719 | 3 | 0 | 1 | 150 | 224.72 |
| **DSI Hard D-PHY Gear 16** | | | | | | | | |
| 4-lane Non-continuous clock Packet parser enabled Word aligner enabled Lane aligner LUT FIFO | 687 | 1245 | 1877 | 4 | 10 | 0 | 75 | 211.33 |
| 2-lane Non-continuous clock Packet parser enabled Word aligner enabled Lane aligner EBR FIFO | 411 | 654 | 1025 | 4 | 6 | 0 | 75 | 243.6 |
| 1-lane Non-continuous clock Packet parser enabled Word aligner enabled Lane aligner disabled | 261 | 370 | 564 | 1 | 4 | 0 | 75 | 205.8 |
| 4-lane Continuous clock Packet parser enabled Word aligner enabled Lane aligner EBR FIFO | 550 | 158 | 1772 | 8 | 10 | 0 | 75 | 182.55 |
| 2-lane Continuous clock Packet parser disabled Word aligner enabled Lane aligner EBR FIFO | 255 | 450 | 671 | 4 | 6 | 0 | 75 | 208.68 |
| 1-lane Continuous clock Packet parser enabled Word aligner enabled Lane aligner disabled | 252 | 363 | 555 | 1 | 4 | 0 | 75 | 231.8 |

## IP Configuration for Nexus Family

| DSI Soft D-PHY Gear 8 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 4-lane Non-continuous clock Packet parser disabled Word aligner enabled Lane aligner EBR FIFO | 288 | 550 | 800 | 6 | 10 | 0 | 150 | 234.03 |
| 2-lane Non-continuous clock Packet parser enabled Word aligner enabled Lane aligner LUT FIFO | 335 | 466 | 696 | 1 | 6 | 0 | 150 | 257.73 |
| 1-lane Non-continuous clock Packet parser enabled Word aligner enabled Lane aligner disabled | 254 | 293 | 416 | 1 | 4 | 0 | 150 | 246.73 |
| 4-lane Continuous clock Packet parser enabled Word aligner enabled Lane aligner EBR FIFO | 456 | 741 | 1136 | 6 | 10 | 0 | 150 | 235.57 |
| 2-lane Continuous clock Packet parser enabled Word aligner enabled Lane aligner LUT FIFO | 326 | 459 | 687 | 1 | 6 | 0 | 150 | 207.34 |
| 1-lane Continuous clock Packet parser disabled Word aligner enabled Lane aligner disabled | 116 | 152 | 214 | 1 | 4 | 0 | 150 | 243.49 |

**Notes:**

1. The performance and utilization data target an LIF-MD6000-6MG81I device with -6 speed grade using Lattice Diamond 3.9 and Lattice Synthesis Engine. Performance may vary when using a different software version or targeting a different device density or speed grade within the CrossLink family.
2. The target fMAX is the target byte clock frequency of each configuration. Actual fMAX may vary depending on the complete top-level design.