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## Acronyms in This Document

A list of acronyms used in this document.

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>AHB</td>
<td>Advance High Performance</td>
</tr>
<tr>
<td>APB</td>
<td>Advanced Peripheral Bus</td>
</tr>
<tr>
<td>API</td>
<td>Application Programming Interface</td>
</tr>
<tr>
<td>AXI</td>
<td>Advanced extensible Interface</td>
</tr>
<tr>
<td>CRC</td>
<td>Cyclic Redundancy Check</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers</td>
</tr>
<tr>
<td>IP</td>
<td>Internet Protocol</td>
</tr>
<tr>
<td>MAC</td>
<td>Media Access Controller</td>
</tr>
<tr>
<td>SDK</td>
<td>Software Development Kit</td>
</tr>
<tr>
<td>TSEMAC</td>
<td>Tri-Speed Ethernet Media Access Controller</td>
</tr>
</tbody>
</table>
1. Introduction
Tri-Speed Ethernet Media Access Controller (TSEMAC) IP core is a complex core containing all necessary logic and interfacing and clocking infrastructures necessary to integrate an external industry-standard Ethernet PHY with an internal processor efficiently with minimal overhead.

The TSEMAC IP core supports the ability to transmit and receive data between standard interfaces such as APB, AHB-Lite or AXI4-lite, and an Ethernet network. The main function of the TSEMAC IP is to ensure that the Media Access rules specified in the 802.3 IEEE standard are met while transmitting a frame of data over Ethernet. On the receiving side, the TSEMAC extracts different components of a frame and transfers them to higher applications through the AXI4-stream interface.

Refer to the Tri-Speed Ethernet MAC IP Core – Lattice Radiant Software (FPGA-IPUG-02084) user guide for more details about the IP core.

1.1. Purpose
TSEMAC and its SDK is a set of application programming interfaces (APIs) that provide access to specific Lattice hardware and software capabilities. This document is intended to act as a reference guide for developers by providing details of the C language driver APIs and function call flows.

1.2. Audience
The intended audience for this document includes embedded system designers and embedded software developers using Lattice MachXO2™, MachXO3D™, MachXO3L™, MachXO3LF™, CrossLink™-NX, Certus™-NX, CertusPro™-NX, Mach™-NX, MachXO5™-NX, and Lattice Avant™ devices. The technical guide assumes readers have expertise in embedded systems and FPGA technologies.

1.3. Driver Versioning

1.3.1. Driver Version
Driver version: 1.0.0

1.3.2. IP Version
IP version: 1.4.2

1.4. Driver and IP Compatibility

<table>
<thead>
<tr>
<th>Driver version</th>
<th>IP version</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSEMAC</td>
<td>1.4.2</td>
</tr>
<tr>
<td>RISC-V-RX</td>
<td>2.2.0</td>
</tr>
<tr>
<td>PLL</td>
<td>1.7.0</td>
</tr>
<tr>
<td>OSC</td>
<td>1.4.0</td>
</tr>
<tr>
<td>APB Interconnect</td>
<td>1.2.0</td>
</tr>
<tr>
<td>Memory</td>
<td>2.0.0</td>
</tr>
<tr>
<td>AXI4 Interconnect</td>
<td>1.2.0</td>
</tr>
<tr>
<td>AXI4 to APB Bridge</td>
<td>1.1.0</td>
</tr>
<tr>
<td>GPIO</td>
<td>1.6.1</td>
</tr>
<tr>
<td>UART</td>
<td>1.3.0</td>
</tr>
</tbody>
</table>
2. API Description

2.1. Ethernet_init()
This API initializes the TSEMAC IP with a speed of 10/100/1000 Mbps and configures Tx MAC and Rx MAC to receive any frame address and multicast and broadcast frames.

```c
uint8_t ethernet_init(tsemac_handle_t *handle)
```

<table>
<thead>
<tr>
<th>In/Out</th>
<th>Parameter</th>
<th>Description</th>
<th>Returns</th>
</tr>
</thead>
<tbody>
<tr>
<td>In</td>
<td>adr</td>
<td>• Part of the tsemac_handle_t structure.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Represents the base address of TSEMACH.</td>
<td></td>
</tr>
<tr>
<td>In</td>
<td>speed_mode</td>
<td>Part of the structure used to set the speed 10/100/1000 Mbps for TSE MAC.</td>
<td></td>
</tr>
<tr>
<td>In</td>
<td>tx_rx_ctrl_var</td>
<td>• Part of the tsemac_handle_t structure.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Used for setting the control register to receive short pause frames and to receive the multicast and broadcast frames.</td>
<td></td>
</tr>
<tr>
<td>In</td>
<td>enable_tx_mac</td>
<td>Part of the tsemac_handle_t structure used for enabling the Tx MAC.</td>
<td></td>
</tr>
<tr>
<td>In</td>
<td>enable_rx_mac</td>
<td>Part of the tsemac_handle_t structure used for enabling the Rx MAC.</td>
<td></td>
</tr>
</tbody>
</table>

2.2. Ethernet_packet_handle()
This API handles the transmitting and receiving of Ethernet packet by using shared memory and data mover. The same packet is looped back by the TSEMAC IP into shared memory.

```c
void ethernet_packet_handle(tsemac_handle_t *handle,unsigned int *src_packet,unsigned int *dest_packet)
```

<table>
<thead>
<tr>
<th>In/Out</th>
<th>Parameter</th>
<th>Description</th>
<th>Returns</th>
</tr>
</thead>
<tbody>
<tr>
<td>In/Out</td>
<td>src_packet</td>
<td>• Parameter used for both input and output.</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Represents the Ethernet packet to transmit to TSEMACH.</td>
<td></td>
</tr>
<tr>
<td>In</td>
<td>dest_packet</td>
<td>• Parameter used for both input and output.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Represents the Ethernet packet received from TSEMACH.</td>
<td></td>
</tr>
</tbody>
</table>

2.3. Ethernet_set_mac_address()
This API sets the six-byte MAC address for a source or destination device for TSEMACH.

```c
unsigned char ethernet_set_mac_address(tsemac_handle_t *handle)
```

<table>
<thead>
<tr>
<th>In/Out</th>
<th>Parameter</th>
<th>Description</th>
<th>Returns</th>
</tr>
</thead>
<tbody>
<tr>
<td>In</td>
<td>adr</td>
<td>• Part of the tsemac_handle_t structure.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Represents the base address of TSEMACH.</td>
<td></td>
</tr>
<tr>
<td>In</td>
<td>mac_upper</td>
<td>Part of the tsemac_handle_t structure used to set the first four bytes of the mac address for TSEMACH.</td>
<td></td>
</tr>
<tr>
<td>In</td>
<td>mac_lower</td>
<td>Part of the tsemac_handle_t structure used to set the last two bytes of the mac address for TSEMACH.</td>
<td></td>
</tr>
</tbody>
</table>
2.4. Ethernet_get_mac_address()
This API reads the six-byte MAC address from MAC address word 0 and MAC address word 1 register of TSEMAC.

```c
unsigned char ethernet_get_mac_address(tsemac_handle_t *handle)
```

<table>
<thead>
<tr>
<th>In/Out</th>
<th>Parameter</th>
<th>Description</th>
<th>Returns</th>
</tr>
</thead>
</table>
| In     | adr         | • Part of the tsemac_handle_t structure.  
             • Represents the base address of TSEMAC. | 0: failure  
             1: success |

2.5. Ethernet_set_multicast_address()
This API sets the 8-byte multicast address for multicast frame from the 64-bit hash table. The first four bytes of the 64-bit hash table is stored into Multicast Table Word 0 register and the last four bytes of the 64-bit hash table is stored into Multicast Table Word 1 register.

```c
unsigned char ethernet_set_multicast_address(tsemac_handle_t *handle)
```

<table>
<thead>
<tr>
<th>In/Out</th>
<th>Parameter</th>
<th>Description</th>
<th>Returns</th>
</tr>
</thead>
</table>
| In     | adr                 | • Part of the tsemac_handle_t structure.      
             • Represents the base address of TSEMAC.  | 0: failure  
             1: success |
| In     | multicast_upper     | • A 4-byte variable of the tsemac_handle_t structure.  
             • Used to set the first four bytes of multicast address for TSEMAC. | |
| In     | multicast_lower     | • A 4-byte variable of the tsemac_handle_t structure.  
             • Used to set the last four bytes of multicast address for TSEMAC. | |

2.6. Ethernet_get_multicast_address()
This API reads the eight-byte multicast address from Multicast Table Word 0 and Multicast Table Word 1 register of TSEMAC.

```c
unsigned char ethernet_get_multicast_address(tsemac_handle_t *handle)
```

<table>
<thead>
<tr>
<th>In/Out</th>
<th>Parameter</th>
<th>Description</th>
<th>Returns</th>
</tr>
</thead>
</table>
| In     | adr         | • Part of the tsemac_handle_t structure.  
             • Represents the base address of TSEMAC. | 0: failure  
             1: success |

2.7. Ethernet_statistics_counter_register_read()
This API reads the statistics counter register of TSEMAC when multiple frames are transmitted or received.

```c
unsigned int ethernet_statistics_counter_register_read(tsemac_handle_t handle)
```

<table>
<thead>
<tr>
<th>In/Out</th>
<th>Parameter</th>
<th>Description</th>
<th>Returns</th>
</tr>
</thead>
</table>
| In     | adr                 | • Part of the tsemac_handle_t structure.  
             • Represents the base address of TSEMAC. | 0: failure  
             1: success |
| In     | stat_counter_reg_enum | • Part of the tsemac_handle_t structure.  
             • Represents the index position of the statistics counter register. | total_count: The count of the total frames transmitted or received after the statistics counter register is read. |
2.8. **Ethernet_tx_rx_status_reg_read()**

This API reads the transmit and receive status register of TSEMAC.

```c
unsigned int ethernet_tx_rx_status_reg_read(tsemac_handle_t *handle)
```

<table>
<thead>
<tr>
<th>In/Out</th>
<th>Parameter</th>
<th>Description</th>
<th>Returns</th>
</tr>
</thead>
</table>
| In     | adr       | • Part of the tsemac_handle_t structure.  
|        |           | • Represents the base address of TSEMAC.    |         |

2.9. **Ethernet_mode_reg_read()**

This API reads the TSEMAC mode register.

```c
unsigned int ethernet_mode_reg_read(tsemac_handle_t *handle)
```

<table>
<thead>
<tr>
<th>In/Out</th>
<th>Parameter</th>
<th>Description</th>
<th>Returns</th>
</tr>
</thead>
</table>
| In     | adr       | • Part of the tsemac_handle_t structure.  
|        |           | • Represents the base address of TSEMAC.    |         |

2.10. **Ethernet_tx_rx_control_reg_set()**

This API sets the bit for the control register.

```c
unsigned char ethernet_tx_rx_control_reg_set(tsemac_handle_t *handle, unsigned char bit_pos)
```

<table>
<thead>
<tr>
<th>In/Out</th>
<th>Parameter</th>
<th>Description</th>
<th>Returns</th>
</tr>
</thead>
</table>
| In     | adr       | • Part of the tsemac_handle_t structure.  
|        |           | • Represents the base address of TSEMAC.    |         |
| In     | bit_pos   | • Represents the bit position that the control register sets. |

2.11. **Ethernet_set_speed()**

This API sets the bit for the control register.

```c
unsigned char ethernet_set_speed(tsemac_handle_t *handle)
```

<table>
<thead>
<tr>
<th>In/Out</th>
<th>Parameter</th>
<th>Description</th>
<th>Returns</th>
</tr>
</thead>
</table>
| In     | adr       | • Part of the tsemac_handle_t structure.  
|        |           | • Represents the base address of TSEMAC.    |         |
| In     | speed_mode| • Part of the structure used to set the speed 10/100/1000 Mbps for TSE MAC. |         |
3. **Function Call Flow Diagrams**

3.1. **Ethernet_init()**

![Flow Diagram](image)

*Figure 3.1. ethernet_init()*
3.2. **Ethernet_packet_handle()**

![Diagram of Ethernet_packet_handle()]

3.3. **Ethernet_set_mac_address()**

![Diagram of Ethernet_set_mac_address()]
3.4. **Ethernet_get_mac_address()**

```
Start

Read the six-byte address from mac_addr0 and mac_addr1 register

Copy the first four bytes of MAC address into mac_upper and the last four bytes of MAC address into the mac_lower variable

End
```

*Figure 3.4. ethernet_get_mac_address()*

3.5. **Ethernet_set_multicast_address()**

```
Start

Pass eight-byte multicast address

Configure the first four bytes into multicast_table0 register

Configure the last four bytes into multicast_table1 register

End
```

*Figure 3.5. ethernet_set_multicast_address()*
3.6. **Ethernet_get_multicast_address()**

![Figure 3.6. ethernet_get_multicast_address()](image)

**Start**

- Read the eight-byte address from multicast_table0 and multicast_table1 register

- Copy the first four bytes of multicast address into multicast_upper and the last four bytes into the multicast_lower variable

**End**

3.7. **Ethernet_statistics_counter_register_read()**

![Figure 3.7. ethernet_statistics_counter_register_read()](image)

**Start**

- Pass the base address to TSEMAC

- Pass the statistics counter register index for offset

- Read the value of counter register_0 and register_1

- Return the total count after reading the register

**End**
3.8. **Ethernet_tx_rx_status_reg_read()**

Start

Pass the base address of TSEMAC

Return the Transmit and Receive status register read value

End

Figure 3.8. ethernet_tx_rx_status_reg_read()

3.9. **Ethernet_mode_reg_read()**

Start

Pass the base address of TSEMAC

Return the Mode register read value

End

Figure 3.9. ethernet_mode_reg_read()
3.10. Ethernet\_tx\_rx\_control\_reg\_set()
3.11. Ethernet_set_speed()

![Flowchart diagram showing the process of setting Ethernet speeds]

**Figure 3.11. ethernet_set_speed()**
4. API Data Structures

4.1. tsemac_reg_type_t

This structure assigns offsets for the TSEMAC register.

```c
volatile unsigned int mode_reg; //0x0000
volatile unsigned int tx_rx_ctrl;
volatile unsigned int max_packet_size;
volatile unsigned int ipg;
volatile unsigned int mac_addr0; //0x0010
volatile unsigned int mac_addr1;
volatile unsigned int tx_rx_status;
volatile unsigned int vlan_tag;
volatile unsigned int gmii_mgmt_ctrl; //0x0020
volatile unsigned int gmii_mgmt_data;
volatile unsigned int multi_cast0;
volatile unsigned int multi_cast1;
volatile unsigned int pause_opcode; //0x0030
volatile unsigned int tx_fifo_afull;
volatile unsigned int tx_fifo_aempty;
volatile unsigned int rx_fifo_afull; //0x0040
volatile unsigned int rx_fifo_aempty;
volatile unsigned int interrupt_status;
volatile unsigned int interrupt_enable; //0x0048
volatile unsigned int tx_stat_unicst_0;
volatile unsigned int tx_stat_unicst_1;
volatile unsigned int tx_stat_multcst_0;
volatile unsigned int tx_stat_multcst_1; //0x0058
volatile unsigned int tx_stat_brdcst_0;
volatile unsigned int tx_stat_brdcst_1;
volatile unsigned int tx_stat_badfcs_0;
volatile unsigned int tx_stat_badfcs_1; //0x0068
volatile unsigned int tx_stat_jumbo_0;
volatile unsigned int tx_stat_jumbo_1;
volatile unsigned int tx_stat_under_run_0;
volatile unsigned int tx_stat_under_run_1; //0x0078
volatile unsigned int tx_stat_pause_0;
volatile unsigned int tx_stat_pause_1;
volatile unsigned int tx_stat_vlan_tg_0;
volatile unsigned int tx_stat_vlan_tg_1; //0x0088
volatile unsigned int tx_stat_frm_length_0;
volatile unsigned int tx_stat_frm_length_1;
volatile unsigned int tx_stat_deferred_trans_0;
volatile unsigned int tx_stat_deferred_trans_1; //0x0098
volatile unsigned int tx_stat_excess_deferred_trans_0;
volatile unsigned int tx_stat_excess_deferred_trans_1;
volatile unsigned int tx_stat_late_col_0;
volatile unsigned int tx_stat_late_col_1; //0x00A8
volatile unsigned int tx_stat_excess_col_0;
volatile unsigned int tx_stat_excess_col_1;
volatile unsigned int tx_stat_num_early_col_0;
```
volatile unsigned int tx_stat_num_early_col_1; //0x00B8
volatile unsigned int tx_stat_shrt_frm_dis_fcs_0;
volatile unsigned int tx_stat_shrt_frm_dis_fcs_1;
volatile unsigned int tx_stat_ptp_1588_frm_0;
volatile unsigned int tx_stat_ptp_1588_frm_1; //0x00C8
volatile unsigned int tx_stat_frm_64_0;
volatile unsigned int tx_stat_frm_64_1;
volatile unsigned int tx_stat_frm_65_127_0;
volatile unsigned int tx_stat_frm_65_127_1; //0x00D8
volatile unsigned int tx_stat_frm_128_255_0;
volatile unsigned int tx_stat_frm_128_255_1;
volatile unsigned int tx_stat_frm_256_511_0;
volatile unsigned int tx_stat_frm_256_511_1; //0x00E8
volatile unsigned int tx_stat_frm_512_1023_0;
volatile unsigned int tx_stat_frm_512_1023_1;
volatile unsigned int tx_stat_frm_1024_1518_0;
volatile unsigned int tx_stat_frm_1024_1518_1; //0x00F8
volatile unsigned int tx_stat_frm_1519_2047_0;
volatile unsigned int tx_stat_frm_1519_2047_1;
volatile unsigned int tx_stat_frm_2048_4095_0;
volatile unsigned int tx_stat_frm_2048_4095_1; //0x108
volatile unsigned int tx_stat_frm_4096_9216_0;
volatile unsigned int tx_stat_frm_4096_9216_1;
volatile unsigned int tx_stat_frm_9217_16383_0;
volatile unsigned int tx_stat_frm_9217_16383_1; //0x118
volatile unsigned int rx_stat_frm_length_0;
volatile unsigned int rx_stat_frm_length_1;
volatile unsigned int rx_stat_vlan_tg_0;
volatile unsigned int rx_stat_vlan_tg_1; //0x128
volatile unsigned int rx_stat_pause_0;
volatile unsigned int rx_stat_pause_1;
volatile unsigned int rx_stat_ctrl_0;
volatile unsigned int rx_stat_ctrl_1; //0x138
volatile unsigned int rx_stat_unsp_opcode_0;
volatile unsigned int rx_stat_unsp_opcode_1;
volatile unsigned int rx_stat_dribb_nibb_0;
volatile unsigned int rx_stat_dribb_nibb_1; //0x148
volatile unsigned int rx_stat_brdcst_0;
volatile unsigned int rx_stat_brdcst_1;
volatile unsigned int rx_stat_multcst_0;
volatile unsigned int rx_stat_multcst_1; //0x158
volatile unsigned int rx_stat_unicst_0;
volatile unsigned int rx_stat_unicst_1;
volatile unsigned int rx_stat_rcvd_ok_0;
volatile unsigned int rx_stat_rcvd_ok_1; //0x168
volatile unsigned int rx_stat_length_error_0;
volatile unsigned int rx_stat_length_error_1;
volatile unsigned int rx_stat_crc_error_0;
volatile unsigned int rx_stat_crc_error_1; //0x178
volatile unsigned int rx_stat_pkt_ignore_0;
volatile unsigned int rx_stat_pkt_ignore_1;
volatile unsigned int rx_stat_previous_carrier_event_0;
volatile unsigned int rx_stat_previous_carrier_event_1; //0x188
volatile unsigned int rx_stat_ptp1588_frm_0;
volatile unsigned int rx_stat_ptp1588_frm_1;
volatile unsigned int rx_stat_ipg_viol_0;
volatile unsigned int rx_stat_ipg_viol_1; //0x198
volatile unsigned int rx_stat_shrt_frm_0;
volatile unsigned int rx_stat_shrt_frm_1;
volatile unsigned int rx_stat_lng_frm_0;
volatile unsigned int rx_stat_lng_frm_1; //0x1A8
volatile unsigned int rx_stat_frm_undersize_0;
volatile unsigned int rx_stat_frm_undersize_1;
volatile unsigned int rx_stat_frm_fragment_0;
volatile unsigned int rx_stat_frm_fragment_1; //0x1B8
volatile unsigned int rx_stat_frm_jabber_0;
volatile unsigned int rx_stat_frm_jabber_1;
volatile unsigned int rx_stat_frm_64_good_crc_0;
volatile unsigned int rx_stat_frm_64_good_crc_1; //0x1C8
volatile unsigned int rx_stat_frm_1518_good_crc_0;
volatile unsigned int rx_stat_frm_1518_good_crc_1;
volatile unsigned int rx_stat_frm_64_0;
volatile unsigned int rx_stat_frm_64_1; //0x1D8
volatile unsigned int rx_stat_frm_65_127_0;
volatile unsigned int rx_stat_frm_65_127_1;
volatile unsigned int rx_stat_frm_128_255_0;
volatile unsigned int rx_stat_frm_128_255_1; //0x1E8
volatile unsigned int rx_stat_frm_256_511_0;
volatile unsigned int rx_stat_frm_256_511_1;
volatile unsigned int rx_stat_frm_512_1023_0;
volatile unsigned int rx_stat_frm_512_1023_1; //0x1F8
volatile unsigned int rx_stat_frm_1024_1518_0;
volatile unsigned int rx_stat_frm_1024_1518_1;
volatile unsigned int rx_stat_frm_1519_2047_0;
volatile unsigned int rx_stat_frm_1519_2047_1; //0x208
volatile unsigned int rx_stat_frm_2048_4095_0;
volatile unsigned int rx_stat_frm_2048_4095_1;
volatile unsigned int rx_stat_frm_4096_9216_0;
volatile unsigned int rx_stat_frm_4096_9216_1; //0x218
volatile unsigned int rx_stat_frm_9217_16383_0;
volatile unsigned int rx_stat_frm_9217_16383_1;
4.2. tsemac_handle_t

This structure is used to declare different types of parameters used for the TSEMAC API. Table 4.1 shows the available parameters and description.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>speed_mode</td>
<td>- Part of the tsemac_handle_t structure.</td>
</tr>
<tr>
<td></td>
<td>- Used for setting the speed for TSEMAC.</td>
</tr>
<tr>
<td>adr</td>
<td>- Part of the tsemac_handle_t structure.</td>
</tr>
<tr>
<td></td>
<td>- Represents the base address of TSEMAC.</td>
</tr>
<tr>
<td>frame_length</td>
<td>- Part of the tsemac_handle_t structure.</td>
</tr>
<tr>
<td></td>
<td>- Represents the Ethernet packet length to be transmitted to TSEMAC.</td>
</tr>
<tr>
<td>mac_upper</td>
<td>- Part of the tsemac_handle_t structure.</td>
</tr>
<tr>
<td></td>
<td>- Represents the variable to set and get first four bytes of MAC address for TSEMAC.</td>
</tr>
<tr>
<td>mac_lower</td>
<td>- Part of the tsemac_handle_t structure.</td>
</tr>
<tr>
<td></td>
<td>- Represents the variable to set and get last two bytes of MAC address for TSEMAC.</td>
</tr>
<tr>
<td>multicast_upper</td>
<td>- Part of the tsemac_handle_t structure.</td>
</tr>
<tr>
<td></td>
<td>- Represents the variable to set and get first four bytes of 64-bit hash for TSEMAC.</td>
</tr>
<tr>
<td>multicast_lower</td>
<td>- Part of the tsemac_handle_t structure.</td>
</tr>
<tr>
<td></td>
<td>- Represents the variable to set and get last four bytes of 64-bit hash for TSEMAC.</td>
</tr>
<tr>
<td>tx_rx_ctrl_var</td>
<td>- Part of the tsemac_handle_t structure.</td>
</tr>
<tr>
<td></td>
<td>- Represents the transmit and receive control register configuration for TSEMAC.</td>
</tr>
<tr>
<td>enable_tx_mac</td>
<td>- Part of the tsemac_handle_t structure.</td>
</tr>
<tr>
<td></td>
<td>- Used to enable the Tx MAC.</td>
</tr>
<tr>
<td>enable_rx_mac</td>
<td>- Part of the tsemac_handle_t structure.</td>
</tr>
<tr>
<td></td>
<td>- Used to enable the Rx MAC.</td>
</tr>
</tbody>
</table>
5. API Enum

5.1. speed_mode_set

This enum sets the different speeds and modes for TSEMAC. Table 5.1. speed_mode_set Enum Variables shows the speed_mode_set enum variables and description.

<table>
<thead>
<tr>
<th>Variable</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>fast_half_duplex_mode</td>
<td>This variable is used to set TSEMAC to half duplex mode and speed at 10/100 Mbps.</td>
</tr>
<tr>
<td>fast_full_duplex_mode</td>
<td>This variable is used to set TSEMAC to full duplex mode and speed at 10/100 Mbps.</td>
</tr>
<tr>
<td>one_g_mode</td>
<td>This variable is used to set TSEMAC to full duplex mode and speed at 1000 Mbps.</td>
</tr>
</tbody>
</table>

5.2. statistics_counter_reg

This enum is used to assign the offset for the statistics counter register by passing enum values. Table 5.2 shows the statistics_counter_reg enum variables and description.

<table>
<thead>
<tr>
<th>Variable</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>tx_unicast_frame_counter_reg</td>
<td>This variable is used to read the total unicast frame transmit.</td>
</tr>
<tr>
<td>tx_multicast_frame_counter_reg</td>
<td>This variable is used to read the total multicast frame transmit.</td>
</tr>
<tr>
<td>tx_broadcast_frame_counter_reg</td>
<td>This variable is used to read the total broadcast frame transmit.</td>
</tr>
<tr>
<td>tx_badfcs_frame_counter_reg</td>
<td>This variable is used to read the total bad fcs frame transmit.</td>
</tr>
<tr>
<td>tx_jumbo_frame_counter_reg</td>
<td>This variable is used to read the total jumbo frame transmit.</td>
</tr>
<tr>
<td>tx_under_run_frame_counter_reg</td>
<td>This variable is used to read the total FIFO under run.</td>
</tr>
<tr>
<td>tx_pause_frame_counter_reg</td>
<td>This variable is used to read the total pause frame transmit.</td>
</tr>
<tr>
<td>tx_vlan_tag_frame_counter_reg</td>
<td>This variable is used to read the total vlan tagged frame transmit.</td>
</tr>
<tr>
<td>tx_frame_length_counter_reg</td>
<td>This variable is used to read the total frame length.</td>
</tr>
<tr>
<td>tx_deferred_transmission_counter_reg</td>
<td>This variable is used to read the total deferred frame while transmit.</td>
</tr>
<tr>
<td>tx_excessive_deferred_transmission_counter_reg</td>
<td>This variable is used to read the total excessive frame deferred while transmitting.</td>
</tr>
<tr>
<td>tx_late_collision_counter_reg</td>
<td>This variable is used to read the total number of collisions.</td>
</tr>
<tr>
<td>tx_excessive_collision_counter_reg</td>
<td>This variable is used to read the total number of excessive collisions.</td>
</tr>
<tr>
<td>tx_num_early_collision_counter_reg</td>
<td>This variable is used to read the total number of early collisions.</td>
</tr>
<tr>
<td>tx_short_frame_dis_fcs_counter_reg</td>
<td>This variable is used to read the total short frames transmitted when FCS field is disabled.</td>
</tr>
<tr>
<td>tx_ptp_1588_frame_counter_reg</td>
<td>This variable is used to read the total ptp frames transmitted.</td>
</tr>
<tr>
<td>tx_frame_length_64_counter_reg</td>
<td>This variable is used to read the total frames transmitted with length of 64.</td>
</tr>
<tr>
<td>tx_frame_length_65_127_counter_reg</td>
<td>This variable is used to read the total frames transmitted with of 65 to 127.</td>
</tr>
<tr>
<td>tx_frame_length_128_255_counter_reg</td>
<td>This variable is used to read the total frames transmitted with of 128 to 255.</td>
</tr>
<tr>
<td>tx_frame_length_256_511_counter_reg</td>
<td>This variable is used to read the total frames transmitted with of 256 to 511.</td>
</tr>
<tr>
<td>tx_frame_length_512_1023_counter_reg</td>
<td>This variable is used to read the total frames transmitted with of 512 to 1023.</td>
</tr>
<tr>
<td>tx_frame_length_1024_1518_counter_reg</td>
<td>This variable is used to read the total frames transmitted with of 1024 to 1518.</td>
</tr>
<tr>
<td>tx_frame_length_1519_2047_counter_reg</td>
<td>This variable is used to read the total frames transmitted with of 1519 to 2047.</td>
</tr>
<tr>
<td>Variable</td>
<td>Description</td>
</tr>
<tr>
<td>-----------------------------------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>tx_frame_length_2048_4095_counter_reg</td>
<td>This variable is used to read the total frames transmitted with of 2048 to 4095.</td>
</tr>
<tr>
<td>tx_frame_length_4096_9216_counter_reg</td>
<td>This variable is used to read the total frames transmitted with of 4096 to 9216.</td>
</tr>
<tr>
<td>tx_frame_length_9217_16383_counter_reg</td>
<td>This variable is used to read the total frames transmitted with of 9217 to 16383.</td>
</tr>
<tr>
<td>rx_frame_length_counter_reg</td>
<td>This variable is used to read the total frame length received.</td>
</tr>
<tr>
<td>rx_vlan_tag_frame_counter_reg</td>
<td>This variable is used to read the total vlan tag frames received.</td>
</tr>
<tr>
<td>rx_pause_frame_counter_reg</td>
<td>This variable is used to read the total pause frames received.</td>
</tr>
<tr>
<td>rx_control_frame_counter_reg</td>
<td>This variable is used to read the total control frames received.</td>
</tr>
<tr>
<td>rx_unsupported_opcode_reg</td>
<td>This variable is used to read the total unsupported opcode frames received.</td>
</tr>
<tr>
<td>rx_dribble_nibble_counter_reg</td>
<td>This variable is used to read the total dribble nibble frames received.</td>
</tr>
<tr>
<td>rx_broadcast_frame_counter_reg</td>
<td>This variable is used to read the total broadcast frames received.</td>
</tr>
<tr>
<td>rx_multicast_frame_counter_reg</td>
<td>This variable is used to read the total multicast frames received.</td>
</tr>
<tr>
<td>rxunicast_frame_counter_reg</td>
<td>This variable is used to read the total unicast frames received.</td>
</tr>
<tr>
<td>rx_frame_received_ok_counter_reg</td>
<td>This variable is used to read the total frames received.</td>
</tr>
<tr>
<td>rx_frame_received_length_error_counter_reg</td>
<td>This variable is used to read the total error in received frame length.</td>
</tr>
<tr>
<td>rx_frame_received_crc_error_counter_reg</td>
<td>This variable is used to read the total crc error in received frame.</td>
</tr>
<tr>
<td>rx_frame_received_packet_ignored_counter_reg</td>
<td>This variable is used to read the total number of packets ignored.</td>
</tr>
<tr>
<td>rx_frame_received_carrier_event_counter_reg</td>
<td>This variable is used to read the total number of packets received with carrier event detected.</td>
</tr>
<tr>
<td>rx_ptp_1588_frame_counter_reg</td>
<td>This variable is used to read the total ptp frames received.</td>
</tr>
<tr>
<td>rx_frame_received_ipg_violation_counter_reg</td>
<td>This variable is used to read the total frames received with igp violation.</td>
</tr>
<tr>
<td>rx_received_short_frame_counter_reg</td>
<td>This variable is used to read the total short frames received.</td>
</tr>
<tr>
<td>rx_received_long_frame_counter_reg</td>
<td>This variable is used to read the total long frames received.</td>
</tr>
<tr>
<td>rx_received_undersize_frame_counter_reg</td>
<td>This variable is used to read the total frames received of length less than 64 bytes.</td>
</tr>
<tr>
<td>rx_received_frame.fragments_counter_reg</td>
<td>This variable is used to read the total frames received of length less than 64 bytes and has either an FCS error or an Alignment error.</td>
</tr>
<tr>
<td>rx_received_frame.jabber_counter_reg</td>
<td>This variable is used to read the total frame length of more than 1518 bytes and has either an FCS error or an Alignment error.</td>
</tr>
<tr>
<td>rx_received_frame_length64.good_crc_counter_reg</td>
<td>This variable is used to read the total received frames with length of less than 64 bytes and has a good CRC.</td>
</tr>
<tr>
<td>rx_received_frame_length1518.good_crc_counter_reg</td>
<td>This variable is used to read the total received frames with length of more than 1518 bytes and has a good CRC.</td>
</tr>
<tr>
<td>rx_frame_length_64_counter_reg</td>
<td>This variable is used to read the total frames received with length of 64.</td>
</tr>
<tr>
<td>rx_frame_length_65_127_counter_reg</td>
<td>This variable is used to read the total frames received with length of 65 to 127.</td>
</tr>
<tr>
<td>rx_frame_length_128_255_counter_reg</td>
<td>This variable is used to read the total frames received with length of 128 to 255.</td>
</tr>
<tr>
<td>rx_frame_length_256_511_counter_reg</td>
<td>This variable is used to read the total frames received with length of 256 to 511.</td>
</tr>
<tr>
<td>rx_frame_length_512_1023_counter_reg</td>
<td>This variable is used to read the total frames received with length of 512 to 1023.</td>
</tr>
<tr>
<td>rx_frame_length_1024_1518_counter_reg</td>
<td>This variable is used to read the total frames received with length of 1024 to 1518.</td>
</tr>
<tr>
<td>rx_frame_length_1519_2047_counter_reg</td>
<td>This variable is used to read the total frames received with length of 1519 to 2047.</td>
</tr>
<tr>
<td>rx_frame_length_2048_4095_counter_reg</td>
<td>This variable is used to read the total frames received with length of 2048 to 4095.</td>
</tr>
<tr>
<td>Variable</td>
<td>Description</td>
</tr>
<tr>
<td>-----------------------------------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td><code>rx_frame_length_4096_9216_counter_reg</code></td>
<td>This variable is used to read the total frames received with length of 4096 to 9216.</td>
</tr>
<tr>
<td><code>rx_frame_length_9217_16383_counter_reg</code></td>
<td>This variable is used to read the total frames received with length of 9217 to 16383.</td>
</tr>
</tbody>
</table>
6. API Variables

Table 6.1 shows the variables and their description.

Table 6.1. Variable Description

<table>
<thead>
<tr>
<th>Variable</th>
<th>Description</th>
</tr>
</thead>
</table>
| handle   | • Used in the TSEMAC API.  
          | • A structure variable that consists of different variables. |
| status   | Returns success or failure from the API. |
7. API Macros

7.1. Success and Failure
#define SUCCESS 1
#define FAILURE 0

7.2. Frame Length
#define FRAME_LENGTH 64

7.3. IPG Time
#define IPG_TIME 12

7.4. Maximum Packet size
#define MAX_PACKET_SIZE 1500

7.5. Control Register Macros
#define SET_FULL_DUPLEX_MODE 5
#define SET_HALF_DUPLEX_MODE 5

7.6. Mode Register Macros
#define SPEED_10_OR_100_MBPS 0
#define SPEED_1G 0

7.7. Shift value
#define SIXTEEN_BIT 16

7.8. Index value
#define ZERO 0
#define ONE 1
References

- Tri-Speed Ethernet MAC IP Core – Lattice Radiant Software (FPGA-IPUG-02084) user guide
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Certus-NX web page
- CertusPro-NX web page
- CrossLink-NX web page
- Mach-NX web page
- MachXO2 web page
- MachXO3D web page
- MachXO5-NX web page
- Lattice Solutions IP Cores web page
- Lattice Radiant Software FPGA web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans
Technical Support Assistance

Submit a technical support case through [www.latticesemi.com/techsupport](http://www.latticesemi.com/techsupport).

For frequently asked questions, refer to the Lattice Answer Database at [www.latticesemi.com/Support/AnswerDatabase](http://www.latticesemi.com/Support/AnswerDatabase).
### Revision History

**Revision 1.0, December 2023**

<table>
<thead>
<tr>
<th>Section</th>
<th>Change Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Initial release.</td>
</tr>
</tbody>
</table>