sysI/O User Guide for Nexus Platform

Technical Note

FPGA-TN-02067-2.4

July 2024
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## Acronyms in This Document

A list of acronyms used in this document.

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td>Double Data Rate</td>
</tr>
<tr>
<td>HDL</td>
<td>Hardware Description Language</td>
</tr>
<tr>
<td>LVCMOS</td>
<td>Low Voltage Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>LVDS</td>
<td>Low-Voltage Differential Signaling</td>
</tr>
<tr>
<td>LVTTL</td>
<td>Low Voltage Transistor-Transistor Logic</td>
</tr>
<tr>
<td>PIO</td>
<td>Programmable Input/Output</td>
</tr>
<tr>
<td>VHDL</td>
<td>VHSIC Hardware Description Language</td>
</tr>
<tr>
<td>VHSIC</td>
<td>Very High Speed Integrated Circuit</td>
</tr>
</tbody>
</table>
1. Introduction

FPGA devices built on the Lattice Nexus™ platform feature sysI/O™ buffers that are designed to support a wide range of interfaces. Two types of I/O are offered, wide range I/O on the top, left and right banks and high performance I/O on the bottom banks only. It gives user the ability to easily interface with other devices using advanced system I/O standards. For detailed information about supported sysI/O standards, refer to CrossLink™-NX Family Data Sheet (FPGA-DS-02049), Certus™-NX Family Data Sheet (FPGA-DS-02078), CertusPro™-NX Family Data Sheet (FPGA-DS-02086), MachXO5™-NX Family Data Sheet (FPGA-DS-02102), and CrossLink-NX™-33 and CrossLinkU™-NX Data Sheet (FPGA-DS-02104).

2. sysI/O Overview

The key features of the sysI/O block are:

- Wide range I/O bank supports single-ended standards only. High-performance I/O bank supports differential standards as well as single-ended standards.
- Wide-range I/O (WRIO) banks are located on the Top, Left, and Right sides of the device.
- High-performance I/O (HPIO) banks are located on the Bottom side of the device.
- Internal weak pull down on all I/O.
- Support for on-chip programmable 3.3 kΩ pull-up resister in WRIO banks, for I2C, I3C, and other general-purpose applications.
- Support for on-chip dynamic differential input 100 Ω termination for I/O in bottom HPIO banks.
- Single-end termination with a programmable 40/50/60/75 Ω resistor is supported in all banks.
- Input Hysteresis on all LVCMOS33/LVTTL33, LVCMOS25, LVCMOS18, and LVCMOS15.
- Programmable Open Drain on all outputs.
- Programmable Clamp WRIO banks.
- Hot socket-compliant GPIO is available in WRIO banks.
3. sysI/O Banking Scheme

3.1. CrossLink-NX, Certus-NX, and CertusPro-NX Devices

CrossLink-NX, Certus-NX, and CertusPro-NX devices have up to eight banks in total. For the 28k, 40k, 50k, and 100k devices, there is one bank on top, two banks each on the left and right side of the device, and three on the bottom side of the device. For the 9k and 17k device, there is one bank on top, one on the right side, and three on the bottom side of the device. The higher the density of the Nexus platform device, the more pins there are in each bank. I/O in Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7 are wide range I/O support of up to VCCIO 3.3 V. While I/O in Bank 3, Bank 4, and Bank 5 are high-performance I/O support of up to VCCIO 1.8 V. In addition, Bank 3, Bank 4, and Bank 5 support two VREF inputs for flexibility to receive two different referenced input levels on the same bank. Figure 3.1 shows the location of each bank.

*Note: Banks not available in 9k and 17k device.

Figure 3.1. CrossLink-NX, Certus-NX, CertusPro-NX sysI/O Banking

3.1.1. Vcc (1.0 V)

This is the core supply. This Vcc supply is used to power the control logic. The control signals and data signals from the I/O logic are then translated to a higher supply of the I/O buffers.
3.1.2. **$V_{CCIO}^{[0, 1, 2, 6, 7]}$ Wide Range (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V)**
Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7 have a $V_{CCIO}$ supply that operates from 3.3 V down to 1.2 V.

3.1.3. **$V_{CCIO}^{[3, 4, 5]}$ High Performance (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V)**
Bank 3, Bank 4, and Bank 5 operate with $V_{CCIO}$ of 1.8 V down to 1.0 V. Standards such as LVDS, SSTL, HSTL, and SLVS are only supported on these three banks.

3.1.4. **$V_{CC AUX}$ (1.8 V)**
In addition to the bank $V_{CCIO}$ supplies and a $V_{CC}$ core logic supply, Nexus platform devices have a $V_{CC AUX}$ auxiliary supply that powers the differential and referenced input buffers.

3.2. **MachXO5-NX Devices**
The LFMXOS-25/LFMXOS-15D devices have ten GPIO banks. There are two banks on top, three banks each on the left and right side of the device, and two on the bottom side of the device.
Bank 1 can support only $V_{CCIO}$ 3.3 V. Bank 0, Bank 2, Bank 3, Bank 4, Bank 7, Bank 8 and Bank 9 support up to $V_{CCIO}$ 3.3 V. Bank 5 and Bank 6 support up to $V_{CCIO}$ 1.8 V. In addition, Bank 5 and Bank 6 support two VREF inputs for flexibility to receive two different referenced input levels on the same bank. Figure 3.2 shows the location of each bank.
The LFMXOS-100T/LFMXOS-55T/LFMXOS-55TD devices have eight GPIO banks. There is one bank on top, two banks each on the left and right side of the device, and three on the bottom side of the device.
Bank 0 can support only $V_{CCIO}$ 3.3 V. Bank 1, Bank 2, Bank 6, and Bank 7 support up to $V_{CCIO}$ 3.3 V. Bank 3, Bank 4, and Bank 5 support up to $V_{CCIO}$ 1.8 V. In addition, Bank 3, Bank 4, and Bank 5 support two VREF inputs for flexibility to receive two different referenced input levels on the same bank. Figure 3.3 shows the location of each bank.

Figure 3.2. LFMXOS-25/LFMXOS-15D sysl/O Banking
3.2.1. **V_CCC (1.0 V)**

This is the core supply. This V_CC supply is used to power the control logic. The control signals and data signals from the I/O logic are then translated to higher supply of the I/O buffers.

3.2.2. **V_CCIO \([0, 1, 2, 3, 4, 7, 8, 9]\) Wide Range for LFMXOS-25/LFMXO5-15D (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V)**

Bank 1 has a V_CCIO supply that operates on 3.3 V. Bank 0, Bank 2, Bank 3, Bank 4, Bank 7, Bank 8, and Bank 9 have a V_CCIO supply that operates from 3.3 V down to 1.2 V.

3.2.3. **V_CCIO \([0, 1, 2, 6, 7]\) Wide Range for LFMXOS-100T/LFMXOS-55T/LFMXOS-55TD (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V)**

Bank 0 has a V_CCIO supply that operates on 3.3 V. Bank 0, Bank 1, Bank 2, Bank 6 and Bank 7 have a V_CCIO supply that operates from 3.3 V down to 1.2 V.

3.2.4. **V_CCIO \([5, 6]\) High Performance for LFMXOS-25/LFMXO5-15D (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V)**

Bank 5 and Bank 6 operate with V_CCIO of 1.8 V down to 1.0 V. Standards such as LVDS, SSTL, HSTL, and SLVS are only supported on these two banks.

3.2.5. **V_CCIO \([3, 4, 5]\) High Performance for LFMXOS-100T/LFMXOS-55T/LFMXOS-55TD (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V)**

Bank 3, Bank 4, and Bank 5 operate with V_CCIO of 1.8 V down to 1.0 V. Standards such as LVDS, SSTL, HSTL, and SLVS are only supported on these three banks.

Figure 3.3. LFMXOS-100T/LFMXOS-55T/LFMXOS-55TD sysI/O Banking
3.2.6. $V_{\text{CCAUX}}$ (1.8 V)
In addition to the bank $V_{\text{CCIO}}$ supplies and a $V_{\text{CC}}$ core logic supply, Nexus platform devices have a $V_{\text{CCAUX}}$ auxiliary supply that powers the differential and referenced input buffers.

3.3. CrossLink-NX-33 Devices
CrossLink-NX-33 devices have six banks in total, three banks on the top side of the device and three banks on the bottom side of the device. I/O in Bank 0, Bank 1, and Bank 5 are wide range I/O support of up to $V_{\text{CCIO}}$ 3.3 V. Bank 2, Bank 3, and Bank 4, on the other hand, are high-performance I/O support of up to $V_{\text{CCIO}}$ 1.8 V. In addition, Bank 2, Bank 3, and Bank 4 support two VREF inputs for flexibility to receive two different reference input levels on the same bank. Figure 3.4 shows the location of each bank.

3.3.1. $V_{\text{CC}}$ (1.0 V)
This is the core supply. This $V_{\text{CC}}$ supply is used to power the control logic. The control signals and data signals from the I/O logic are then translated to a higher supply of the I/O buffers.

3.3.2. $V_{\text{CCIO}}$ [0, 1, 5] Wide Range (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V)
Bank 0, Bank 1, and Bank 5 have a $V_{\text{CCIO}}$ supply that operates from 3.3 V down to 1.2 V.

3.3.3. $V_{\text{CCIO}}$ [2, 3, 4] High Performance (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V)
Bank 2, Bank 3, and Bank 4 operate with $V_{\text{CCIO}}$ of 1.8 V down to 1.0 V. Standards such as LVDS, SSTL, HSTL, and SLVS are only supported on these three banks.

3.3.4. $V_{\text{CCAUX}}$ (1.8 V)
In addition to the bank $V_{\text{CCIO}}$ supplies and a $V_{\text{CC}}$ core logic supply, Nexus platform devices have a $V_{\text{CCAUX}}$ auxiliary supply that powers the differential and referenced input buffers.
### 3.4. CrossLinkU-NX Devices

CrossLinkU-NX devices have five banks in total, two banks on the top side of device and three banks on the bottom side of device. I/O in Bank 0 and Bank 1 are wide range I/O support of up to $V_{CCIO}$ 3.3 V. Bank 2, Bank 3, and Bank 4, on the other hand, are high performance I/O support of up to $V_{CCIO}$ 1.8 V. In addition, Bank 2, Bank 3, and Bank 4 support two VREF inputs for flexibility to receive two different reference input levels on the same bank. Figure 3.5 shows the location of each bank.

![CrossLinkU-NX sysI/O Banking](image)

#### 3.4.1. $V_{CC}$ (1.0 V)

This is the core supply. This $V_{CC}$ supply is used to power the control logic. The control signals and data signals from the I/O logic are then translated to higher supply of the I/O buffers.

#### 3.4.2. $V_{CCIO}$ [$0, 1$] Wide Range (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V)

Bank 0 and Bank 1 have a $V_{CCIO}$ supply that operates from 3.3 V down to 1.2 V.

#### 3.4.3. $V_{CCIO}$ [$2, 3, 4$] High Performance (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V)

Bank 2, Bank 3, and Bank 4 operate with $V_{CCIO}$ of 1.8 V down to 1.0 V. Standards such as LVDS, SSTL, HSTL, and SLVS are only supported on these three banks.

#### 3.4.4. $V_{CCaux}$ (1.8 V)

In addition to the bank $V_{CCIO}$ supplies and a $V_{CC}$ core logic supply, Nexus platform devices have a $V_{CCaux}$ auxiliary supply that powers the differential and referenced input buffers.
3.5. Standby

Using Standby mode dynamically powers down the bank. It disables the differential/reference receiver, true differential driver, current mirrors, and bias circuits.

In Standby mode, differential drivers and differential input buffers can be powered down to save power. Standby mode is enabled on a bank-by-bank basis. Each bank has user-routed input signals to enable Standby (dynamic power-down) mode.

Refer to Power Management and Calculation for CrossLink-NX Devices (FPGA-TN-02075) or Power Management and Calculation for Certus-NX, CertusPro-NX, MachXO5-NX (FPGA-TN-02257) for detailed information.

3.6. High-Performance sysI/O Buffer Pairs (On Bottom Side)

The I/O pair consists of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The A pad-referenced input buffer can also be configured as a differential input. Each I/O has a weak pullup, pulldown, or buskeeper feature. These are disabled in output mode. The two pads in the pair are referred to as True and Comp, where the True pad is associated with the positive side of the differential I/O and the Comp or complement pad is associated with the negative side.

Every pair also has a programmable 100 Ω differential input termination resistor. Every pair also has a true LVDS and SLVS200 TX driver. They have an independent tri-state capability.

The single-ended driver associated with the complementary pad can be optionally driven by the complement of the data that drives the single-ended driver associated with the true pad. This allows a pair of single-ended drivers to be used to drive complementary outputs with the lowest possible skew between the signals. Pads A and B form a DIFF I/O pair. When this option is selected, the tri-state control for the driver associated with the complementary pad is driven by the same signal as the tri-state control for the driver associated with the true pad.

Refer to the High-Performance I/O pair block diagram in Figure 3.6.
3.7. Wide Range sysI/O Buffer Pair (On Top, Left/Right Sides)

The I/O pair consists of two single-ended output drivers and two sets of single-ended input buffers (ratioed only). Each I/O has a weak pullup, pulldown, or buskeeper feature. These are disabled in output mode. The two pads in the pair are referred to as True and Comp, where the True pad is associated with the positive side of the Complementary I/O, and the Comp or complement pad is associated with the negative side.

The single-ended driver associated with the complementary pad can be optionally driven by the complement of the data that drives the single-ended driver associated with the True pad. This allows a pair of single-ended drivers to be used to drive complementary outputs with the lowest possible skew between the signals. Pads A and B form a Complementary I/O pair. When this option is selected, the tri-state control for the driver associated with the complement pad is driven by the same signal as the tri-state control for the driver associated with the true pad.

Figure 3.7 shows the Wide Range I/O pair block diagram.
Figure 3.7. Wide Range sysI/O Buffer for Top, Left/Right Side

*From CIB
4. **V\textsubscript{CCIO} Requirement for I/O Standards**

Each I/O bank of a device built on the Nexus platform has a separate V\textsubscript{CCIO} supply pin that can be connected to 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V for bottom banks and 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V for the rest of the banks. These voltages are used to power the output I/O standard and source the drive strength for the output. On the input side, each pad is connected to a set of ratioed input buffers that provide support for the following:

- Fixed threshold 1.0 V/1.2 V input standards
- Ratioed V\textsubscript{CCIO} input standards
- Ratioed V\textsubscript{CCAUX} based 1.8/1.5V LVCMOS inputs

These three buffers are connected to V\textsubscript{CC}, V\textsubscript{CCIO}, and V\textsubscript{CCAUX} respectively.

### Table 4.1. Input Mixed Mode\textsuperscript{4} for Wide Range Input Buffers

<table>
<thead>
<tr>
<th>V\textsubscript{CCIO} (V)</th>
<th>LVCMOS\textsubscript{10}</th>
<th>LVCMOS\textsubscript{12}</th>
<th>LVCMOS\textsubscript{15}</th>
<th>LVCMOS\textsubscript{18}</th>
<th>LVCMOS\textsubscript{25}</th>
<th>LVCMOS\textsubscript{33}</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>V\textsubscript{CC} Powered Buffer</td>
<td>V\textsubscript{CCAUX} Powered Buffer</td>
<td>V\textsubscript{CCIO} Powered Buffer</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.2</td>
<td>✓ 2</td>
<td>✓ 2</td>
<td>✓ 1, 3</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>1.5</td>
<td>✓ 2</td>
<td>✓ 2</td>
<td>✓ 1, 3</td>
<td>✓</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>1.8</td>
<td>✓ 2</td>
<td>✓ 2</td>
<td>✓ 1, 3</td>
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<td>—</td>
<td>—</td>
</tr>
<tr>
<td>2.5</td>
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<td>✓ 2</td>
<td>✓ 1, 3</td>
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<td>✓ 2</td>
<td>✓ 1, 3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

**Notes:**
1. Increased ICC is due to underdrive.
2. No Hysteresis.
3. Reduced Hysteresis.
4. Set CLAMP setting on the I/Os to OFF to support mixed mode.

### Table 4.2. Input Mixed Mode\textsuperscript{3} for High-Performance Input Buffers

<table>
<thead>
<tr>
<th>V\textsubscript{CCIO} (V)</th>
<th>LVCMOS\textsubscript{1.0}</th>
<th>LVCMOS\textsubscript{1.2}</th>
<th>LVCMOS\textsubscript{1.5}</th>
<th>LVCMOS\textsubscript{1.8}</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>V\textsubscript{CC} Powered Buffer</td>
<td>V\textsubscript{CCIO} Powered Buffer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.0</td>
<td>✓</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>1.2</td>
<td>✓</td>
<td>✓</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>1.5</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>—</td>
</tr>
<tr>
<td>1.8</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓, 2</td>
</tr>
</tbody>
</table>

**Notes:**
1. Increased ICC is due to underdrive.
2. Reduced Hysteresis.
3. Set CLAMP setting on the I/Os to OFF to support mixed mode.
5. sysI/O Buffer Configurations

This section describes the various sysI/O features available on the Nexus platform device.

5.1. Programmable Drive Strength

All single-ended drivers have programmable drive strength. Table 5.1 and Table 5.2 show the programmable drive strength of all the I/O standards available in devices built on the Nexus platform. The maximum current allowed per bank as well as the package thermal limit current should be taken into consideration when selecting the drive strength.

Table 5.1. Programmable Drive Strength Values at Various V\text{CCIO} Voltages for Wide Range Output Driver

<table>
<thead>
<tr>
<th>I/O TYPE</th>
<th>Drive Strength (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVCMOS33</td>
<td>2, 4, 8, 12, 16</td>
</tr>
<tr>
<td>LVCMOS25</td>
<td>2, 4, 8, 10</td>
</tr>
<tr>
<td>LVCMOS18</td>
<td>2, 4, 8</td>
</tr>
<tr>
<td>LVCMOS15</td>
<td>2, 4</td>
</tr>
<tr>
<td>LVCMOS12</td>
<td>2, 4</td>
</tr>
</tbody>
</table>

Table 5.2. Programmable Drive Strength Values at Various V\text{CCIO} Voltages for High-Performance Output Driver

<table>
<thead>
<tr>
<th>I/O TYPE</th>
<th>Drive Strength (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVCMOS18</td>
<td>2, 4, 8, 12</td>
</tr>
<tr>
<td>LVCMOS15</td>
<td>2, 4</td>
</tr>
<tr>
<td>LVCMOS12</td>
<td>2, 4</td>
</tr>
<tr>
<td>LVCMOS10</td>
<td>2, 4</td>
</tr>
</tbody>
</table>

5.2. Programmable Slew Rate

The single-ended output buffer for each I/O pin has programmable output slew rate control that can be configured for either low noise, SLEWRATE=SLOW; or high speed, SLEWRATE=FAST; or in between, SLEWRATE=MED.

5.3. Tri-state Control

On the output side, each single-ended driver has a separate tri-state control. The differential driver has a tri-state control as well.

5.4. Open Drain Control

In addition to the tri-state control, the single-ended drivers also support open drain operation on each I/O independently. Unlike non-open drain output which consists of a source and sink section, an open drain output is composed of only the sink section of the output driver. User can implement an open drain output by turning on the OPENDRAIN attribute in the software.
5.5. **Differential Input Termination**

Nexus platform devices support a programmable 100 Ω input termination between all pairs on the bottom banks. The input termination of 100 Ω can be programmed between on and off. Figure 5.1 shows the discrete off-chip and on-chip solutions for dedicated, differential input termination.

![Figure 5.1. Off-Chip and On-Chip Solutions](image)

5.6. **Programmable Clamp**

Programmable Clamp only applies to I/O on the Top, Left, and Right banks.

5.7. **Soft MIPI D-PHY Support**

The following primitive should be used when implementing soft MIPI D-PHY I/O in Nexus platform devices for High Speed (HS) as well as Low Power (LP) mode for RX and TX. MIPI primitive is supported in Bank 3, Bank 4, and Bank 5 on the bottom side of the device.

![Figure 5.2. MIPI Primitive Symbol](image)
Table 5.3. MIPI Port List

<table>
<thead>
<tr>
<th>Port</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BP</td>
<td>I/O</td>
<td>Bidirectional PAD A used for D-PHY Clock/Data in both HS and LP mode</td>
</tr>
<tr>
<td>BN</td>
<td>I/O</td>
<td>Bidirectional PAD B used for D-PHY Clock/Data in both HS and LP mode</td>
</tr>
<tr>
<td>AP</td>
<td>I</td>
<td>Input from fabric to PAD A – used for LP Tx function only</td>
</tr>
<tr>
<td>AN</td>
<td>I</td>
<td>Input from fabric to PAD B – used for LP Tx function only</td>
</tr>
<tr>
<td>HSRXEN</td>
<td>I</td>
<td>Enable to receive HS differential signals</td>
</tr>
<tr>
<td>HSTXEN</td>
<td>I</td>
<td>Enable to transmit HS differential signals</td>
</tr>
<tr>
<td>TP</td>
<td>I</td>
<td>Tri-state for PAD A</td>
</tr>
<tr>
<td>TN</td>
<td>I</td>
<td>Tri-state for PAD B</td>
</tr>
<tr>
<td>OLSP</td>
<td>O</td>
<td>LP Rx signal from BP</td>
</tr>
<tr>
<td>OLSN</td>
<td>O</td>
<td>LP Rx signal from BN</td>
</tr>
<tr>
<td>OHS</td>
<td>O</td>
<td>HS Rx signal from BP/BN differential</td>
</tr>
<tr>
<td>IHS</td>
<td>I</td>
<td>De-serialized input from DDR output register</td>
</tr>
</tbody>
</table>

When IO_TYPE is MIPI, the MIPI primitive above should be instantiated in the design, otherwise the software Design Rule Check (DRC) errors out. The output from the MIPI D-PHY buffer can only be used with the Double Data Rate (DDR) registers. Refer to Certus-NX High-Speed I/O Interface (FPGA-TN-02216), CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097), CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244), MachXO5-NX Family Data Sheet (FPGA-DS-02102), or CrossLink-NX-33 and CrossLinkU-NX Data Sheet (FPGA-DS-02104) for details on building MIPI D-PHY interfaces.
6. Software sysI/O Attributes

The sysI/O attributes can be specified in the Hardware Description Language (HDL), using Device Constraint Editor, or in Pre/Post Timing Constraint Editor (.ldc/.pdc).

6.1. IO_TYPE

This attribute is used to set the sysI/O standard for an I/O. The $V_{CCIO}$ required to set these I/O standards is embedded in the attribute names. Table 6.1 lists the available I/O types.

<table>
<thead>
<tr>
<th>sysI/O Signaling Standard</th>
<th>IO_TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default</td>
<td>LVCMOS18</td>
</tr>
<tr>
<td>LVDS 1.8V</td>
<td>LVDS</td>
</tr>
<tr>
<td>LVDS 1.8V Emulation</td>
<td>LVDS15</td>
</tr>
<tr>
<td>Sub-LVDS</td>
<td>SUBLVDS</td>
</tr>
<tr>
<td>Sub-LVDS Emulation</td>
<td>SUBLVDSE</td>
</tr>
<tr>
<td>Sub-LVDS Emulation High Speed</td>
<td>SUBLVDSEH</td>
</tr>
<tr>
<td>SLVS</td>
<td>SLVS</td>
</tr>
<tr>
<td>MIPI_DPHY</td>
<td>MIPI_DPHY</td>
</tr>
<tr>
<td>SSTL 1.5V Class I</td>
<td>SSTL15_I</td>
</tr>
<tr>
<td>SSTL 1.5V Class II</td>
<td>SSTL15_II</td>
</tr>
<tr>
<td>SSTL 1.5V Differential Class I</td>
<td>SSTL15D_I</td>
</tr>
<tr>
<td>SSTL 1.5V Differential Class II</td>
<td>SSTL15D_II</td>
</tr>
<tr>
<td>SSTL 1.35V Class I</td>
<td>SSTL135_I</td>
</tr>
<tr>
<td>SSTL 1.35V Class II</td>
<td>SSTL135_II</td>
</tr>
<tr>
<td>SSTL 1.35V Differential Class I</td>
<td>SSTL135D_I</td>
</tr>
<tr>
<td>SSTL 1.35V Differential Class II</td>
<td>SSTL135D_II</td>
</tr>
<tr>
<td>HSTL 1.5V Class I</td>
<td>HSTL15_I</td>
</tr>
<tr>
<td>HSTL 1.5V Differential Class I</td>
<td>HSTL15D_I</td>
</tr>
<tr>
<td>HSUL 1.2V</td>
<td>HSUL12</td>
</tr>
<tr>
<td>HSUL 1.2V Differential</td>
<td>HSUL12D</td>
</tr>
<tr>
<td>LVTTL 3.3V</td>
<td>LVTTL33</td>
</tr>
<tr>
<td>LVTTL 3.3V differential</td>
<td>LVTTL33D</td>
</tr>
<tr>
<td>LVCMOS 3.3V</td>
<td>LVCMOS33</td>
</tr>
<tr>
<td>LVCMOS 3.3V Differential</td>
<td>LVCMOS33D</td>
</tr>
<tr>
<td>LVCMOS 2.5V</td>
<td>LVCMOS25</td>
</tr>
<tr>
<td>LVCMOS 2.5V Differential</td>
<td>LVCMOS25D</td>
</tr>
<tr>
<td>LVCMOS 1.8V</td>
<td>LVCMOS18</td>
</tr>
<tr>
<td>LVCMOS 1.8V High Speed</td>
<td>LVCMOS18H</td>
</tr>
<tr>
<td>LVCMOS 1.5V</td>
<td>LVCMOS15</td>
</tr>
<tr>
<td>LVCMOS 1.5V High Speed</td>
<td>LVCMOS15H</td>
</tr>
<tr>
<td>LVCMOS 1.2V</td>
<td>LVCMOS12</td>
</tr>
<tr>
<td>LVCMOS 1.2V High Speed</td>
<td>LVCMOS12H</td>
</tr>
<tr>
<td>LVCMOS 1.0V</td>
<td>LVCMOS10</td>
</tr>
<tr>
<td>LVCMOS 1.0V High Speed</td>
<td>LVCMOS10H</td>
</tr>
<tr>
<td>LVCMOS 1.0V Referenced</td>
<td>LVCMOS10R</td>
</tr>
</tbody>
</table>
6.2. PULLMODE
The PULLMODE attribute can be enabled for each I/O independently. This attribute is available for all the LVTLL and LVCMOS inputs and bidirectional I/O.
Values: UP, DOWN, NONE, I3C, KEEPER, FAILSAFE
Default: DOWN for standards mentioned above. Others defaulted to NONE.

Note:
1. FAILSAFE is only available for LVDS input. PULLMODE in FAILSAFE mode enables the pull-up for the P input and pull-down for the N input in LVDS.

6.3. CLAMP
The CLAMP option can be enabled for each I/O independently.
Values: ON, OFF
Default: For OUTPUT=OFF.
For INPUT=ON if $V_{CCIO}$ is the same as the I/O standard.
For INPUT=OFF if $V_{CCIO}$ is some other value than the I/O standard.

6.4. HYSTERESIS
The hysteresis option can be used to change the amount of hysteresis for the LVTTL and LVCMOS input and bidirectional I/O standards. LVCMOS12/12H and LVCMOS10/10H do not support hysteresis.
Values: ON, NA
Default: ON for LVTTL and LVCMOS15/18/33 for input and bidirectional standards. Others defaulted to NA.

6.5. VREF
The VREF option is enabled for referenced LVCMOS10 as well as referenced input buffers such as HSTL, SSTL, and HSUL.
Values: OFF, VREF1_LOAD, VREF2_LOAD
Default: VREF1_LOAD for standards mentioned above. Others defaulted to OFF.

6.6. OPENDRAIN
The OPENDRAIN option is available for all LVTTL and LVCMOS.
An I/O can be assigned independently to be an open drain when this attribute is turned on.
Values: OFF, ON
Default: OFF

6.7. SLEWRATE
Each I/O pin has an individual slew rate control. This allows the user to specify slew rate control on a pin-by-pin basis.
Slew rate control is not a valid attribute for inputs.
Values: SLOW, MED, FAST, NA
Default: SLOW
Hardware default: SLOW
6.8. DIFFRESISTOR
This attribute is used to provide differential termination. It is available only for differential I/O types.
Values: OFF, 100
Default: 100

6.9. TERMINATION
The I/O supports single-ended input parallel termination to $V_{CCIO}/2$. All input parallel terminations use a Thevenin termination scheme.
Values: OFF, 40, 50, 60, 75
Default: OFF

6.10. DRIVE STRENGTH
The DRIVE STRENGTH attribute is available for the output and bidirectional I/O standards. The default drive value depends on the I/O standard used.

Table 6.2. Drive Strength Values

<table>
<thead>
<tr>
<th>Output Standard</th>
<th>Drive</th>
<th>DiffDrive</th>
<th>$V_{CCIO}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single Ended Interfaces</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVTTL33</td>
<td>2 mA, 4 mA, 8 mA, 12 mA, 16 mA, 50RS</td>
<td>—</td>
<td>3.3</td>
</tr>
<tr>
<td>LVCMOS33</td>
<td>2 mA, 4 mA, 8 mA, 12 mA, 16 mA, 50RS</td>
<td>—</td>
<td>3.3</td>
</tr>
<tr>
<td>LVCMOS25</td>
<td>2 mA, 4 mA, 8 mA, 12 mA, 50RS</td>
<td>—</td>
<td>2.5</td>
</tr>
<tr>
<td>LVCMOS18</td>
<td>2 mA, 4 mA, 8 mA, 50RS</td>
<td>—</td>
<td>1.8</td>
</tr>
<tr>
<td>LVCMOS18H</td>
<td>2 mA, 4 mA, 8 mA, 12 mA, 50RS</td>
<td>—</td>
<td>1.8</td>
</tr>
<tr>
<td>LVCMOS15</td>
<td>2 mA, 4 mA</td>
<td>—</td>
<td>1.5</td>
</tr>
<tr>
<td>LVCMOS15H</td>
<td>2 mA, 4 mA, 8 mA</td>
<td>—</td>
<td>1.5</td>
</tr>
<tr>
<td>LVCMOS12</td>
<td>2 mA, 4 mA</td>
<td>—</td>
<td>1.2</td>
</tr>
<tr>
<td>LVCMOS12H</td>
<td>2 mA, 4 mA, 8 mA</td>
<td>—</td>
<td>1.2</td>
</tr>
<tr>
<td>LVCMOS10H</td>
<td>2 mA, 4 mA</td>
<td>—</td>
<td>1</td>
</tr>
<tr>
<td>LVTTL33 (Open Drain)</td>
<td>2 mA, 4 mA, 8 mA, 12 mA</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS33 (Open Drain)</td>
<td>2 mA, 4 mA, 8 mA, 12 mA</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS25 (Open Drain)</td>
<td>2 mA, 4 mA, 8 mA, 10 mA</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS18 (Open Drain)</td>
<td>2 mA, 4 mA, 8 mA</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS18H (Open Drain)</td>
<td>2 mA, 4 mA, 8 mA, 12 mA</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS15 (Open Drain)</td>
<td>2 mA, 4 mA</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS15H (Open Drain)</td>
<td>2 mA, 4 mA, 8 mA</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS12 (Open Drain)</td>
<td>2 mA, 4 mA</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS12H (Open Drain)</td>
<td>2 mA, 4 mA, 8 mA</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS10H (Open Drain)</td>
<td>2 mA, 4 mA</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>HSUL12</td>
<td>4 mA, 6 mA, 8 mA</td>
<td>—</td>
<td>1.2</td>
</tr>
<tr>
<td>HSTL15_1</td>
<td>8 mA</td>
<td>—</td>
<td>1.5</td>
</tr>
<tr>
<td>SSTL15_1</td>
<td>8 mA</td>
<td>—</td>
<td>1.5</td>
</tr>
<tr>
<td>SSTL15_2</td>
<td>10 mA</td>
<td>—</td>
<td>1.5</td>
</tr>
<tr>
<td>SSTL135_1</td>
<td>8 mA</td>
<td>—</td>
<td>1.35</td>
</tr>
<tr>
<td>SSTL135_2</td>
<td>10 mA</td>
<td>—</td>
<td>1.35</td>
</tr>
<tr>
<td>Differential Interfaces</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVDS</td>
<td>—</td>
<td>3.5 mA</td>
<td>1.8</td>
</tr>
<tr>
<td>SLVS</td>
<td>—</td>
<td>2.0 mA</td>
<td>—</td>
</tr>
</tbody>
</table>
### Output Standard

<table>
<thead>
<tr>
<th>Output Standard</th>
<th>Drive</th>
<th>DiffDrive</th>
<th>$V_{CCIO}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SUBLVDS</td>
<td>8 mA</td>
<td>—</td>
<td>1.8</td>
</tr>
<tr>
<td>SUBLVDSH</td>
<td>8 mA</td>
<td>—</td>
<td>1.8</td>
</tr>
<tr>
<td>LVDS</td>
<td>8 mA</td>
<td>—</td>
<td>2.5</td>
</tr>
<tr>
<td>HSUL12D</td>
<td>4 mA, 6 mA, 8 mA</td>
<td>—</td>
<td>1.2</td>
</tr>
<tr>
<td>HSTL15D_I</td>
<td>8 mA</td>
<td>—</td>
<td>1.5</td>
</tr>
<tr>
<td>SSTL15D_I</td>
<td>8 mA</td>
<td>—</td>
<td>1.5</td>
</tr>
<tr>
<td>SSTL15D_II</td>
<td>10 mA</td>
<td>—</td>
<td>1.5</td>
</tr>
<tr>
<td>SSTL135D_I</td>
<td>8 mA</td>
<td>—</td>
<td>1.35</td>
</tr>
<tr>
<td>SSTL135D_II</td>
<td>10 mA</td>
<td>—</td>
<td>1.35</td>
</tr>
<tr>
<td>LVTTL33D</td>
<td>8 mA, 2 mA, 4 mA, 12 mA, 50RS</td>
<td>—</td>
<td>3.3</td>
</tr>
<tr>
<td>LVCMOS33D</td>
<td>8 mA, 2 mA, 4 mA, 12 mA, 50RS</td>
<td>—</td>
<td>3.3</td>
</tr>
<tr>
<td>LVCMOS25D</td>
<td>8 mA, 2 mA, 4 mA, 12 mA, 50RS</td>
<td>—</td>
<td>2.5</td>
</tr>
</tbody>
</table>

### Note:

1. 50RS is an additional drive strength setting to mitigate reflection issues when driving an unterminated open transmission line trace of 50 Ω. It is only offered for 3.3 V, 2.5 V, and 1.8 V LVCMOS outputs.
2. For Output Standards that have multiple drive values, the default drive values are bolded.

### 6.11. LOC

This attribute can be used to make pin assignments to the I/O ports in the design. This attribute is used only when the pin assignments are made in HDL source code.

### 6.12. DIN/DOUT

This attribute can be used when an I/O register needs to be assigned. Using DIN asserts an input register and using DOUT asserts an output register in the design. By default, the software will attempt to assign the I/O registers if applicable. Users can turn this OFF by using a synthesis attribute. These attributes can only be applied to registers.
## Appendix A. sysI/O Attribute Examples

### IO_TYPE

**VHDL:**
```
ATTRIBUTE IO_TYPE: string;
ATTRIBUTE IO_TYPE OF portA: SIGNAL IS "LVCMOS18";
ATTRIBUTE IO_TYPE OF portB: SIGNAL IS "LVCMOS33";
ATTRIBUTE IO_TYPE OF portC: SIGNAL IS "SSTL15_II";
ATTRIBUTE IO_TYPE OF portD: SIGNAL IS "LVCMOS25";
```

**Verilog:**
```
output [4:0] portA /* synthesis IO_TYPE="LVCMOS33" DRIVE="16" PULLMODE="UP" SLE- WRATE="FAST"*/;
```

### OPENRAIN

**VHDL:**
```
ATTRIBUTE OPENDRAIN: string;
ATTRIBUTE OPENDRAIN OF q_lvttl33_17: SIGNAL IS "ON";
```

**Verilog:**
```
output [4:0] portA /* synthesis attribute OPENDRAIN of q_lvttl33_17 is ON */;
```

### DRIVE

**VHDL:**
```
ATTRIBUTE DRIVE: string;
ATTRIBUTE DRIVE OF portD: SIGNAL IS "8";
```

**Verilog:**
```
output [4:0] portA /* synthesis DRIVE = "8" */;
```

### DIFFDRIVE

**VHDL:**
```
ATTRIBUTE DIFFDRIVE: string;
ATTRIBUTE DIFFDRIVE OF portF: SIGNAL IS "3.5";
```

**Verilog:**
```
output [4:0] portF/* synthesis IO_TYPE="LVDS" DIFFDRIVE="3.5" */;
```

### TERMINATION

**VHDL:**
```
ATTRIBUTE TERMINATION: string;
ATTRIBUTE TERMINATION OF portF: SIGNAL IS "50";
```

**Verilog:**
```
output [4:0] portA /* synthesis IO_TYPE="SSTL18_I" TERMINATION = "50"*/;
```

### DIFFRESISTOR

**VHDL:**
```
ATTRIBUTE DIFFRESISTOR: string;
ATTRIBUTE DIFFRESISTOR OF portF: SIGNAL IS "100";
```

**Verilog:**
```
output [4:0] portA /* synthesis IO_TYPE="LVDS" DIFFRESISTOR = "100"*/;
```
PULLMODE

VHDL:
ATTRIBUTE PULLMODE: string;
ATTRIBUTE PULLMODE OF portF: SIGNAL IS "PULLUP";

Verilog:
output [4:0] portA /* synthesis IO_TYPE="LVCMOS33" PULLMODE = "PULLUP"*/;

SLEWRATE

VHDL:
ATTRIBUTE SLEWRATE: string;
ATTRIBUTE SLEWRATE OF portF: SIGNAL IS "FAST";

Verilog:
output [4:0] portA /* synthesis IO_TYPE="LVCMOS33" SLEWRATE = "FAST"*/;

CLAMP

VHDL:
ATTRIBUTE CLAMP: string;
ATTRIBUTE CLAMP OF portF: SIGNAL IS "ON";

Verilog:
output [4:0] portA /* synthesis IO_TYPE="LVCMOS33" CLAMP = "ON"*/;

HYSTERESIS

VHDL:
ATTRIBUTE HYSTERESIS: string;
ATTRIBUTE HYSTERESIS OF portF: SIGNAL IS "ON";

Verilog:
output [4:0] portA /* synthesis IO_TYPE="LVCMOS25" HYSTERESIS = "ON"*/;

LOC

VHDL:
ATTRIBUTE LOC: string;
ATTRIBUTE LOC OF output_vector: SIGNAL IS "H5";

Verilog:
Input rst /* synthesis LOC="H5" */;

VREF

To set User Vref Locate:
1. After opening the design project, choose Tools > Device Constraint Editor.
2. Select the Global tab at the bottom of the view.
3. Double-click the cell beside Vref Locate. A dialog box opens.
4. For each available site, click on the desired row and enter a unique name in the VREF Name field.

Syntax

dl_create_vref -name <vref_name> -site <site_value>

where:
<vref_name> = string
<site_value> = already pre-filled by Radiant.

For more details regarding I/O type, see the sysI/O User Guide for the target device family.

Example:
This constraint assigns a custom site name TEST_SITE to the selected site.
dl_create_vref -name TESTING_SITE 8
Appendix B. sysI/O Buffer Design Rules

- Only one VCCIO level is allowed in a given bank. As such, all IO_TYPES of that bank should be compatible with the VCCIO level.
- Banks at the top left, and right side of the device can only support single-ended I/O.
- Bottom banks support differential inputs and outputs as well as single-ended I/O.
- When an output is configured as an OPENDRAIN, the PULLMODE is set to NONE and the CLAMP setting is set to OFF.
- For bidirectional ports, pull-up and pull-down are allowed. The PULLMODE is set to NONE by default.
- When an output is configured as an OPENDRAIN, it can be placed independent of VCCIO.
- When a ratioed input buffer is placed in a bank with a different VCCIO (mixed mode), the Pull mode options of Up are no longer available.
- The IO_TYPE attribute for a differential buffer can only be assigned to the TRUE pad. The Lattice Radiant® design tool automatically assigns the other I/O of the differential pair to the complementary pad.
- DIFFRESISTOR termination is available on all sysI/O pairs of bottom banks.
- If none of the pins are used for a given bank, the VCCIO of the bank should be grounded except for the JTAG bank.
Appendix C. sysI/O Attributes using the Lattice Radiant Device Constraint Editor User Interface

sysI/O buffer attributes can be assigned using the Device Constraint Editor in the Lattice Radiant software. The Port Assignments Sheet lists all the ports in a design and all the available sysI/O attributes in multiple columns. Click on each of these cells for a list of all the valid I/O preferences for that port. Each column takes precedence over the next. Therefore, when user chooses a particular IO_TYPE, the columns for the PULLMODE, DRIVE, SLEWRATE, and other attributes list only the valid entries for that IO_TYPE.

Pin locations can be locked by using the Pin column of the Port Tab Sheet or by using the Pin Tab Sheet. User can right-click on a cell and go to Assign Pins to see a list of available pins.

In Device Constraint Editor, go to Design > Constraint DRC to look for incorrect pin assignments.

All the preferences assigned using the Device Constraint Editor are written into the post synthesis constraint file (.pdc).

Figure C.1 shows the Port Sheet of Device Constraint Editor. For further information on how to use Device Constraint Editor, refer to the Lattice Radiant Help documentation, available in the Help menu option of the software.

<table>
<thead>
<tr>
<th>Name</th>
<th>Group</th>
<th>Pin</th>
<th>IO_TYPE</th>
<th>CLAMP</th>
<th>DIFFRING</th>
<th>DIFFSPLIT</th>
<th>DRIVE</th>
<th>QUICKFILTER</th>
<th>HIGHZ</th>
<th>LOWZ</th>
<th>PULLMODE</th>
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</table>

Figure C.1. Port Tab of Device Constraint Editor
References

For more information, refer to:

- CrossLink-NX Family Data Sheet (FPGA-DS-02049)
- CrossLink-NX-33 and CrossLinkU-NX Data Sheet (FPGA-DS-02104)
- CertusPro-NX Family Data Sheet (FPGA-DS-02086)
- Certus-NX Family Data Sheet (FPGA-DS-02078)
- MachXO5-NX Family Data Sheet (FPGA-DS-02102)
- Lattice Nexus Platform web page

For more information on Nexus-related IP, reference designs, and board documents, refer to the following web pages:

- IP and Reference Designs for CrossLink-NX
- Development Kits and Boards for CrossLink-NX
- IP and Reference Designs for CertusPro-NX
- Development Kits and Boards for CertusPro-NX
- IP and Reference Designs for Certus-NX
- Development Kits and Boards for Certus-NX
- IP and Reference Designs for MachXO5-NX
- Development Kits and Boards MachXO5-NX

A variety of technical notes for Lattice Nexus devices are available:

- CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097)
- CrossLink-NX-33 and CrossLinkU-NX High-Speed I/O Interface (FPGA-TN-02280)
- CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244)
- Certus-NX High-Speed I/O Interface (FPGA-TN-02216)
- MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286)
- Power Management and Calculation for CrossLink-NX Devices (FPGA-TN-02075)
- Power Management and Calculation for Certus-NX, CertusPro-NX, and MachXO5-NX (FPGA-TN-02257)

Other references:

- Lattice Insights for Lattice Semiconductor training courses and learning plans
- Lattice Radiant FPGA design software
Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/en/Support/AnswerDatabase.
# Revision History

**Revision 2.4, July 2024**

<table>
<thead>
<tr>
<th>Section</th>
<th>Change Summary</th>
</tr>
</thead>
</table>
| sysI/O Banking Scheme            | • In the CrossLink-NX, Certus-NX, and CertusPro-NX Devices section:  
  • changed For the 40k, 50k, and 100k devices, there is one bank on top, two banks each on the left and right side of the device, and three on the bottom side of the device to  
  For the 28k, 40k, 50k, and 100k devices, there is one bank on top, two banks each on the left and right side of the device, and three on the bottom side of the device;  
  • changed For the 17k device, there is one bank on top, one on the right side, and three on the bottom side of the device to  
  For the 9k and 17k device, there is one bank on top, one on the right side, and three on the bottom side of the device.  
  • In Figure 3.1. CrossLink-NX, Certus-NX, CertusPro-NX sysI/O Banking, changed the note from Banks not available in 17k devices to Banks not available in 9k and 17k devices. |

---

**Revision 2.3, June 2024**

<table>
<thead>
<tr>
<th>Section</th>
<th>Change Summary</th>
</tr>
</thead>
</table>
| All                              | • Changed MachXO5-NX 25 to LFMXO5-25 globally.  
  • Changed MachXO5-NX 100T/55T to LFMXO5-100T/LFMXO5-55T globally. |
| sysI/O Banking Scheme            | • Added LFMXO5-15D device to:  
  • the following paragraph in MachXO5-NX Devices:  
  The LFMXO5-25/LFMXO5-15D devices have ten GPIO banks. There are two banks on top, three banks each on the left and right side of the device, and two on the bottom side of the device;  
  • caption of Figure 3.2. LFMXO5-25/LFMXO5-15D sysI/O Banking;  
  • headers of VCCIO [0,1,2,3,4,7,8,9] Wide Range for LFMXO5-25/LFMXO5-15D (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V) and VCCIO [5,6] High Performance for LFMXO5-25/LFMXO5-15D (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V) sections.  
  • Added LFMXO5-55TD device to:  
  • the following paragraph in MachXO5-NX Devices:  
  The LFMXO5-100T/LFMXO5-55T/LFMXO5-55TD devices have eight GPIO banks. There is one bank on top, two banks each on the left and right side of the device, and three on the bottom side of the device;  
  • caption of Figure 3.3. LFMXO5-100T/LFMXO5-55T/LFMXO5-55TD sysI/O Banking;  
  • headers of VCCIO [0,1,2,6,7] Wide Range for LFMXO5-100T/LFMXO5-55T/LFMXO5-55TD (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V) and VCCIO [3,4,5] High Performance for LFMXO5-100T/LFMXO5-55T/LFMXO5-55TD (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V) sections. |
| VCCO Requirement for I/O Standards | Added table notes on mixed mode in Table 4.1. Input Mixed Mode\(^4\) for Wide Range Input Buffers and Table 4.2. Input Mixed Mode\(^3\) for High-Performance Input Buffers. |
| Software sysI/O Attributes       | • Added PULLMODE in FAILSAFE mode enables the pull-up for the P input and pull-down for the N input in LVDS to the note in the PULLMODE section.  
  • Table 6.2. Drive Strength Values:  
  • removed 8 mA from the drive values for LVCMOS15, LVCMOS12, LVCMOS10H, LVCMOS15 (Open Drain), LVCMOS12 (Open Drain), and LVCMOS10H (Open Drain);  
  • added a table note on the default drive value. |
| sysI/O Buffer Design Rules       | • Added For bidirectional ports, pull-up and pull-down are allowed. The PULLMODE is set to NONE by default. |
### Revision 2.2, October 2023

<table>
<thead>
<tr>
<th>Section</th>
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<tr>
<td>All</td>
<td>Changed CrossLink-NX-33U to CrossLinkU-NX.</td>
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### Revision 2.1, August 2023

<table>
<thead>
<tr>
<th>Section</th>
<th>Change Summary</th>
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<tbody>
<tr>
<td>Introduction</td>
<td>Updated reference to the combined CrossLink-NX-33 and CrossLinkU-NX Data Sheet.</td>
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</tbody>
</table>
| sysI/O Banking Scheme    | • Corrected banks in the VCCIO [0, 1, 3] Wide Range (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V) and VCCIO [2, 3, 4] High Performance (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V) sections.  
  • Added the CrossLinkU-NX section. |
| sysI/O Buffer Configurations | Added reference to the combined CrossLink-NX-33 and CrossLinkU-NX Data Sheet in the Soft MIPI D-PHY Support section. |
| References               | Updated reference to the combined CrossLink-NX-33 and CrossLinkU-NX Data Sheet. Added references to web pages and other documents. |

### Revision 2.0, August 2023

<table>
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<tr>
<td>sysI/O Banking Scheme</td>
<td>Updated Figure 3.5. High-Performance sysI/O Buffer Pair for Bottom Side to show that the Outputs of the Single Ended Drivers are connected to (+) Referenced Input Comparator and Input Buffers.</td>
</tr>
<tr>
<td>Software sysI/O Attributes</td>
<td>In Table 6.2. Drive Strength Values, added I/O Type SSTL135_1 and SSTL135_II.</td>
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<tr>
<td>References</td>
<td>Added this section.</td>
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### Revision 1.9, February 2023

<table>
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<tbody>
<tr>
<td>All</td>
<td>Minor adjustments in formatting across the document.</td>
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</table>
| sysI/O Banking Scheme    | • Added MachXOS-NX 25 and MachXOS-NX 100T/55T information, including Figure 3.3. LFMXOS-100T/LFMXOS-55T/LFMXOS-55TD sysI/O Banking, VCCIO [0, 1, 2, 6, 7] Wide Range for LFMXOS-100T/LFMXOS-55T/LFMXOS-55TD (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V), and VCCIO [1, 4, 5] High Performance for LFMXOS-100T/LFMXOS-55T/LFMXOS-55TD (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V).  
  • Updated Figure 3.6. High-Performance sysI/O Buffer Pair for Bottom Side to add missing connection on the SE drive input. |
| Software sysI/O Attributes | Updated PULLMODE section to add KEEPER value and note reference for FAILSAFE. |

### Revision 1.8, December 2022

<table>
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<td>Software sysI/O Attributes</td>
<td>Changed the default value of the attribute from OFF to 100 in the DIFFRESISTOR section.</td>
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<tr>
<td>Technical Support Assistance</td>
<td>Added reference link to Lattice Answer Database.</td>
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### Revision 1.7, August 2022

<table>
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<th>Section</th>
<th>Change Summary</th>
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| sysI/O Banking Scheme    | • Removed reference to the 125k device from the CrossLink-NX, Certus-NX, and CertusPro-NX sections.  
  • Removed reference to MachXOS-NX 55k device from the MachXOS-NX section. Revised banking description and Figure 3.2.  
  • Corrected title of the referenced document to Power Management and Calculation for CrossLink-NX Devices (FPGA-TN-02075). |
## Revision 1.6, June 2022

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<td>Added CrossLink-NX-33 support.</td>
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## Revision 1.5, December 2021

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<td>Added MachXO5-NX support.</td>
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## Revision 1.4, October 2021

<table>
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</table>
| Software sysI/O Attributes    | • In the PULLMODE section, changed Default to DOWN for standards mentioned above. Others defaulted to NONE.  
• In HYSTERESIS section, changed Default to ON for LVTTL, and LVCMOS15/18/33 for input and bidirectional standards. Others defaulted to NA.  
• Minor editorial changes. |

## Revision 1.3, June 2021

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<tr>
<td>All</td>
<td>Added references to the CertusPro-NX data sheet and technical notes.</td>
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| sysI/O Banking Scheme          | • Updated section introduction.  
• Updated footnote in Figure 3.1. sysI/O Banking.  
• Updated Figure 3.3. Wide Range sysI/O Buffer for Top, Left/Right Side. |

## Revision 1.2, November 2020

<table>
<thead>
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<th>Section</th>
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<td>Introduction</td>
<td>Added references to data sheets and removed some statements.</td>
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<tr>
<td>sysI/O Overview</td>
<td>Added this section.</td>
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</table>
| sysI/O Banking Scheme          | • Updated introductory paragraph.  
• Updated headings of sub-sections 3.2 and 3.3.                               |
| sysI/O Buffer Configurations   | Updated Programmable Clamp section.                                          |
| Software sysI/O Attributes     | Deleted Preference Editor from DIN/DOUT description.                          |
| Appendix A. sysI/O Attribute Examples | • Updated default of PULLMODE and CLAMP attributes.  
• Updated values of TERMINATION attribute.  
• Updated subheading to DRIVE STRENGTH. |
| All                            | Minor adjustments in formatting/style.                                        |

## Revision 1.1, June 2020

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| All                            | • Updated document title to sysI/O Usage Guide for Nexus Platform.  
• Added Nexus platform (which includes CrossLink-NX and Certus-NX) support. |
| sysI/O Banking Scheme          | • Updated note in Figure 3.1.  
• Added the High Performance sysI/O Buffer Pairs (On Bottom Side) and Wide Range sysI/O Buffer Pair (On Top, Left/Right Sides) sections.  
• Added references in Standby section. |
| sysI/O Buffer Configurations   | Added the Soft MIPI D-PHY Support section.                                    |
| Appendix A. sysI/O Attribute Examples | Added this section.                                                             |
| Appendix B. sysI/O Buffer Design Rules | Added this section.                                                           |
## Change Summary

### Section

**Appendix C. sysI/O Attributes using the Lattice Radiant Device Constraint Editor User Interface**

- Added this section.

### Revision 1.0, November 2019

<table>
<thead>
<tr>
<th>Section</th>
<th>Change Summary</th>
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</thead>
<tbody>
<tr>
<td>All</td>
<td>Initial release</td>
</tr>
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</table>