Solder Reflow Guide for Surface Mount Devices

Technical Note

FPGA-TN-02041 Version 3.8

November 2017

Contents

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
BGA	Ball Grid Array
caBGA	Chip Array BGA
csBGA	Chip-Scale BGA
DI	Deionized
fcBGA	Flip Chip BGA
fpBGA	Fine Pitch BGA
ftBGA	Thin BGA
IPC	Association Connecting Electronics Industries
JEDEC	JEDEC Solid State Technology Association
PCB	Printed circuit board
PPM	Parts per million
QFNS	Quad Flat Pack Saw-Singulated
RoHS	Restriction of Use of Hazardous Substances
SMT	Surface-mount technology (assembling and mounting technology)
TQFP	Thin Quad Flat Pack
TS	Technical Specification
ucBGA	Ultra Chip-Scale BGA
WLCSP	Wafer Level Chip Scale Package

1. Introduction

This technical note provides general guidelines for solder reflow and rework process for Lattice Semiconductor surface mount products. The data used in this document is based on IPC/JEDEC (Association Connecting Electronics Industries/JEDEC Solid State Technology Association) standards. Each board has its own profile which depends upon the reflow equipment used and the board design. The PCB (printed circuit board) must be individually characterized to find the reliable profile. This document covers Sn/Pb (Tin/Lead), Pb-Free (Lead-Free), and Halogen-Free processes.

2. Reflow

- Use caution when profiling to insure that the maximum temperature difference between components is less than 10 °C (7 °C within an individual component).
- Forced convection reflow with nitrogen is preferred (with maximum oxygen content of 50-75 PPM). Select an appropriate heat sink and thermal interface material for the package.

3. Inspection

- Pre-reflow: Use visual inspection to verify solder paste dispense location and quantity.
- Pick and place: Use machine vision as necessary to ensure proper component placement.
- Post reflow: Use electrical testing to verify solder joint formation (100% post-reflow visual inspection is not recommended).

4. Cleaning Recommendations

- After solder reflow, printed circuit boards should be thoroughly cleaned and dried using standard cleaning equipment.
- Final rinse should be warm deionized (DI) water (50 °C to 75 °C) with resistivity of 0.2 MΩ /cm or greater.
- After cleaning, the boards should be baked for a minimum of one hour at 125 °C to evaporate residual moisture.

5. Rework Recommendations

Removal and replacement of SMT (surface-mount technology) packages on PCBs is fairly straightforward. However, reattachment or touch-up of SMT packages that have already been soldered to the board is not practical in most cases.

A few important criteria should be considered when choosing a rework system:

- Minimize the change in temperature across the solder joint array to promote good solder joint formation, minimize intermetallic growth, improve solderability and minimize component warpage.
- Minimize die temperature to prevent die delamination and wire bond failure.
- Minimize board temperature adjacent to the rework site to reduce intermetallic growth, prevent secondary reflow, and prevent possible component delamination.
- For boards with no internal ground plane, apply localized heat to the SMT package. When the solder is molten, remove package using appropriate vacuum tool.
- While the board is still hot, remove excess solder from the site using a vacuum desoldering system or a soldering iron and solder wicking material. Use care to avoid damaging the solder pads or the surrounding solder mask.
- For PCBs with internal ground plane(s), preheat the entire board to at least 80 °C before removing the SMT packages.
- Use alcohol to remove residual flux, then wash the entire board using the standard board cleaning process before attempting to replace SMT components.

6. BGA Reballing

BGA reballing is not recommended. Reballed BGA packages void the original Lattice specifications.

7. Pb-Free/Halogen-Free (RoHS-Compliant) Products

All Lattice Pb-Free products are also fully RoHS compliant. Similarly, all Lattice Halogen-free products are also Pb-Free and RoHS compliant. Lattice offers a broad range of Pb-Free and Halogen-Free (RoHS-compliant) products in a variety of package configurations. These packages include the Thin Quad Flat Pack (TQFP), Quad Flat Pack Saw-Singulated (QFNS), Fine Pitch BGA (fpBGA), Thin BGA (ftBGA), Chip-Scale BGA (csBGA), Ultra Chip-Scale BGA (ucBGA), Chip Array BGA (caBGA) and Flip Chip BGA (fcBGA), Chip Array BGA (caBGA), Flip Chip BGA (fcBGA) and Wafer Level Chip Scale Package(WLCSP).

8. Peak Reflow Temperature (T_P) by Package Size

Table 8.1 illustrates the peak reflow temperatures by package size. Refer to the Package Diagrams document and use maximum package dimensions to determine package thickness and volume.

Table 8.1. Peak Reflow Temperature (T_P)

Classification	Package Thickness	Volume < 350 mm^3	Volume = 350–2000 mm^3	Volume > 2000 mm^3
SnPb Package	< 2.5 mm	240 + 0/–5 °C	225 + 0/–5 °C	
	≤ 2.5 mm	225 + 0/–5 °C		
Pb-Free and Halogen-Free Packages	< 1.6 mm	260 + 0/–5 °C		
	1.6 mm to < 2.5 mm	260 + 0/–5 °C	250 + 0/–5 °C	245 + 0/–5 °C
	≤ 2.5 mm	250 + 0/–5 °C	245 + 0/–5 °C	

Note:
Package volume excludes external terminals (balls, bumps, lands, leads) and non-integral heat sinks.

Table 8.2 shows the peak reflow temperature for Lattice devices by package type and size.

Table 8.2. Peak Reflow Temperature (T_P) by Package Type and Size

Package Type	Number of Lead/Balls	SnPb Package		Pb-Free / Halogen-Free Package (RoHS Compliant)	
		Moisture Sensitivity Level	Peak Reflow Temp. (+0/–5 °C)	Moisture Sensitivity Level	Peak Reflow Temp. (+0/–5 °C)
caBGA	49	3	240	Not Available	
	100	3	240	Not Available	
	256	3	240	3	260
	324	Not Available		3	260
	332	Not Available		3	260
	381	Not Available		3	260
	400	Not Available		3	260
	554	Not Available		3	260
	756	Not Available		3	260
csBGA	56	3	240	3	260
	64	Not Available		3	260
	81	Not Available		3	260
	100	3	240	3	260
	121	Not Available			260
	132	3	240	3	260
	144	Not Available		3	260
	184	Not Available		3	260
	328	Not Available		3	260
csfBGA	121	Not Available		3	260
	256	Not Available		3	260
	285	Not Available		3	260
	324	Not Available		3	260
ucBGA	36	Not Available		3	260
	49	Not Available		3	260
	64	Not Available		3	260
	81	Not Available		3	260
	121	Not Available		3	260
	132	Not Available		3	260
	225	Not Available		3	260

Package Type	Number of Lead/Balls	SnPb Package		Pb-Free / Halogen-Free Package (RoHS Compliant)	
		Moisture Sensitivity Level	Peak Reflow Temp. (+0/–5 °C)	Moisture Sensitivity Level	Peak Reflow Temp. (+0/–5 °C)
ucfBGA	36	Not Available		3	260
fcBGA	1020	4	225	4	245
	1152	4	225	4	245
	1704	4	225	4	245
fpBGA	100	3	240	3	260
	144	3	240	Not Available	
	208	3	225	3	250
	256	3	225	3	250
	388	3	225	3	250
	416	3	225	Not Available	
	484	3	225	3	250
	516	3	225	3	250
	672	3	225	3	250
	676	3	225	Not Available	
	680	3	225	3	250
	900	3	225	3	250
	1152	3	225	3	250
	1156	3	225	3	250
fpSBGA	680	3	225	Not Available	
ftBGA	208	Not Available		3	260
	256 (Option 1)[1]	3	225	3	260
	256 (Option 2)[2]	Not Available		3	250
	324	3	225	260	260
TQFP (Thickness: 1.4 mm)	48	3	240	3	260
	64	3	240	3	260
	100	3	240	3	260
	128	3	240	3	260
	144	3	256	3	260
	176	3	256	3	260
TQFP (Thickness: 1.0 mm)	44	3	240	3	260
	48	3	240	3	260
	100	Not Available		3	260
BGA	256	3	225	Not Available	
	272	3	225	Not Available	
	352	3	225	Not Available	
	388	3	225	Not Available	
PLCC	20	1	225	1	250
	28	1	225	1	245
	44	3	225	3	245
	68	3	225	Not Available	
	84	3	225	4	245
PQFP	100	3	225	3	245
	120	3	225	Not Available	
	128	3	225	3	245
	160	3	225	3	245

Package Type	Number of Lead/Balls	SnPb Package		Pb-Free / Halogen-Free Package (RoHS Compliant)	
		Moisture Sensitivity Level	Peak Reflow Temp. (+0/–5 °C)	Moisture Sensitivity Level	Peak Reflow Temp. (+0/–5 °C)
	208	3	225	3	245
QFNS	24	Not Available		1	260
	32 (Option 1)	1	240	1	260
	32 (Option 2)[3]	Not Available		3	245
	36	Not Available		3	245
	48	Not Available		3	245
	64	Not Available		3	245
	84	Not Available		3	245
QFN	48	Not Available		3	260
SBGA	256	3	225	Not Available	
	320	3	225	Not Available	
	352	3	225	Not Available	
	432	3	225	Not Available	
SSOP	28	1	225	Not Available	
WLCSP	16	Not Available		1	260
	20	Not Available		1	260
	25	Not Available		1	260
	30	Not Available		1	260
	36 (Option 1)[4]	Not Available		1	260
	36 (Option 2)[5]	Not Available		1	250
	49	Not Available		1	250
	81	Not Available		1	250

Notes:

1. ispMACH® 4000, MachXO2™, MachXO™, LatticeXP2™
2. LatticeECP3™
3. MachXO2, iCE40™ LP384
4. iCE5™ LP
5. MachXO3L™

9. Reflow Profile for SMT Packages

The typical reflow process includes four phases.

1. Preheat – Brings the assembly from 25 °C to TS. During this phase the solvent evaporates from the solder paste. Preheat temperature ramp rate should be less than 2 °C/second to avoid solder ball spattering and bridging.
    - Solder Ball Spattering – The most common solder balling defect is spattering which is caused by explosive evaporation of solvents. It can be eliminated by a slower temperature rise in the preheat phase.
    - Bridging – Often seen on fine pitch components and usually caused by inaccurate or splashy screen printing. But it can also be a result of solder paste slumping caused by rapid temperature rise in the pre-heat phase.
2. Flux Activation – The temperature rises slowly and reaches a point at which the flux completely wets the surfaces to be soldered.
3. Reflow – In this phase, the temperature rises to a level sufficient to reflow the solder. The flux wicks surface oxides and contaminants away from the melted solder, resulting in a clean solder joint.
4. Cool Down – Ramp down rate should be as fast as possible in order to control grain size, but should not exceed 6 °C/second.

Table 9.1 and Figure 9.1 describe the reflow profile.

Table 9.1. Peak Reflow Temperature (T_P)

Parameter	Description	SnPb Package	Pb-Free and Halogen-Free Packages
Ramp-Up	Average Ramp-Up Rate (T_{SMAX} to T_P)	3 °C/second max.	3 °C/second max.
T_{SMIN}	Preheat Peak Min. Temperature	100 °C	150 °C
T_{SMAX}	Preheat Peak Max. Temperature	150 °C	200 °C
t_S	Time between T_{SMIN} and T_{SMAX}	60 seconds–120 seconds	60 seconds–120 seconds
T_L	Solder Melting Point	183 °C	217 °C
t_L	Time Maintained above T_L	60 seconds–150 seconds	60 seconds–150 seconds
t_P	Time within 5 °C of Peak Temperature	10 seconds–30 seconds	30 seconds
Ramp-Down	Ramp-Down Rate	6 °C/second max.	6 °C/second max.
t 25 °C to T_P	Time from 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

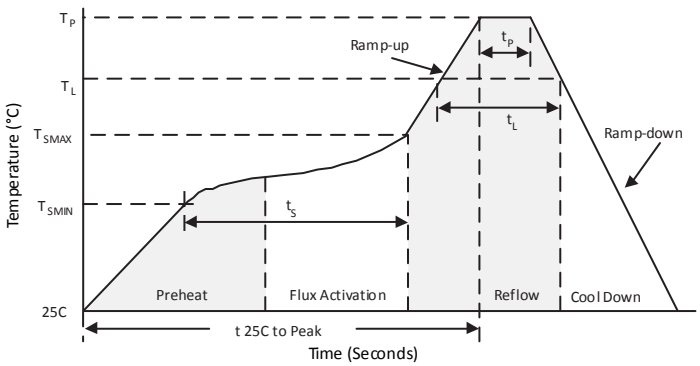

Figure 9.1. Thermal Reflow Profile

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
November 2017	3.8	• Updated Table 8.2. Peak Reflow Temperature (TP) by Package Type and Size. Changed Moisture Sensitivity Level value for csfBGA 285 Balls from 5 to 3. • Changed document ID from TN1076 to FPGA-TN-02041. • Updated document template. • Added Acronyms in This Document section. • Applied minor editorial changes.
January 2017	3.7	Updated Table 8.2. Peak Reflow Temperature (TP) by Package Type and Size. • Changed Moisture Sensitivity Level value for csfBGA 285 Balls from 3 to 5. • Added Moisture Sensitivity Level values for TQFP (Thickness: 1.4 mm) packages.
December 2016	3.6	Updated Table 8.2. Peak Reflow Temperature (TP) by Package Type and Size. Added WLCSP 30-ball package type.
June 2015	3.5	Updated Table 8.2. Peak Reflow Temperature (TP) by Package Type and Size. • Added caBGA package type for iCE40 Ultra. • Added QFN package type for iCE40 Ultra.
		Updated Technical Support Assistance section.
October 2014	3.4	Updated Table 8.2. Peak Reflow Temperature (TP) by Package Type and Size. • Added ucFBGA packages for ECP5. • Added csfBGA package type for ECP5.
	3.3	Updated Table 8.2. Peak Reflow Temperature (TP) by Package Type and Size. • Added caBGA packages for MachXO3L. • Added csfBGA package type for MachXO3L. • Added WLCSP packages for MachXO3L.
June 2014	3.2	Updated Pb-Free/Halogen-Free (RoHS-Compliant) Products section. Added packages.
		Updated Table 8.2. Peak Reflow Temperature (TP) by Package Type and Size. Added WLCSP package types for iCE40 Ultra.
May 2014	03.1	Updated Table 8.2. Peak Reflow Temperature (TP) by Package Type and Size. Added QFNS package type for MachXO2 and iCE40 LP384.
		Updated Table 9.1. Peak Reflow Temperature (TP). Updated the t_P parameter for Pb-Free and Halogen-Free packages based on J-STD-020D.1 standard.
		Updated Technical Support Assistance information.
August 2013	03.0	Updated Table 8.2. Peak Reflow Temperature (TP) by Package Type and Size.
February 2013	02.9	Updated Table 8.2. Peak Reflow Temperature (TP) by Package Type and Size.
August 2012	02.8	Updated document to support iCE40 mobile FPGA packaging: • 36, 49, 81, 121 and 225-ball ucBGA • 81 and 121-ball csBGA • 36 and 84-ball QFNS • 100-pin TQFP (1.0 mm thickness)
April 2012	02.7	Updated document to include the 328-ball csBGA package.
February 2012	02.6	Updated document with new corporate logo.
June 2011	02.5	Updated document to include 25 WLCSP package.
November 2010	02.4	Updated for Halogen-free package support.
June 2009	02.3	Updated QFN information in Table 8.2. Peak Reflow Temperature (TP) by Package Type and Size, SnPb Packages table.
		Updated QFN information in Table 8.2. Peak Reflow Temperature (TP) by Package Type and Size, Pb-Free Packages table.

Date	Version	Change Summary
April 2008	02.2	Updated Table 8.2. Peak Reflow Temperature (TP) by Package Type and Size.
		Previous Lattice releases.

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