

## Introduction

This application note provides a step-by-step procedure for simulating ispPAC<sup>®</sup>-POWR1208 designs developed in the PAC-Designer<sup>®</sup> LogiBuilder<sup>™</sup> system, covering the essential tools to edit a stimulus file and analyze the output. The procedure starts after a sequence has been compiled, with the editing of the default stimulus file, then moves to the review and analysis of the simulation output. Functional logic simulation is fully supported; however, neither high-speed timing simulations nor analog transient analysis are provided using PAC-Designer. Nevertheless, the software tools discussed in this application note add value to the process of design, simulation, and debug, for power supply sequence and monitoring.

Monitoring and sequencing power supplies is becoming more important as higher performance semiconductors require their multiple supplies to be brought on and off line in a certain and repeatable order. Specific power-up and power-down details are provided in the data sheets from numerous manufacturers. Lattice Semiconductor Corporation has made available several application notes that show how the ispPAC-POWR1208 can be used to disentangle many of these power sequencing designs. This application note discusses the essential details of simulation and analysis as outlined below.

- Start with a sequence that compiles successfully.
- Edit the default stimulus file using Waveform Editor.
- Modify the input clock.
- Add input signals and adjust the timing.
- Save the customized stimulus file.
- Launch the Simulator from PAC-Designer.
- View the simulator output using Waveform Viewer.
- Add waveforms to the display.
- Add internal signals to the display.
- Add the step counter to the display.
- Use the markers to analyze the output.
- Print the results.
- Save the display settings for the next simulation.

## ispPAC-POWR1208 Background

The ispPAC-POWR1208 is a complete, single-chip solution for monitoring and sequencing power supplies for circuit boards and systems with multiple voltages. Sixteen inputs are provided, of which twelve are analog inputs for monitoring power supply voltages and four are digital inputs for additional logic control. On the output side, a total of sixteen signals are also provided. Eight of the outputs are comparator outputs, four are digital, and four are configurable as either digital or programmable charge-pump outputs.

The charge pump outputs are programmable in both their constant-current output and maximum voltage. The constant current range is from 0.5 $\mu$ A to 50 $\mu$ A, and the maximum voltage can range from 8V to 12V. The outputs are designed to directly drive the gates of N-channel power FETs and can also be programmed as open-drain outputs.

The twelve analog inputs are connected directly to the non-inverting inputs of twelve comparators. Each comparator has a programmable voltage reference connected to the inverting input, which sets the trip point. The outputs of the comparators are used as inputs to the on-chip programmable logic device (PLD).

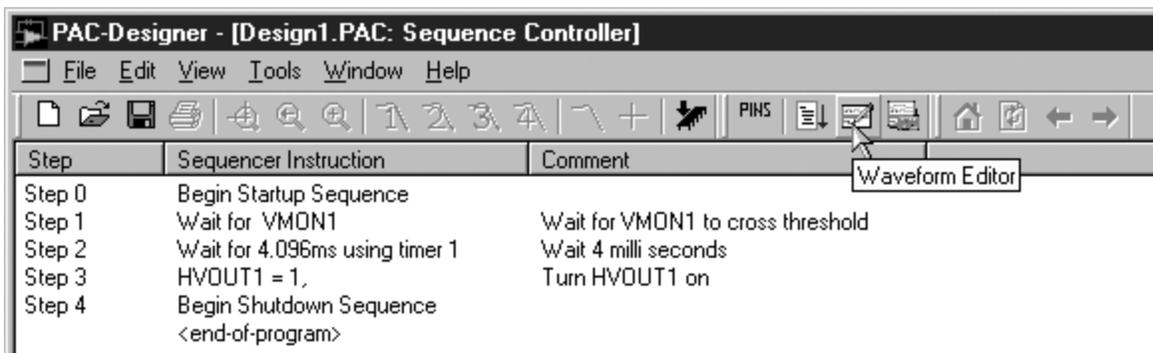
The “brain” of the ispPAC-POWR1208 consists of a 16-macrocell PLD, four programmable timers, and an on-chip clock generator. The outputs of the PLD control the ispPAC-POWR1208 outputs directly. The PLD can be programmed using PAC-Designer (Lattice’s easy-to-use Windows-based design software). LogiBuilder is a design environment within PAC-Designer that can be used to design, simulate, and program the PLD with a series of steps

based on the specific requirements of the application. This application note will focus on the stimulus and simulation aspects of using LogiBuilder.

## Editing the Stimulus File

The functional simulator reads two input files to produce one output file. One of the input files is the stimulus file and the other is the design file. The output file is a wave (\*.WAV) file that can be examined using the waveform editor that is included in the PAC-Designer 2.0 installation. To generate or edit a stimulus file, click on the **<Waveform Editor>** tool shown in Figure 14-1 or **Run Waveform Editor** from the **Tools** menu.” The Waveform Editor uses a data model called the Waveform Description Language (WDL). The language represents a waveform as a sequence of signal states separated by time intervals. The language also has constructs that let you express the waveform pattern hierarchically. However, you do not have to be familiar with the Waveform Description Language in order to use the Waveform Editor.

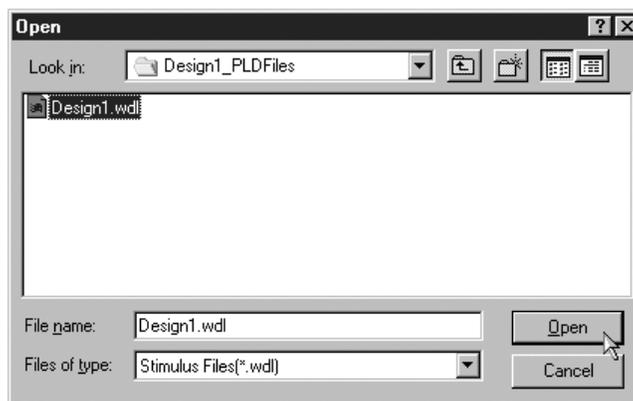
Figure 14-1. PAC-Designer LogiBuilder Window



## Opening the Default Stimulus File

Click on **Open...** from the **File** menu in the Waveform Editor to open the default stimulus file. In this application note, our design was named **Design1** and thus the file name of the default stimulus file is **Design1.wdl**, located in the **Design1\_PLDFiles** folder (Figure 14-2).

Figure 14-2. Opening the Default Stimulus File in the Waveform Viewer

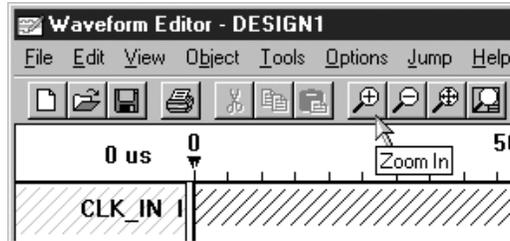


## Using the Zoom Tool and Cursor

The signal that is always defined in the default stimulus file is the input clock, named **CLK\_IN**. When a signal has more detail than can be displayed, the Waveform Editor will display it with cross-hatching as seen in Figure 14-3. Click the **<Zoom In>** tool (also shown in Figure 14-3) or **Zoom In** from the **View** menu to activate the zoom cursor seen in Figure 14-4. The character displayed after the signal name indicates the type of signal (I = input, O = output, G = global...). Depending upon various settings within PAC-Designer, the **CLK\_IN** signal may be different from

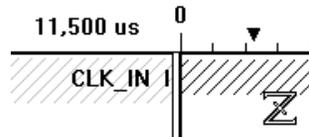
what is shown in this application note. The clock period may change and the number of clock cycles may be different. However, the steps outlined below pertain to any stimulus signal.

Figure 14-3. Zoom-in Tool



Place the zoom cursor near the far left of the signal (zero time index at the top of the window) and apply multiple clicks to zoom in on the waveform. This will reveal the details of the **CLK\_IN** signal as seen in Figure 14-5. To cancel the “Zoom-In” mode and cursor, apply a single right click.

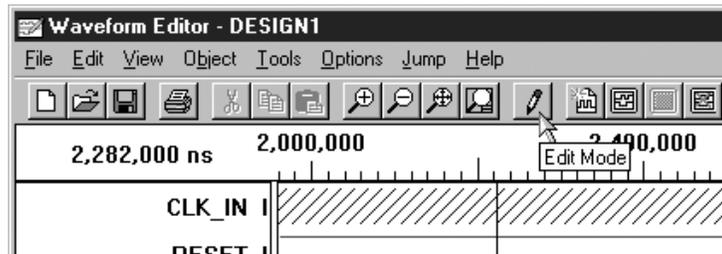
Figure 14-4. Zooming in on the CLK\_IN Signal



### Using Edit Mode

If the “**Selected Pattern (...)**” dialog box (that is shown in Figure 14-6) is not open, click **Edit Mode** from the **Object** menu or the **<Edit Mode>** tool (shown in Figure 14-5) to open the dialog box that will be used to edit and modify waveforms.

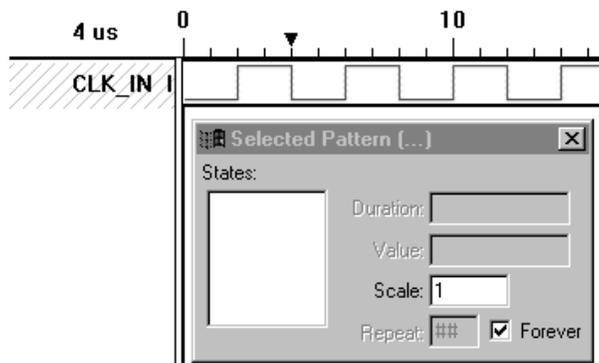
Figure 14-5. Edit Mode Tool



### Modifying CLK\_IN

The CLK\_IN waveform is the main clock for the simulator, and represents either the internal clock or the external clock of the ispPAC-POWR1208. Click and drag across the **CLK\_IN** waveform to select it, as indicated by the heavy solid lines above and below the waveform. This waveform is repeated forever, as indicated in Figure 14-6. In the edits that follow, this waveform will be shortened to speed up the simulation time, and the period will be modified to simulate a 2.5% slower clock.

Figure 14-6. Selecting the CLK\_IN Signal



### Setting the Time Base

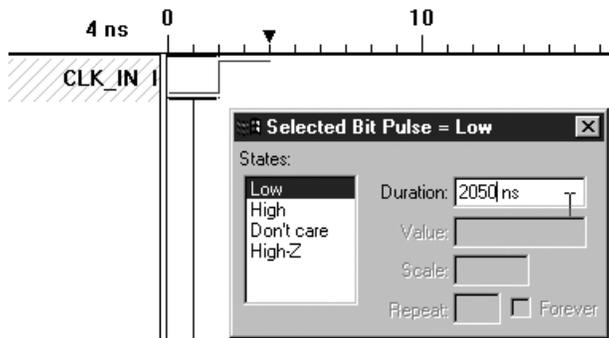
The Waveform Editor time scale can be set to the resolution needed to show the detail of the signals being edited. To set the time scale to 1.0ns, click **Timing Options...** from the **Options** menu to bring up the “**Timing Options**” dialog box which is shown in Figure 14-7. Note that when changing the time scale, the waveforms do not preserve absolute time information. This is seen by comparing Figure 14-6 and Figure 14-8, where the **CLK\_IN** period went from 4μs to 4ns, when the time scale was changed from 1μs to 1ns.

Figure 14-7. Setting the Default Time Scale



To bring the **CLK\_IN** period up to 4.1μs from 4ns and maintain a 50% duty cycle, the duration of both the Low and High segments will be edited. Place the cursor over the Low portion of the waveform and click to select just that portion, as indicated by the heavy solid lines above and below the segment. Edit the Duration to **2050ns**, as shown in Figure 14-8, press **<Enter>** for the change to take effect (see Figure 14-9). This will also move the waveform selector to the next segment.

Figure 14-8. Editing CLK\_IN Low duration



When **<Enter>** is pressed after editing the duration, the view is scrolled to the next segment of the waveform at the same zoom factor, to support multiple edits along that waveform. With the High segment of the **CLK\_IN** signal selected (as shown in Figure 14-9), edit the duration to **2050ns** and press **<Enter>**. To see the entire waveform as shown in Figure 14-10, zoom out near the beginning. Single click twice in a row to select first the Low segment, then the entire waveform, as shown in Figure 14-10. Enter **6000** in the “Repeat:” edit box, as the number of times to repeat the pattern. This will provide 24.6ms of **CLK\_IN** stimulus for the simulation. Alternatively, if the simulation time is unknown, the “Repeat Forever” box can be checked. **Warning:** When using “Repeat Forever” on an 800MHz Pentium computer, a typical design with a 250kHz **CLK\_IN** will take over five hours and will create eight gigabytes of data files because of the 400 second limit of the simulator.

Figure 14-9. Editing CLK\_IN High Duration

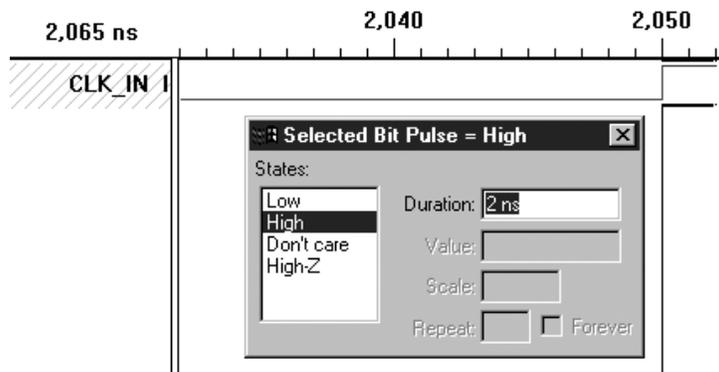
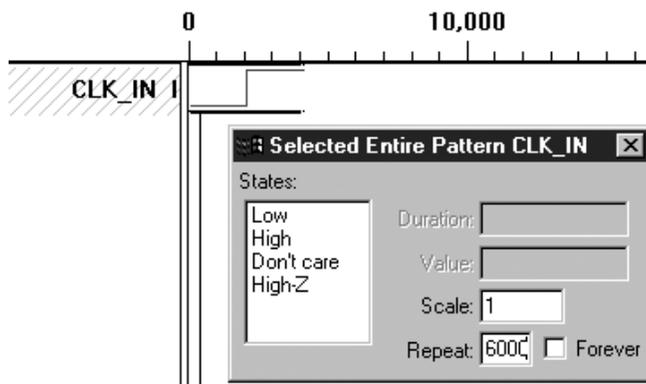


Figure 14-10. Repeat the CLK\_IN Pattern 6000 Times



### Adding the Reset Waveform

Click the **<New Wave>** tool (shown in Figure 14-11) or **New Wave...** from the **Edit** menu to add a new waveform to the stimulus file. To add a **RESET** waveform to the stimulus file, enter the name in the “Add New Wave” dialog box, and click on the **<Add>** button as shown in Figure 14-12. This will place the text label on the left of the screen and highlight it with cross-hatching.

Figure 14-11. Adding a New Waveform to the Stimulus File

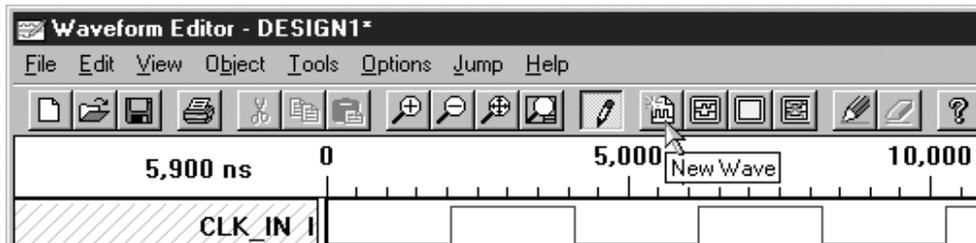
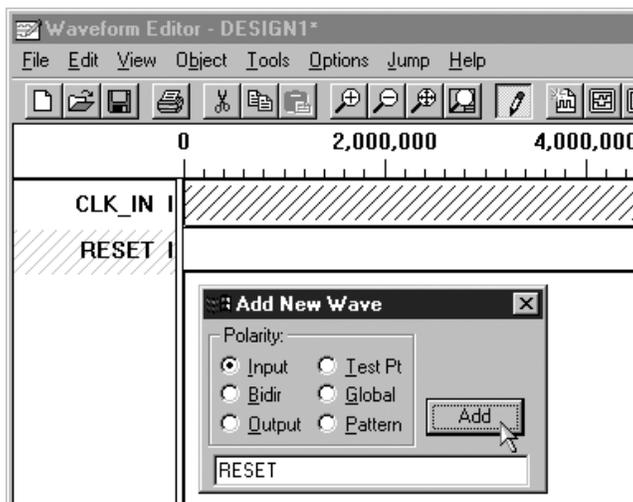
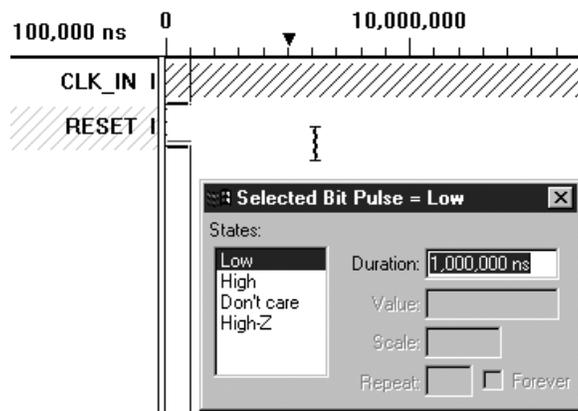


Figure 14-12. Adding a RESET Signal to the Stimulus File



Zoom out to a scale that is similar to that shown in Figure 14-12 (right click to cancel the zoom). Place the cursor horizontally in line with the text and vertically away from the zero time mark. Click the mouse to establish the first segment of the **RESET** waveform. Alternatively, this first segment can be established by clicking and dragging toward the zero time line. Change the properties of the selected segment to Low and duration of 1ms by making the required changes in the dialog box that is shown in Figure 14-13.

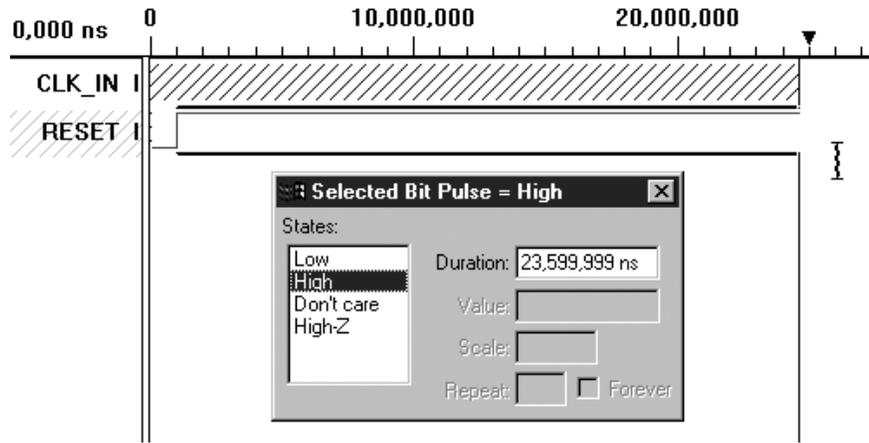
Figure 14-13. Editing the RESET Waveform to Start Low with a Duration of 1ms



Move the cursor to the right, just under the end of the **CLK\_IN** waveform and click to create a transition to the High portion of the **RESET** waveform as shown in Figure 14-14. Course adjustment of this transition can be accom-

plished by clicking and dragging with the mouse and precise adjustment is provided with the “Selected Bit” dialog box.

Figure 14-14. Editing RESET High Duration to 23.5ms



**Adding the VMON1 Waveform**

In step one of the sequence (Figure 14-1), the instruction “Wait for VMON1” will wait for VMON1 to be true. Thus, the stimulus file will have to have a **VMON1** waveform added to it, as shown in Figure 14-15. When a new waveform is added, the default for the first segment is High. To change the initial segment of **VMON1** from High (as seen in Figure 14-16) to Low and to have a duration of 4ms, make the required changes in the “Selected Bit” dialog box. Repeat the process outlined for the **RESET** waveform to add and edit the next segment of the **VMON1** waveform. Note that the simulator will extend the last state of any waveform to time required to simulate the longest waveform. So the duration of the High segments of either **RESET** or **VMON1** do not need to line up exactly under the end of the **CLK\_IN** waveform. Also note that the user defined input names can be copied from the PAC-Designer dialog boxes, using <Ctrl-C>, and pasted, using <Ctrl-V>, into the edit window of the “Add New Wave” dialog box of the Waveform Editor. This will insure the correct signal names are used in the simulation.

Figure 14-15. Adding VMON1 to the Stimulus File

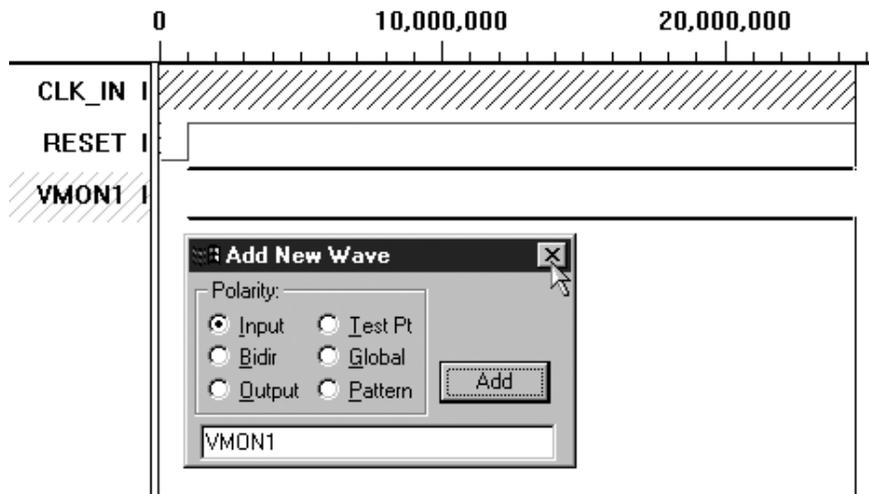
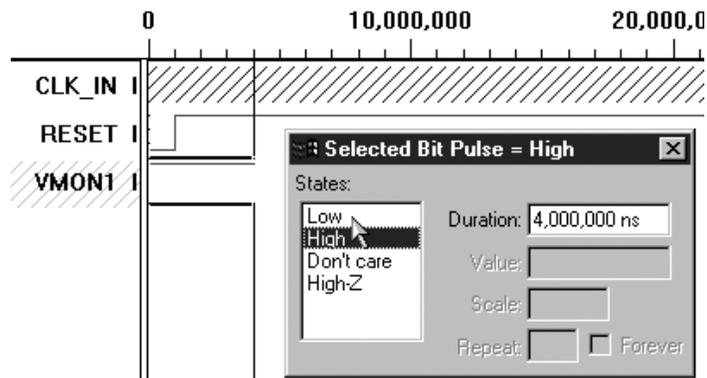


Figure 14-16. Editing VMON1 to start Low for 4ms



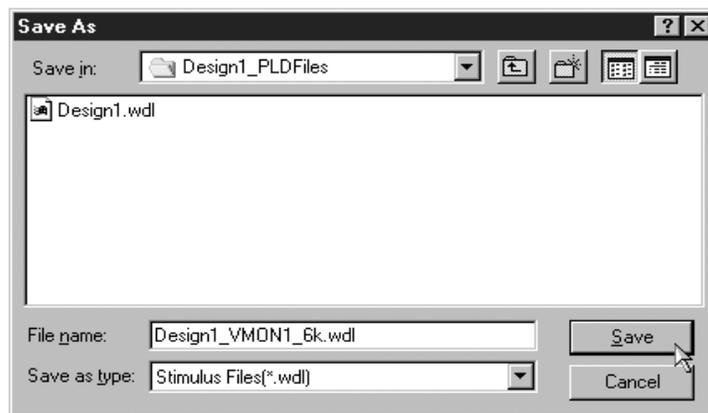
### Adding Output Waveforms

As an option, the user-defined output signal names from PAC-Designer can also be added to the stimulus file with the “Add New Wave” dialog box by checking the **Output** button. Just adding the signal names is all that is required to have the Waveform Viewer automatically display or “show” them when the simulation is complete. Thus, output signals do not need waveforms, because the simulator will define their states. Alternatively, the outputs can be seen in the Waveform Viewer by using the “Show Waveforms” dialog box, as discussed later in the *Viewing the Simulation Output* section.

### Saving the Edits

When the modified stimulus file is ready to be saved, click **Save As...** from the **File** menu to give the file a unique name based on the signals and duration (or other information contained in the file). In Figure 14-17 the filename contains both the input signal name **VMON1** and the duration of clocks in cycles (6k). Alternatively, the time duration of 24ms could have been used in the name (Design1\_24ms.wdl or Design1\_VMON1\_24ms.wdl). At this stage, the Waveform Editor creates two files, Design1\_VMON1\_6k.wet and Design1\_VMON1\_6k.wdl. The \*.WET file contains the names of the nodes or signals for which you have created waveforms. The \*.WDL file contains the waveforms themselves, in the WDL (waveform description language) format.

Figure 14-17. Saving the modified stimulus file



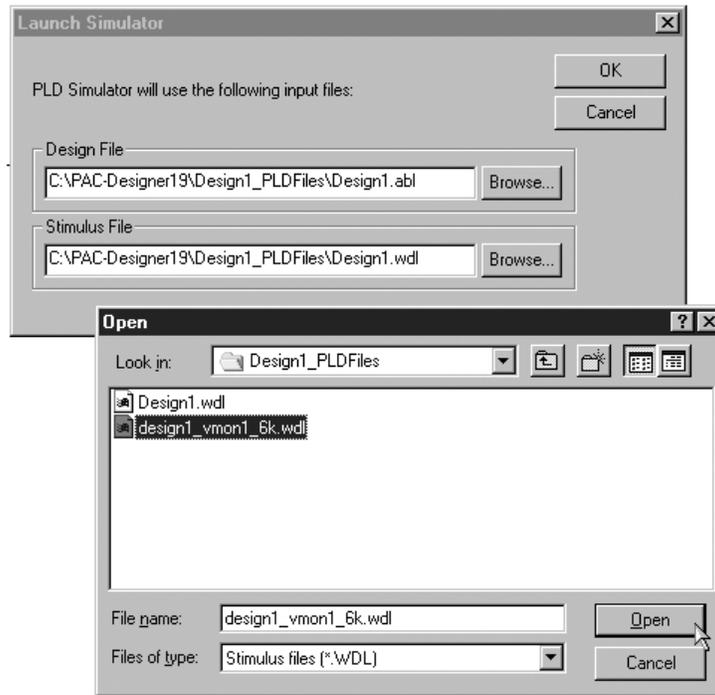
## Running the Simulator

From the LogiBuilder window in PAC-Designer, click **Run PLD Simulator...** from the **Tools** menu to start the simulation process. This menu selection will bring up the “**Launch Simulator**” dialog box.

### Specifying The Stimulus File

Use the lower Browse button to select the modified stimulus file (as shown in Figure 14-18). Then click on the <OK> button to start the simulator. PAC-Designer will remember this stimulus file, and future simulations can be initiated by simply clicking on the <PLD Simulator> tool, which is shown in Figure 14-19.

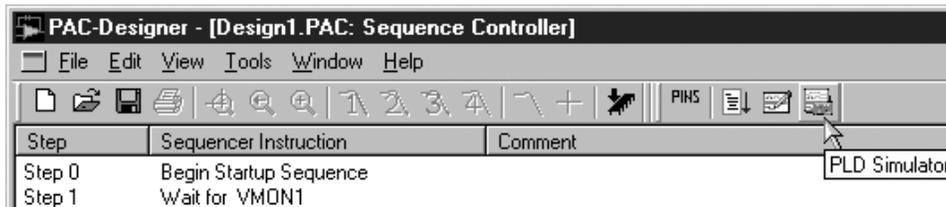
**Figure 14-18. Specifying the Stimulus File**



### Simulator Tool

In subsequent simulations, simply clicking on the <PLD Simulator> tool (shown in Figure 14-19) will start the simulation process directly without bringing up the “**Launch Simulator**” dialog box, but will use the same stimulus file that was used in the last simulation.

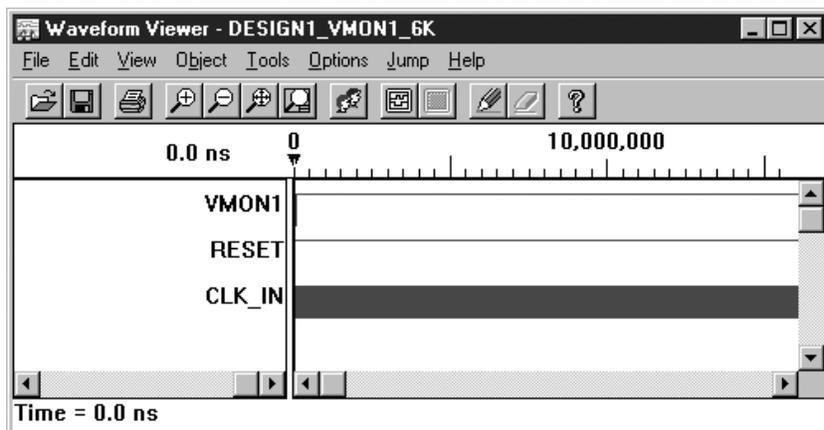
**Figure 14-19. PAC-Designers PLD simulator tool**



## Viewing the Simulation Output

When the simulation is complete, the Waveform Viewer application will be launched to display the results of the simulation (see Figure 14-20). The **CLK\_IN** and **RESET** signals defined in the stimulus file will be displayed by default.

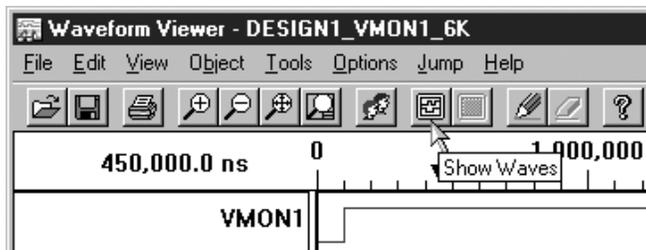
Figure 14-20. Simulation Done - Waveform Viewer



## Adding Waveforms to the Display

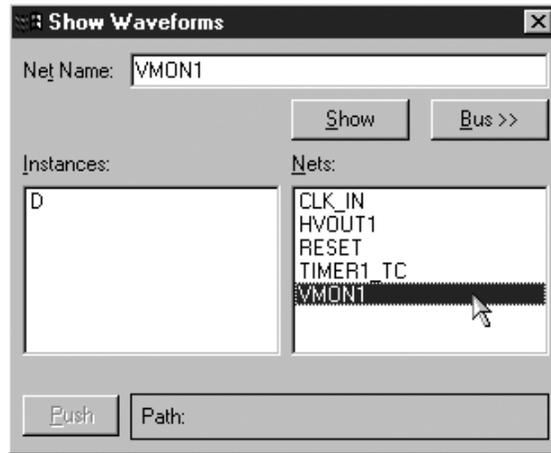
Click the <Show Waves> tool (shown in Figure 14-21) or **Show...** from the **Edit** menu to bring up the “**Show Waveforms**” dialog box. This dialog box (shown in Figure 14-22) is used to select which signals are to be displayed.

Figure 14-21. Show Waveform Tool



Adding signals to the view is as simple as double clicking on the name in the “**Nets:**” list. Add the signals **VMON1**, **HVOUT1**, and **TIMER1\_TC** to the view in this manner. by clicking on it.

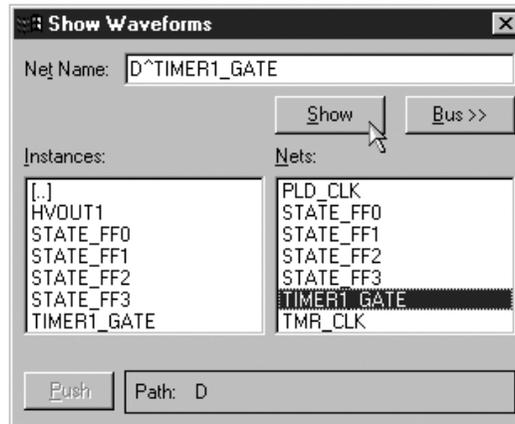
Figure 14-22. Adding VMON1 for Viewing



### Adding Internal Signals to the Display

To add internal signals to the view, “push” into this instance by double clicking on the “D” in the “Instances:” list. Or, highlight the “D” and click on the <Push> button. The appearance of the dialog box will change to be similar to that of Figure 14-23. Click on the **TIMER1\_GATE** signal to highlight it, then click on the <Show> button have it added to the view. This signal is an internal net and PLD output that enables timer 1.

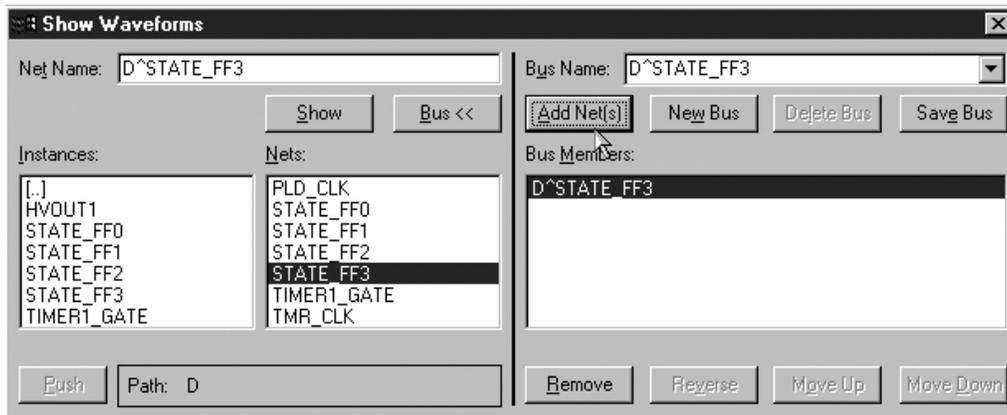
Figure 14-23. Adding an Internal Node - Gate of Timer 1 for Viewing



### Adding the Step Counter to the Display

Click on the <Bus> button to bring up bus interface portion of the dialog box as shown in Figure 14-24. Highlight **STATE\_FF3** and click on the <Add Net(s)> button to add the most significant bit of the step counter (also an output of the PLD) to the bus. Continue with the other bits, in order, down to the least significant bit **STATE\_FF0** as shown in Figure 14-25.

Figure 14-24. Adding the MSB of the Step Counter to a Bus



After all four bits have been added to the bus, change the default bus name from **\$Bus1** to **step** in the “**Bus Name:**” edit box, and click on the **<Save Bus>** button. The name **step** will appear in “**Net Name:**” edit box and clicking on the **<Show>** button will add the step counter to the view as shown in Figure 14-26. Adding the step counter to the simulation display is very helpful when debugging the design. For sequences of more than 16 steps, the **TIMER\_GATE** macrocells are diverted from the respective “unused” timer(s) and configured as the most significant bit(s) of the step counter. In these cases, the **TIMER\_GATE** signals have to be added above the **STATE\_FF3** signal to properly display the step. Increasing the maximum program size is done using PAC-Designer’s menu item **Set Maximum Program size** from the **Edit** menu.

Figure 14-25. Naming and Adding the Step Bus to the View

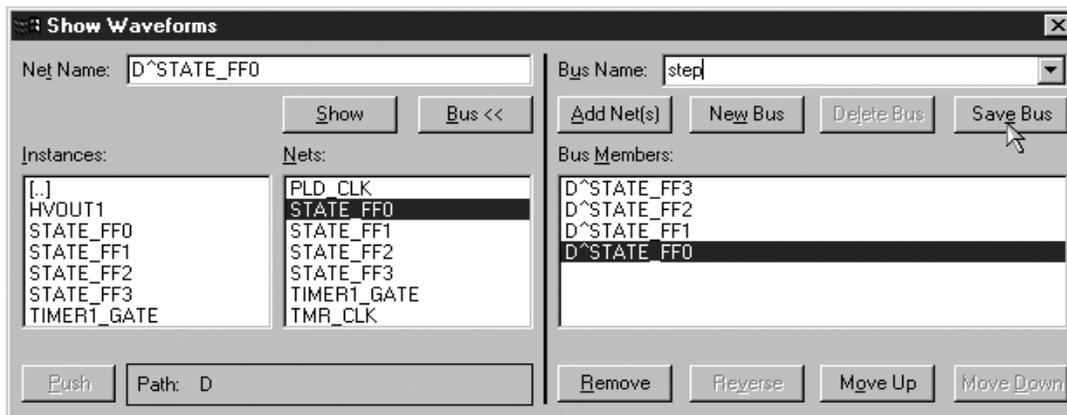
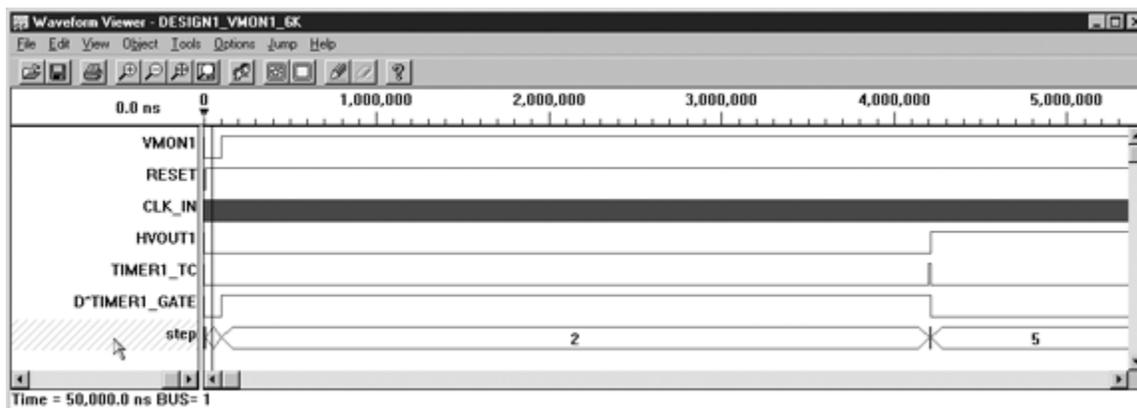


Figure 14-26. Waveform Viewer with All the Added Signals and the Step Counter



The **step** bus is decoded and displayed in the Waveform Window as two horizontal lines with the step number centered. When a step is too short, the display only shows a transition occurring but not the step number. To reveal the step numbers in these short steps, (for example before step 2) highlight the waveform and place the cursor in the center of the step. The decoded step value is displayed in the status bar (at the bottom of the screen) shown in Figure 14-26 as “BUS= 1.” Also, the “Zoom In” tool could be used until the step value is displayed on the waveform.

### Changing the Bus Radix

To change the format in which the steps are displayed click **Bus Radix...** from the **Options** menu. The four available formats are shown in Figure 14-27.

Figure 14-27. Changing the Bus Radix from Hex to Decimal



### Using the Markers to Analyze the Output

Click the **<Place Marker>** tool (shown in Figure 14-28) or **Place Marker** from the **Object** menu to place a marker on specific events in the simulation output. After the first marker is placed, use the menu or tool to place a second marker. The difference in time between the two is displayed in the status bar (at the bottom of the screen) as shown in Figure 14-29. The time from **VMONT** tripping to **HVOUT1** turning on is displayed as 4.21ms. The additional 110µs results from the step latency. This additional delay can become quite significant if the PLD Clock Frequency were to be lowered using the PAC-Designer “**Clock & Timer Settings**” dialog box.

Figure 14-28. Selecting the Place Marker Tool to Measure Timer 1

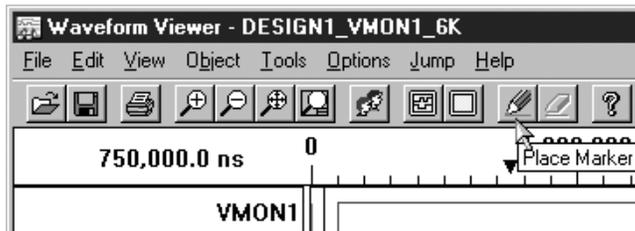
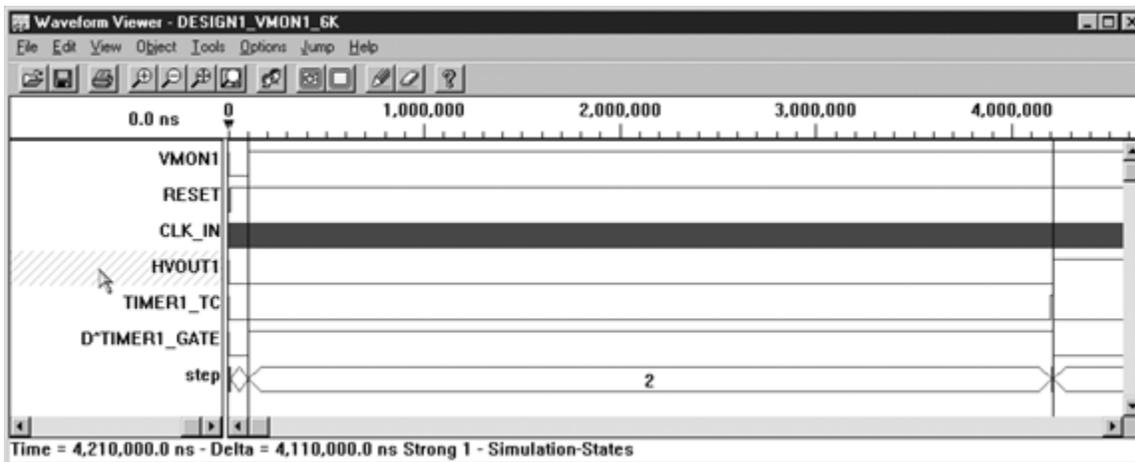


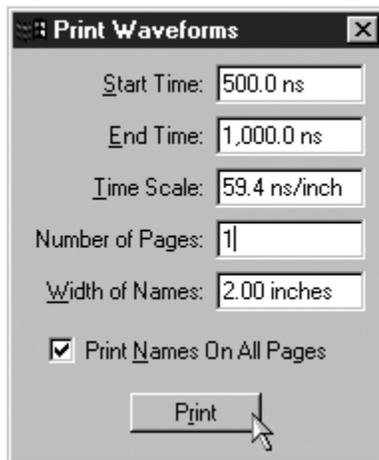
Figure 14-29. HVOUT1 turns on 4.1 ms After VMON1 (Using Timer 1 for the Delay)



### Printing the Results

Click on the <Print> tool or **Print...** from the **File** menu to bring up the “**Print Waveform**” dialog box (as shown in Figure 14-30). This dialog box can be used to “zoom” the printer in by setting the “**Start Time:**” and “**End Time:**” or “**Time Scale:**” The number of pages can also be set from one to as many are needed to display the detail required.

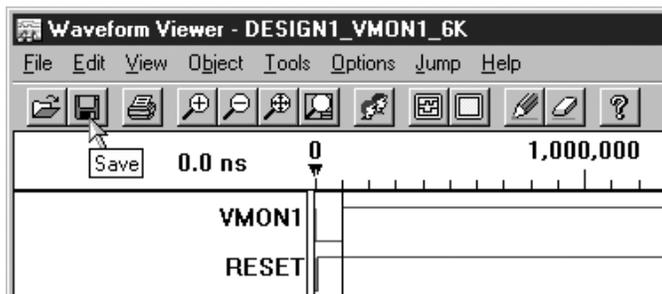
Figure 14-30. Print Waveforms Dialog



## Keeping the Changes for the Next Simulation

After reviewing the simulation output, one may recognize that either the stimulus file or the design needs a slight change. Before returning to PAC-Designer to restart the design, compile, simulate cycle, save the changes made by clicking on the **<Save>** tool (shown in Figure 14-31) or **Save** from the **File** menu. So that the next simulation will automatically display all the waveforms and buses that have been added to the view.

*Figure 14-31. Saving the changes to the WAV file*



## Summary

In this application note we have taken a simple design from stimulus to simulation. We have covered the essential details of creating and editing stimulus files. We have also shown how to use the tools within the Waveform Viewer to debug designs. Both the waveform editor and viewer are just a tool click away from the PAC-Designers LogiBuilder interface and are rich in features that are beyond the scope of this application note. The combination of these three tools greatly simplifies the effort required to design, simulate, and debug a power-supply sequencing design.

## Related Literature

- ispPAC-POWR1208 Data Sheet

## Technical Support Assistance

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+1-408-826-6002 (Outside North America)  
e-mail: [isppacs@latticesemi.com](mailto:isppacs@latticesemi.com)  
Internet: [www.latticesemi.com](http://www.latticesemi.com)

## Revision History

Date	Version	Change Summary
January 2003	01.0	Initial release.
April 2008	01.1	Title changed from "Simulating Power Supply Sequences for the ispPAC-POWR1208 Using PAC-Designer LogiBuilder" to "Simulating Power Supply Sequences for Power Manager Devices Using PAC-Designer LogiBuilder."